Formation and nonvolatile memory characteristics of multilayer nickel-silicide NCs embedded in nitride layer

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Wei-Ren Chen,[1] Ting-Chang Chang,[2,a)] Jui-Lung Yeh,[3] S. M. Sze,[3] and Chun-Yen Chang[3]
[1]*Institute of Electronics, National Chiao Tung University, Taiwan, Hsin-Chu 300, Taiwan*
[2]*Department of Physics and Institute of Electro-Optical Engineering, and Center for Nanoscience and Nanotechnology, National Sun Yat-Sen University, Kaohsiung 804, Taiwan*
[3]*Institute of Electronics, National Chiao Tung University, Taiwan, Hsin-Chu 300, Taiwan*

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The authors provided the formation and memory effects of nonvolatile multilayer nickel-silicide nanocrystal memory in this study. This proposed structure can efficiently improve the drawbacks of current floating gate and single-layer nanocrystal memories for the next-generation nonvolatile memory application. The charge trapping layer of multilayer structure was deposited by sputtering a commixed target ($Ni_{0.3}Si_{0.7}$) in the argon and nitrogen ambiance, and then used a low temperature rapid thermal annealing to form uniform nanocrystals. Transmission electron microscope images clearly show the multilayer and single-layer nanocrystal structures embedded in SiN_x. X-ray photoelectron spectroscopy and x-ray diffraction also present the chemical states and crystallization of nanocrystals under different annealing temperature treatments. The capacitor with different memory structures was also studied and exhibited hysteresis characteristics after electrical operation. In addition, the multilayer nanocrystals revealed better charge storage ability and reliability than the single-layer nanocrystals. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3006126]

I. INTRODUCTION

Nonvolatile nanocarbon (NC) memories and polysilicon-oxide-nitride-oxide-silicon (SONOS)-type memories have recently been promising candidates to take the place of the conventional floating gate nonvolatile memory because the discrete quantum wells and traps as the charge storage media have effectively improved data retention for the scaling down devices.[1–3] Although the scaling down tunnel oxide (<4 nm) is defect-free and of high quality, it is still difficult to prevent the storage charges to leak into substrate under retention test. Because of the quantum effect factor, the wave function of stored electrons can appear in the silicon substrate resulting in larger tunneling probability to increase the charge loss for retention state.[4,5] In the pervious studies, the high-*k* materials can be used to increase the physical thickness of tunnel oxide layer and achieve the same efficiency for scaling down process, such as Si_3N_4, HfO_2, and Al_2O_3.[4,6] Moreover, Ng *et al.*[7] proposed a densely stacked silicon NC layer to keep the better retention time because the charges stored in the NCs near the blocking oxide have low tunnel probability to leak into substrate. However, there are very few researches to investigate the formation and nonvolatile memory effect of multilayer metal NCs.

In our work, the formation and charge storage effect of nonvolatile multilayer nickel-silicide (NiSi) NC memory (NMLNCM) were revealed. The NCs were formed by the Ni–Si–N thin film and this proposed that memory structure was combined with the benefits of SONOS-type and multilayer NCs. Hence, we used the NMLNCM structure to compare with single-layer nickel-silicide NCs for the electrical characteristics of capacitance-voltage (*C-V*), retention, and endurance test in this study.

II. FABRICATION FLOW AND MATERIAL ANALYSES OF NCS

This memory cell structure was fabricated on a 4 in. *p*-type silicon (100) wafer. After a standard RCA process, which removed native oxide and microparticles, a 3-nm-thick tunnel oxide was thermally grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace. Subsequently, a 10-nm-thick nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer that served as the charge trapping layer was deposited by reactive sputtering of $Ni_{0.3}Si_{0.7}$ commixed target in the Ar [24 SCCM (SCCM denotes standard cubic centimeter per minute at STP)] and N_2 (10 SCCM) environment at room temperature. The dc sputtering power and pressure were set to 80 W and 7.6 mtorr. Here, the ratio of commixed target (Ni:Si) was decided by the volumes of NCs and surrounding dielectric. We first analyzed the composition of the charge trapping layer by x-ray photoelectron spectroscopy (XPS) system. Figure 1 shows the Ni $2p$ core-level photoemission spectra of the charge trapping layer which consist of two main peaks, $2p_{3/2}$ (~855 eV) and $2p_{1/2}$ (~873 eV), with two small satellite peaks by XPS system. According to the values of other literatures, Ni $2p_{3/2}$ binding energies are at 852.3 and 853.4 eV for metallic nickel (Ni–Ni) and Ni-silicide (Ni–Si), respectively.[8] However, it can not found that the above-mentioned peak signals are observed at the Ni $2p_{3/2}$ peak by our XPS result. Due to the strong electronegativity of nitrogen atom, the binding energy of Ni–Si bond would shift toward higher binding energy if

a)Electronic mail: tcchang@mail.phys.nsysu.edu.tw.

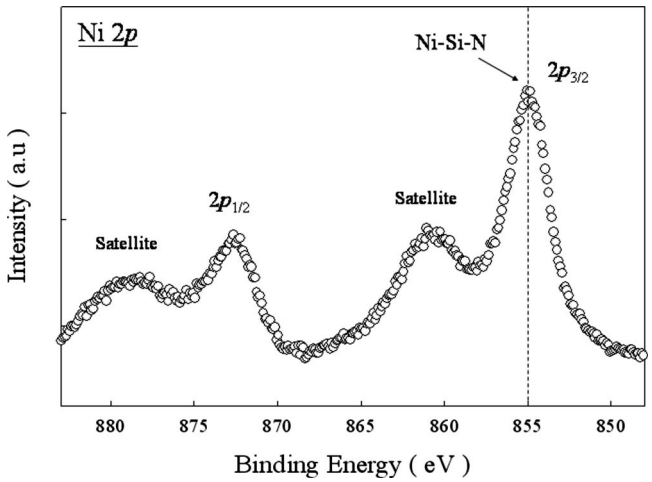


FIG. 1. Ni 2*p* XPS analysis of the NCs. Empty circles indicate experimental and dashed line is the peak of Ni–Si–N (855 eV).

the nitrogen atoms were bound with the Ni–Si compound. At this point, it was reasonably assumed that the charge trapping layer (as deposited thin film) could be assigned to the Ni–Si–N ternary bond. Hence, we could obtain a Ni–Si–N thin layer that serves as the charge trapping layer by sputtering a $Ni_{0.3}Si_{0.7}$ target in the Ar/N_2 environment in our work.

Next, a rapid thermal annealing (RTA) process was performed in N_2 ambient and the annealing condition was 600 °C for 100 s. After the annealing step, the NCs would self-assemble in the dielectric layer, and the single-layer NC memory structure was formed by capping a 30-nm-thick SiO_2 as the blocking oxide. The cross-sectional transmission electron microscope (TEM) and fabrication flow of NCs embedded in the nitride layer are shown in Fig. 2. Here, we further analyzed the chemical states of NCs to find that the peak signal of Si–N bond was shifted toward higher binding energy, and the peak signal of Ni–N was decayed gradually to disappear after the RTA process at 600 °C for 100 s by the N 1*s* results of XPS, as shown in Fig. 3(a). Besides, we also found that the peak of Ni–Si obviously appeared at 32.8° by x-ray diffraction (XRD) analysis after the annealing temperature treatment of 500 °C, as shown in Fig. 3(b). Therefore, we considered this as an internal competition characteristic of Ni–Si–N thin film due to the different Gibbs free energy

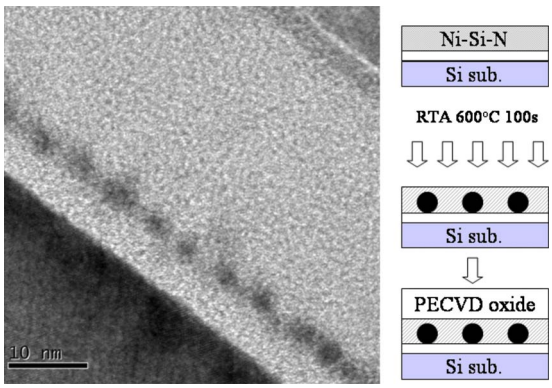


FIG. 2. (Color online) Cross-sectional TEM analysis and memory cell process flow of single-layer NCs.

of Ni–Si (−318 kJ mol^{-1}), Ni–N (−70–85 kJ mol^{-1}), and Si–N (−470 kJ mol^{-1}) to simply form the uniform NiSi NCs embedded in the nitride layer[9]

Moreover, we used this internal competition mechanism of Ni–Si–N thin film to fabricate the second NC layer of multilayer memory sample, and the annealing condition imitated the formed state of our first NC layer. Then, a 20-nm-thick blocking oxide was deposited on the charge trapping layer to completely make a multilayer NiSi NC memory. Finally, Al gate electrodes on the back and front side of the samples were deposited and patterned for our proposed memory structures. Form the NMLNCM cross-sectional TEM image of Fig. 4, it is found that the first deposited NCs layer was separated into two layers, and we believe that this phenomenon was caused by partial diffusion of NiSi NC into SiN_x during the second RTA process (the conjectured formation flow of multilayer NC structure is also shown in Fig. 4).[10,11] Therefore, the upper-layer NC size (5–6 nm) is larger than the lower-layer (2–3 nm) and we can use this material characteristic to fabricate the multilayer NCs. By TEM image analysis, there was a total of three layers of NCs in this proposed memory structure and the physical thickness of the memory cell was the same with the single-layer memory structure. Because of this, we were very interested in the nonvolatile memory effect of multilayer compared with single-layer NCs.

III. RESULTS AND DISCUSSIONS OF NONVOLATILE MEMORY EFFECT

Figure 5(a) shows the *C-V* characteristics of single-layer NC structure, and its memory window is only about 5 V under ±10 V gate voltage operation. However, the multilayer NC structure is clearly observed that the memory windows of 5 and 13 V can be obtained under ±5 and ±10 V operation, respectively, as shown in Fig. 5(b). The *C-V* hysteresis loops are counterclockwise, which is due to injection of electrons from the deep inversion layer and injection of holes from the deep accumulation layer of Si substrate.[12] The memory window of multilayer NC structure was much larger than the single-layer NCs at the same voltage sweeping (±10 V) condition. The enhancement of storage capacity was attributed to the high density number of NCs (three-dimensional structure) and strong coupling with conduction channel of metal NCs, which was related to the high dielectric constant of charge trapping layer.[13,14]

In addition, the difference in flat-band voltage between single-layer and multilayer was also due to strong coupling with conduction channel by the metal NC density (except the twice thermal annealing of multilayer). We provided a simple simulation of electric field (*E*) distribution for our proposed single-layer and multilayer NCs to explain the above-mentioned phenomenon, as shown in Fig. 6. Here we used the Integrated Systems Engineering TCAD software to build the single-layer and multilayer NC structures and model. The simulation conditions of NC structures corresponded with the TEM images (as shown in Figs. 2 and 4). Figures 6(a) and 6(b) show the cross-sectional *E* distribution of single and multilayer NCs whose black dashed line (red dash line) is a

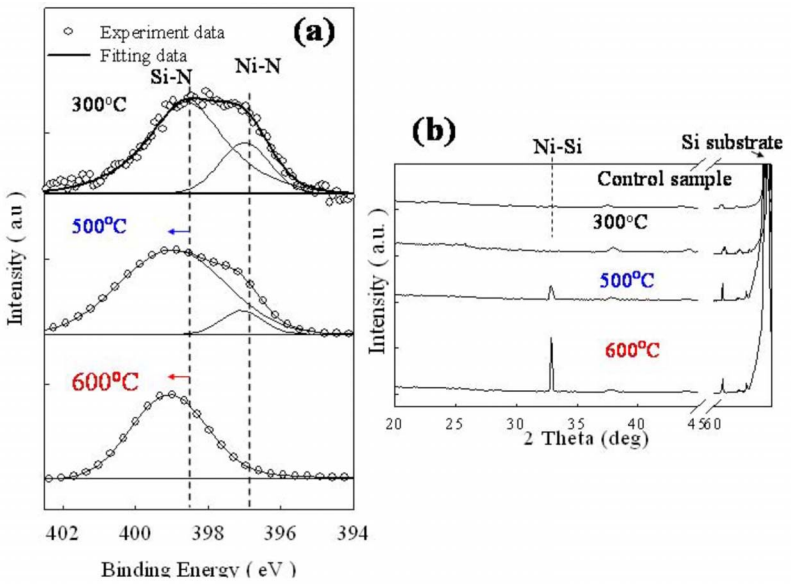


FIG. 3. (Color online) (a) N 1*s* XPS analysis of the NCs (empty circles and straight line indicate experimental and fitting results, respectively) and (b) XRD analysis of the NCs (control sample is only Si substrate with tunnel oxide) under different thermal annealing temperatures of 300, 500, and 600 °C.

distribution of vertical *E* across the NCs (without any NCs). To compare the vertical *E* between the tunnel oxide and the substrate for the single- and multilayer NCs, Figs. 6(c) and 6(d) present the vertical *E* distributions in black and red dashed lines. We can find that the vertical *Es* of the multilayer near the substrate are all larger than single layer and the distribution of *E* on the substrate for multilayer NC structure is more uniform by our simulation analysis. In the other words, the high density of metal NCs can enhance the gate control ability for the conduction channel in our work. Moreover, the large charge storage ability at scale-down devices can be maintained for the multilayer structure with NCs embedded in the nitride.

The endurance characteristics of multilayer NCs and single-layer NCs are provided in Fig. 7. Pulse conditions of $V_G - V_{FB} = \pm 5$ V for 0.1 ms were applied to evaluate endurance characteristics for the program/erase cycle operations. In the endurance test, first, we used this pulse condition to stress our samples and then programmed to a program state or erased to an erase state. After that, we used the read mode to detect the flatband voltage, V_{FB} (read mode: The V_{FB} is obtained by comparing the *C-V* curves from a charged state or a quasineutral state.). Figures 7(a) and 7(b) both show the negligible degradation of memory window up to 10^6 p/e cycles for the multilayer and single-layer structure. In the endurance test, our proposed memory structures had the advantages for the nonvolatile memory application.

Further analysis of the reliability indicated the charge retention properties of single-layer and multilayer NC memory structures at 27 and 85 °C, which are demonstrated in Figs. 8(a) and 8(b), respectively. Here, we purposely kept the same memory window, and this measurement results were carried out using a fixed gate voltage stress of ±5 V (10 and 2 ms for single layer and multilayer) at 27 and 85 °C. Hence, the shift in the flatband voltage as a function of time is obtained by comparing the *C-V* curves. From Fig. 8(a), we used an extrapolation to give a long-term predictable result (solid and dotted line) after 1000 s (stable region

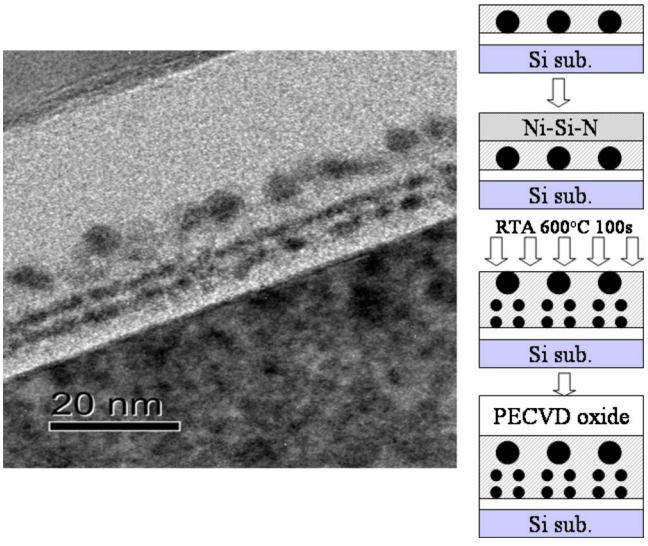
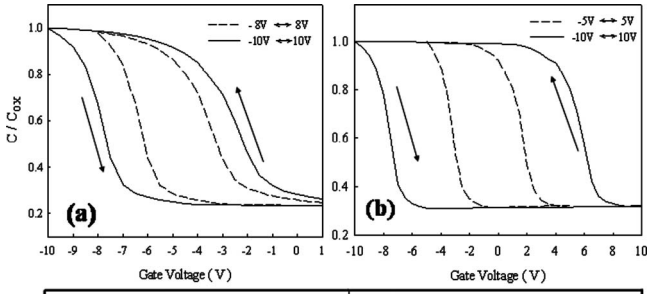


FIG. 4. (Color online) Cross-sectional TEM analysis and memory cell process flow of multilayer NCs. The first deposited NC layer was separated into two layers, and this phenomenon was caused by a partial NiSi NCs diffusing into SiN_x during the second RTA process.



Nonvolatile Memory	Memory window under ±10V
(a) Single-layer NiSi Nanocrystals	5 V
(b) Multi-layer NiSi Nanocrystals	13 V

FIG. 5. Capacitance-voltage (*C-V*) hystereses of memory structure with (a) single-layer and (b) multilayer NCs. The memory windows of (a) 5 and (b) 13 V can be obtained under ±10 gate voltage operation, respectively.

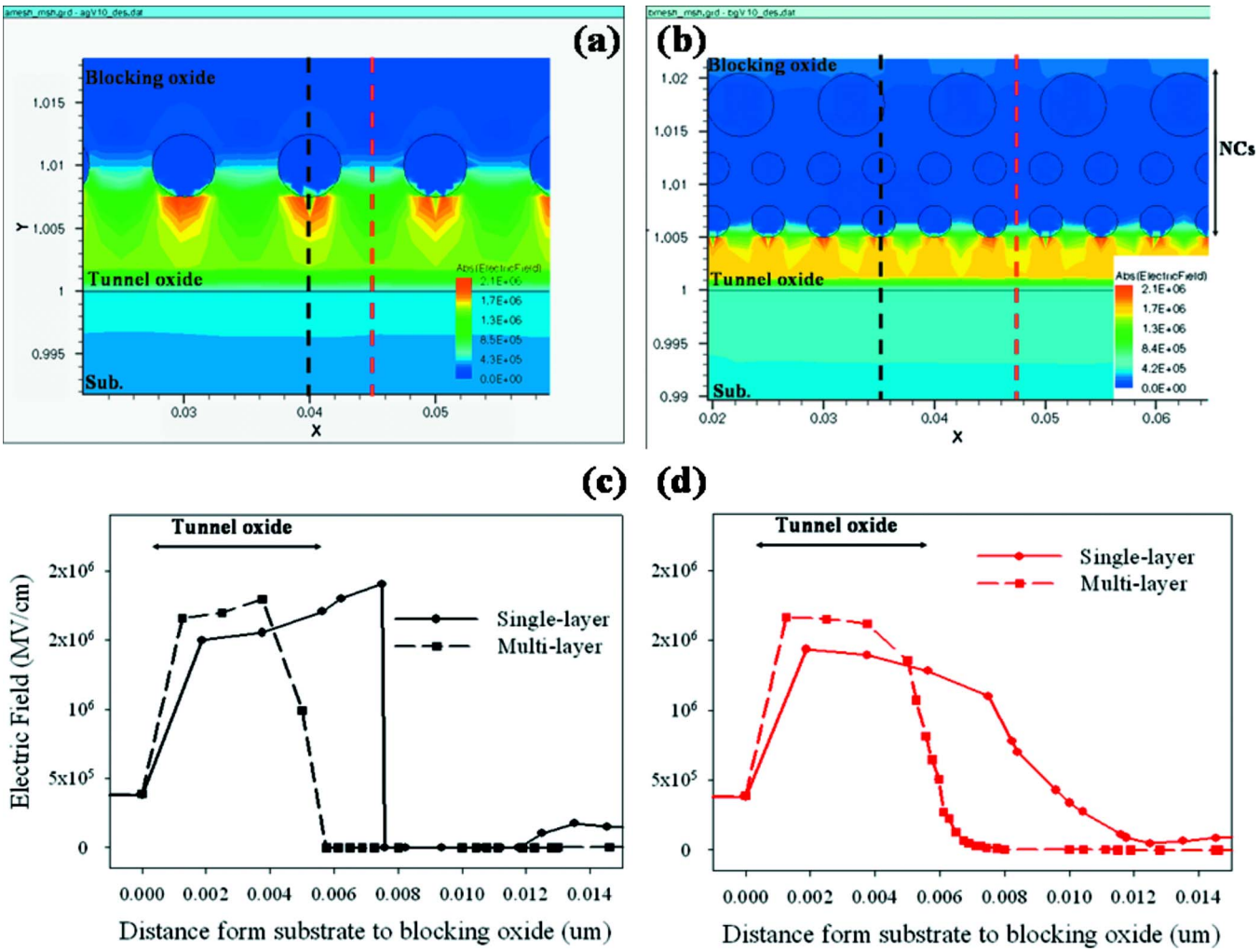


FIG. 6. (Color online) Simulation results of electric field distribution of (a) single-layer and (b) multilayer NiSi NCs embedded in nitride layer. Vertical electric field distribution comparisons of (c) black dashed line (across NCs) and (d) red dashed line (without any NCs) for the single-layer and multilayer NiSi NCs.

of retention).[15] We find that single-layer and multilayer NiSi NCs all have good chare storage ability and get up to 10 years at room temperature, as shown in Fig. 8(a).

However, a serious condition of 85 °C can show the advantages of multilayer NiSi NC memory, and it is found

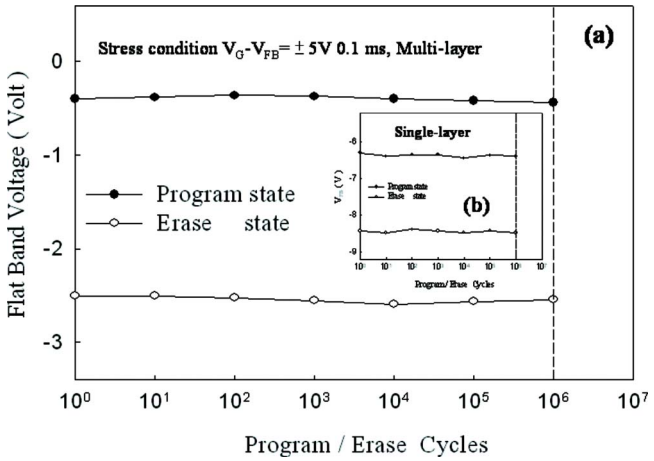


FIG. 7. (Color online) Endurance characteristics of (a) multilayer NiSi NC memory and (b) single-layer NiSi NC memory. Pulse conditions of $V_G - V_{FB} = \pm 5$ V and 0.1 ms.

that the charge loss ratio of a multilayer is much lower than single-layer NCs. In this study, we found that the leakage currents of single- and multilayer NC memories were very small. Therefore, the blocking oxide was enough to block the stored electrons leaking into the Al gate. If the stored electron loss is due to lateral migration effect, the retention test of single- and multilayer NC memories under 85 °C will have the same results. The biggest difference between single- and multilayer NC memory is the position of main stored carriers. The position of main stored carriers for only single-layer NC memory is like the first NC layer of multilayer NC memory. However, the position of main stored carriers for multilayer NC memory is the third NC layer.

Hence, based on the TEM images, we established an energy band diagram of multilayer NCs embedded in SiN_x layer (as shown in Fig. 9) to consider that the reason was due to the charges stored in the upper-layer NCs (the third layer of multilayer structure), which can be suppressed from leaking into substrate under thermal test by the Coulomb blockade effect and energy level quantization of the lower-layer NCs (the first and second layers of the multilayer structure).[16,17] The Coulomb blockade effect was caused by the carriers existing in second layer NCs (as shown in the

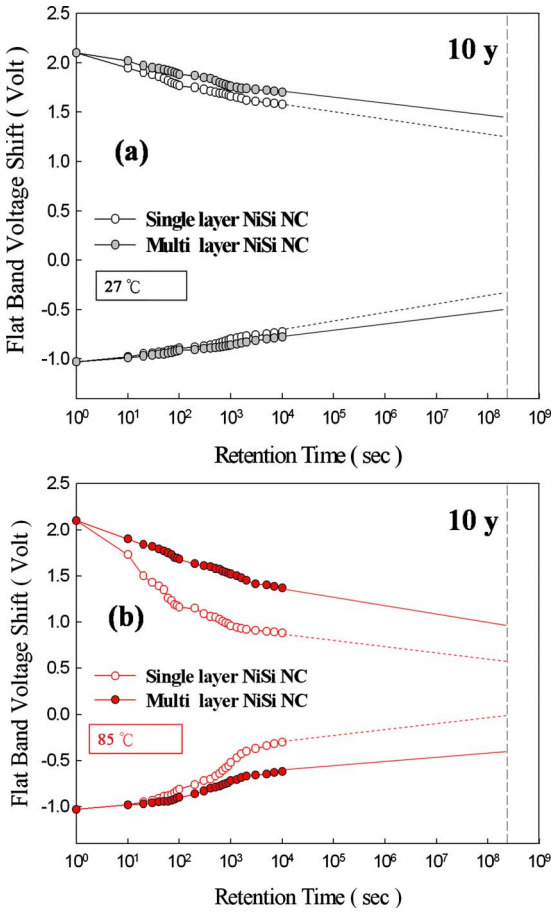


FIG. 8. (Color online) Retention characteristics of the NC memory structure with (a) room temperature, 27 °C, and (b) 85 °C. The dotted line and solid line are the extrapolated values of retention data after 1000 s; this range is a steady state.

second layer of energy band diagram), and this stored charge reduced the electron loss probability from the third layer to the first layer. In addition, the energy level quantization of NCs is limited to the size and effective mass of a NC. by the theoretical simulation of Guan *et al.*[17] Hence, in this model, the ground states (Fermi level) of first and second layers of the multilayer structure were higher than the third layer because their NC size was smaller than 3 nm. This Fermi level shift can partially suppress the electrons stored in the third NC layer from leaking into the first and second NC layers under thermal test. We also depicted this physical phenomenon in Fig. 9 to appear that the nonvolatile multilayer nickel-silicide NC memory can effectively keep carriers in the charge trapping layer for a harsh environment.

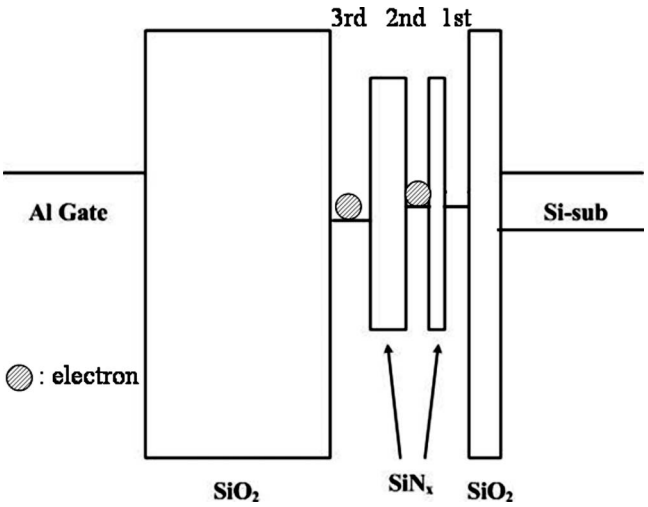


FIG. 9. Energy bond diagram of multilayer NiSi NCs embedded in SiN_x. The ground states of first and second layers of multilayer structure were caused by the energy level quantization effect.

IV. CONCLUSION

In this study we adopted the Ni–Si–N thin film to easily fabricate the NiSi NCs embedded in SiN layer after a RTA process and also proposed a nonvolatile NiSi NC memory with multilayer using low thermal budget. This multilayer NC structure exhibited superior memory performance for the charge storage capacity and reliability than single-layer NC sample. A larger memory window of 13 V was clearly observed after ±10 V voltage sweep and the retention can get up to 10 years for next-generation nonvolatile memory application. We also provided an energy band diagram of the multilayer NC structure to display the predominance of NMLNCM at scaling down process. In addition, this formation technique of charge trapping structure was also suitable for the low temperature substrate on the flexible electronics application.

ACKNOWLEDGMENTS

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