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A dual-phase charge pump circuit with compact size

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Abstract In this paper, a regulated dual-phase charge pump with compact size is presented. By means of a nano-ampere switched-capacitor voltage reference (SCVR) circuit, the dual-phase charge pump regulator can reduce the quiescent current and the output ripple. Besides, a new power stage is proposed to define the stability of the overall system. Owing to the design of buffer stage, the charge pump regulator can extend bandwidth and increase phase margin. Thus, the transient response and driving capability can be improved. Beside, the proposed automatic body switching circuit can efficiently drive the bulk of the power p-type MOSFETs to avoid leakage and potential latch-up. This chip was fabricated by TSMC 0.35 μm, 3.3 V/5 V 2P4 M CMOS technology. The input voltage range varies from 2.9 to 4.9 V for the lithium battery and the output voltage is regulated at 5 V. Experimental results demonstrate the charge pump can provide 50 mA maximum load current without any oscillation problems.

Keywords Voltage reference · Charge pump · Dual-phase power stage · System-on-chip (SoC) · Fast transient response · Output ripple

1 Introduction

The demand for the portable multimedia devices such as cellular phones, digital cameras, and personal digital assistant (PDA), etc., are the emerging market of the electronic devices, even called the daily essentials. For these popular portable devices, the operating time or standby time almost depends on the battery capacity and the conversion efficiency of power converters. However, the capacity of the battery increases at a slow rate and thus the usage time of these portable devices can be extended for a little period. In order to further extend the operating time of portable devices, the efficient power converters are the major consideration in the design of portable devices [1–4]. Beside, the size and weight of these power devices are also important for the users. Therefore, the miniaturization of the power converters and the reduction of the external component are essential in portable devices. That is, the power converters fabricated as a single chip or integrated into a system-on-chip (SoC) chip needs compact size and low cost. For the portable multimedia devices, the reduction of the area on silicon and print circuit broad (PCB) means lower fabrication cost and tinier size.

A compact size power converter is necessary for the power supply system of the SoC systems. In DC/DC power converters, the low drop regulator (LDO) sacrifices power conversion efficiency and decreases operating time of portable devices. The inductor-based switching converter generates high conversion efficiency, but uses a lot of external components. The charge pump regulator needs less external components than the inductor-based switching converter. The advantages of the charge pump regulator are small, quiet, and moderately efficient. The small board size and small silicon area are the special competitive advantage in the power converters. Thus, the power converter implemented by charge pump regulator becomes a good solution compared to the inductor-based switching circuits [5–8]. The charge pump provides an efficient approach the transfer different supply voltage levels. The energy usage in electronic systems efficiently improved by the charge pump regulators can extend the life time of the battery.

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Furthermore, the silicon area of the charge pump and the size of the external components on PCB are also very economic [9–13].

In order to achieve the compact size charge pump regulator, the switched-capacitor voltage reference (SCVR) circuit is used to instead of the conventional bandgap reference circuit and to integrate into the conventional charge pump regulator [14]. The SCVR circuit determines the output voltage and generates the regulating signal for charge pump regulator. Owing to the integration of SCVR circuit and error amplifier, the structure can effectively reduce the quiescent current and chip area. However, there is a regulating problem existed in integration of SCVR circuit and error amplifier. The output voltage is regulated only for one phase and thus the output voltage ripple is large. The regulation performance is deteriorated since the output voltage is regulated during only one phase [15]. Furthermore, the output dominate pole depends on load current and thus causes the unstable issue during load transient due to complex poles, which reduces bandwidth and phase margin. Thus, in order to reduce output ripple and ensure phase margin during load transient, the new proposed method describes a new regulated charge pump regulator with dual-phase regulation. The dual-phase power stage and the current mode buffer stage are presented in this paper.

The organization of this paper is as follows. Section 2 describes the structure and behavior of the proposed dual-phase charge pump regulator. Section 3 shows the implementation of the proposed dual-phase charge pump regulator. Experimental results are shown in Sect. 4. Finally, a conclusion is made in Sect. 5.

2 The structure and behavior of the proposed dual-phase charge pump circuit

Figure 1 shows the conventional schematic of the compact charge pump circuit which includes three major circuit stages. The bandgap stage is used to generate the temperature independent reference voltage and compare with the feedback signal. The sensor stage is used to monitor the regulation of output voltage and generate the regulating signal to power stage. In power stage, the regulating signal is converted to charging current of fly capacitor C_F and store energy for demand of output [9–13]. According to the conventional structure, the compact size charge pump can be achieved. Thus, the proposed dual-phase charge pump regulator is depicted as follows.

2.1 The combination of SCVR stage and sensor stage

In traditionally, the conventional bandgap reference circuit in Fig. 2(a) is used to generate the temperature independent reference voltage. The basic of the bandgap circuit is composed of resistors, operation amplifier (OPA), and bipolar junction transistors (BJT). Owing to the different size of BJT, the ΔV_{EB} is generated to provide the positive temperature coefficient and expressed as (1) and the reference voltage V_{REF} can be expressed as (2).

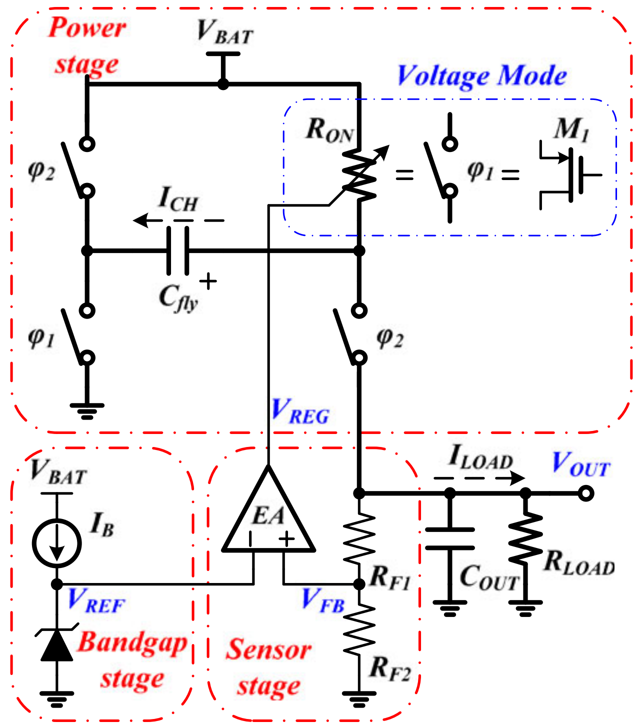


Fig. 1 The schematic of the compact charge pump circuit

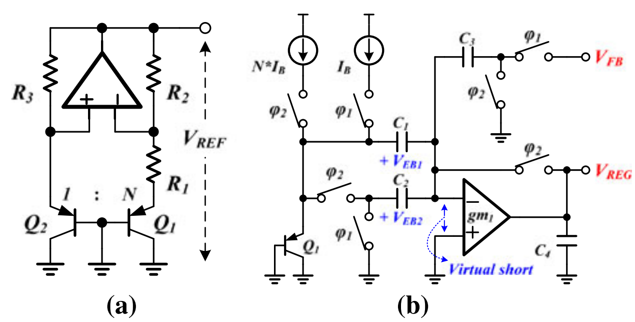


Fig. 2 **a** The conventional bandgap reference circuit and **b** the combination of SCVR stage and sensor stage in [13]

$$\Delta V_{BE} = V_{EB1} - V_{EB2} = V_T \ln N \tag{1}$$

$$V_{REF} = V_{EB2} + \left(\frac{R_2}{R_1}\right) V_T \ln N \tag{2}$$

where the V_T is thermal voltage and the factor N is the ratio of the two BJTs [16]. However, the conventional bandgap circuit occupies a lot of silicon area and consumes large quiescent current. The suitable reference circuit for miniaturization of power converter needs small silicon area and low quiescent current. According to the concept of conventional bandgap reference circuit, the term $\ln N$ should be kept at a constant value to minimize the temperature coefficient of the reference voltage. Thus, the combination of reference voltage stage and sensor stage in Fig. 2(b) is used to increase the integration of the proposed charge pump [14] and generate the regulating signal for the power stage. In this circuit, the different emitter-base voltage levels in single BJT are generated by different bias current during related clock phase. The voltage reference circuit not only reduces quiescent current, but also saves much silicon area. It also directly generates regulating signal for the power stage. During phase ϕ_2, the BJT is biased by NI_B and thus the voltage V_{EB2} is stored on the capacitor C_2. In the meanwhile, the operation transconductance amplifier (OTA) is switched to "reset" mode and the voltage V_{REG} is set to low. When the switches are changed to phase ϕ_1, the BJT is biased by the current I_B. The capacitor C_1 is used to store the value of V_{EB1}. The OTA is switched to the "amplify" mode and used to generate the reference voltage from the summation of the two different voltages with different temperature coefficients. Since the BJT is biased by the current I_B and NI_B during phases ϕ_1 and ϕ_2, respectively. The voltage difference ΔV_{EB} can be derived and shown in (3). When the V_{FB} and V_{REG} are shorted and after several charge distributions, the potential on every capacitor comes off its initial state and the charge at the inverter terminal of the OTA is stabilized. The reference voltage can be got by (4) according to the charge balance principle in (5).

$$\Delta V_{EB} = V_{EB2} - V_{EB1} = V_T \ln \frac{NI}{I_S} - V_T \ln \frac{I}{I_S} = V_T \ln N \tag{3}$$

$$V_{REF} = \frac{C_2}{C_3}\left(V_{EB2} + \frac{C_1}{C_2} V_T \ln N\right) \tag{4}$$

$$\Delta Q_1 + \Delta Q_2 = \Delta Q_3 \tag{5}$$

where $\Delta Q_1 = C_1 \Delta V_{EB1} = C_1 V_T \ln N$, $\Delta Q_2 = C_2 V_{EB2}$, and $\Delta Q_3 = C_3 V_{REF}$. Therefore, the parameter $(C_1/C_2)\ln N$ is fine tuned to determine the zero temperature coefficient of the reference voltage. The parameter C_2/C_3 is used to determine the scale of the reference voltage. There has one problem in the SCVR reference circuit. That is, the reference voltage only appears during the "amplify" mode, which is phase ϕ_1. Thus, the voltage of output only can be accurately regulated during phase ϕ_1.

2.2 The control methodology of power stage

Figure 1 shows conventional power stage which is the charge pump with a fixed switching frequency determines the output voltage by controlling the on-resistance of the switching transistors. In phase ϕ_1, the regulating signal V_{REG} is used to control the gate voltage V_{GS} of the MOSFET M_1 and determine the on-resistance and the charging current I_{CH}. When the power stage switches to phase ϕ_2, the flying capacitor C_{fly} delivers energy to output loads. The charging current I_{CH} can be expressed as (6), which depends on the operation region of MOSFET M_1 and names as the voltage mode control methodology.

$$\left.\begin{array}{ll} I_{CH(triode)} = K'\frac{W_1}{L_1}\left[(V_{GS} - V_{TH}) - \frac{V_{DS}}{2}\right]V_{DS} & 0 < V_{DS} \le (V_{GS} - V_{TH}) \\ I_{CH(sat)} = K'\frac{W_1}{L_1}(V_{GS} - V_{TH})^2 & 0 < (V_{GS} - V_{TH}) \le V_{DS} \end{array}\right\} \tag{6}$$

where K' is parameter of process. W_1 and L_1 are the width and length of MOSFET M_1. The V_{TH} is the threshold voltage. The V_{DS} is the different drain-source voltage level in MOSFET M_1. Owing to the flying capacitor C_{fly} store energy and increase voltage, the operation region of MOSFET M_1 may change from saturation region to triode region during the phase ϕ_1. Thus, the expression of the charging current I_{CH} is a nonlinear function of gate voltage V_{GS}. Furthermore, the nonlinear charging current of MOSFET is difficult to stabilize the control loop and to increase the reliability in the voltage mode control methodology. Due to the operation of the voltage mode, the value of the output resistance may become smaller than that of the load resistance at heavy loads. Thus, it may have a serious stability problem at heavy loads. The pole at the output node is defined as (7). Since a large value of C_{OUT} is selected as the output capacitor, the output pole becomes the dominant pole at light loads.

$$\omega_p = \frac{1}{(r_{O1}//R_{LOAD})C_{OUT}} \approx \frac{1}{R_{LOAD}C_{OUT}} \text{ at light loads} \tag{7}$$

where the R_{LOAD} is the load resistance and r_{O1} is the output resistance of the MOSFET M_1. However, at heavy loads, the output pole is smaller than the pole at the drain of MOSFET M_1 and becomes the first non-dominant pole.

That is, there are two low-frequency poles and may cause the serious stability issue at heavy loads. The simplest compensation method is to add a fixed dominant pole compensation at low frequency and thus the system can be stabilized. However, this method deteriorates the bandwidth and results in slow transient response. Besides, the output pole is moved toward the origin and causes the phase margin smaller than 60° at light loads. Thus, it has a minimum load requirement in the dominant pole compensation method.

In order to eliminate the mentioned problem in the voltage mode control methodology, the buffer stage in Fig. 3 is proposed to generate the current mode control methodology to replace the on-resistance control device. A voltage control current source (VCCS) circuit is used to instead of the on-resistance control device. That is, the MOSFET M_1 operates in the saturation and works as a current source. Owning to the design consideration of current mode control methodology, the charging current I_{CH} can be the linear function of regulating signal V_{REG}. The charging current is equal to (8)

$$I_{CH} = GmV_{REG} = GmA_{EA}(V_{REF} - \beta V_O) \tag{8}$$

where the Gm is the transconductance of VCCS circuit, A_{EA} is the gain of error amplifier, and the β is the ratio of feedback resistance which is equal to $R_{F2}/(R_{F1} + R_{F2})$. Therefore, the linear charging current becomes easy to stabilize the controlling loop and to increase the reliability in the current mode control methodology. In the meanwhile, the dominant pole is located at the output node since the output resistance of MOSFET M_1 is larger than the equivalent resistance of the switched capacitor, which is shown in (9).

$$r_{O1} = \frac{1}{f_{CLK} C_{fly}} \tag{9}$$

where the f_{CLK} is switching frequency of charge pump circuit. According to (6), in order to eliminate the effect of output resistance r_{O1} on the dominate pole, the value of the output resistance r_{O1} must much be larger than that of the output resistance R_{LOAD}. Therefore, the impedance of the flying capacitor must be set to be much smaller than the output impedance r_{O1} in (9).

2.3 The dual-phase charge pump regulator

Since the conventional voltage mode control charge pump regulator only exports the output current only half period. The charging or discharging current on the output capacitor is very drastic. Thus, the transient dip voltage is very large in case of load variations. Therefore, the dual-phase method is utilized, the output current from the charge pump regulator to the output load is continuous and thus the output ripple can be effectively reduced. As depicted in Fig. 4, owing to the SCVR circuit only provides the regulating signal V_{REG} during the phase ϕ_1, the asymmetric dual-phase charge pump regulator is proposed to provide an effective way to reduce the output voltage ripples and ensure the stability of charge pump regulator. In phase ϕ_1, the module 1 stores energy in flying capacitor C_{fly1} through VCCS circuit while the module 2 delivers energy stored in flying capacitor C_{fly2} to the output load through VCCS circuit. During phase ϕ_2, the module 1 delivers storage energy of flying capacitor C_{fly1} to output load and the flying capacitor C_{fly2} is fully charged in module 2. Owing to the waveforms of output have different phases to each other,

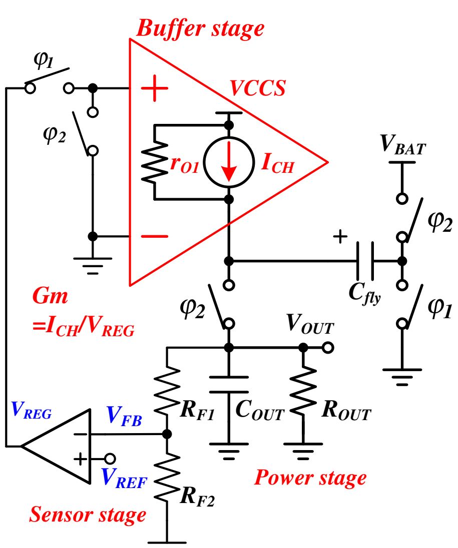


Fig. 3 The buffer stage is used as the output stage of the proposed regulator

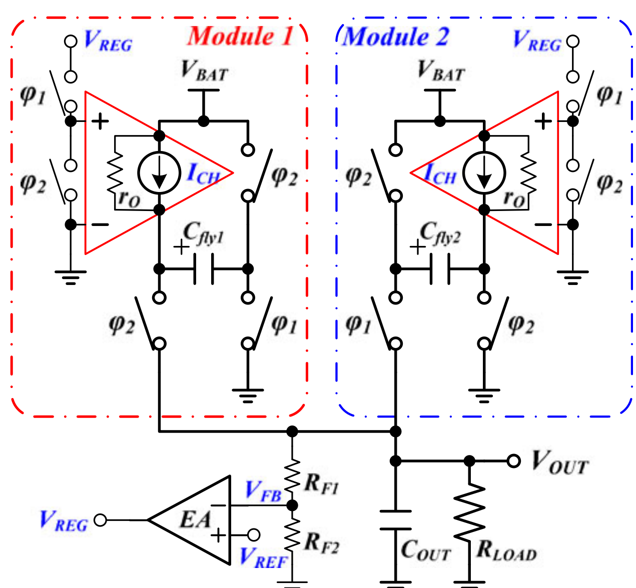


Fig. 4 The proposed asymmetric dual-phase charge-pump regulator

the output ripples can be reduced. The dual-phase regulator can provide twice driving current to the load and the output voltage ripple can be expressed as (10) when the equivalent series resistance (ESR) is considered.

$$V_{\text{ripple}} = \frac{I_{\text{LOAD}}}{2 f_{\text{CLK}} C_{\text{OUT}}} + 2 I_{\text{LOAD}} \text{ESR}_{C_{\text{OUT}}} \tag{10}$$

Figure 5(a) and (b) show the equivalent circuits in steady state during phases ϕ_1 and ϕ_2. In phase ϕ_1, the charging current I_{CH} of VCCS circuit is defined as (8) and the load current I_{LOAD} is drawn from the module 2. During phase ϕ_2, the load current is driven by the module 1 and flying capacitor C_{fly2} is fully charged. According to the equivalent charging current I_{CH} during the two phases, the charging currents can be expressed as (11) for the two phases, respectively. Thus, the output voltage expressed in (12) can be regulated to the multiple of the reference voltage V_{REF}.

$$\left.\begin{array}{ll} I_{\text{CH}} = GmA_{\text{EA}}(V_{\text{REF}} - \beta V_{\text{O}}) & \text{during phase } \phi_1 \\ I_{\text{CH}} = I_{\text{LOAD}} & \text{during phase } \phi_2 \end{array}\right\} \tag{11}$$

$$V_{\text{OUT}} = \left(V_{\text{REF}} - \frac{I_{\text{LOAD}}}{GmA_{\text{EA}}}\right)\left(1 + \frac{R_{\text{F1}}}{R_{\text{F2}}}\right) \approx \left(1 + \frac{R_{\text{F1}}}{R_{\text{F2}}}\right) V_{\text{REF}} \tag{12}$$

3 Implementations of proposed dual-phase charge pump

In Fig. 6, the completely compact size dual-phase charge pump regulator with current mode control methodology is illustrated. It includes the SCVR circuit, the buffer stage, the automatic body switch (ABS) circuit, and the dual-phase charge pump regulator. The complete circuit schematic of each function block is described as follows.

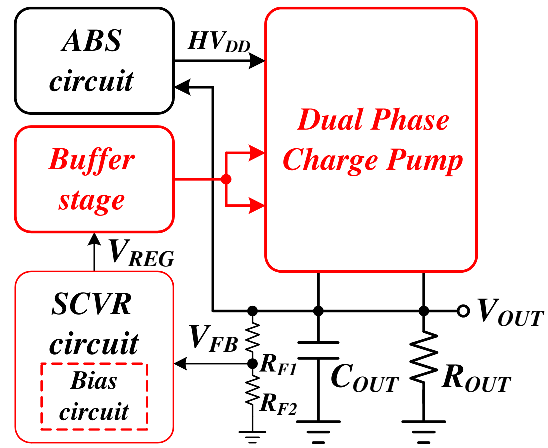


Fig. 6 The schematic of the compact size dual-phase charge pump circuit with current mode control methodology

3.1 The SCVR circuit

The complete schematic of SCVR circuit is shown in Fig. 7(a), which is composed of the start-up circuit, biasing circuit, a bipolar transistor, capacitors, switches, and an error amplifier. Transistors $M_{S1} \sim M_{S3}$ function as a start-up circuit for ensuring the operation of the biasing circuit. In the biasing circuit, transistors M_1 and M_3 are 5 V-NMOS transistors with higher threshold voltage and transistors M_2 and M_4 are 3.3 V-NMOS with lower threshold voltage. Owing to the M_1 and M_3 operate in the subthreshold region, transistors M_2 and M_4 operate in the saturation region. The drain currents of the NMOS operated in the saturation and

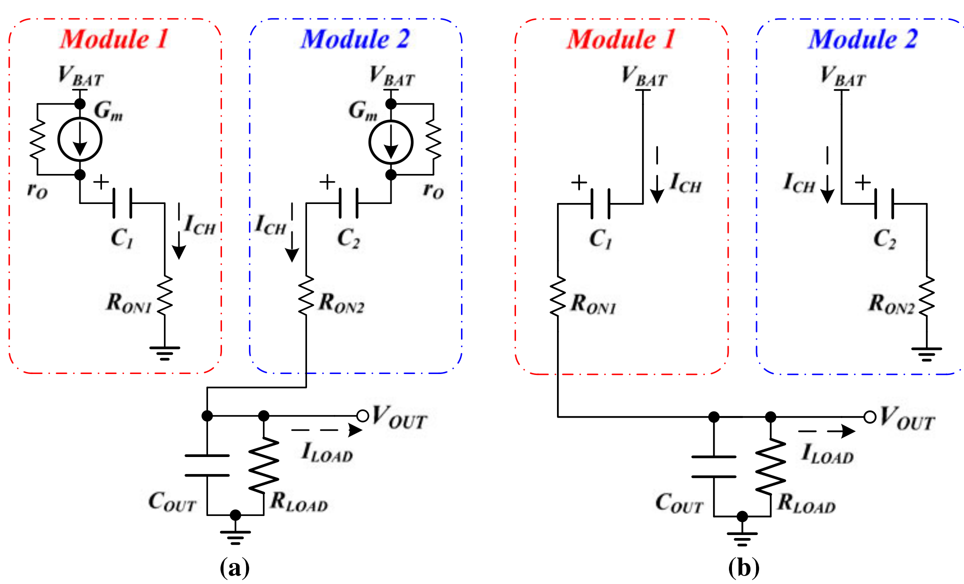


Fig. 5 The equivalent circuits of the power stage at the steady state **a** during phase ϕ_1 and **b** during phase ϕ_2

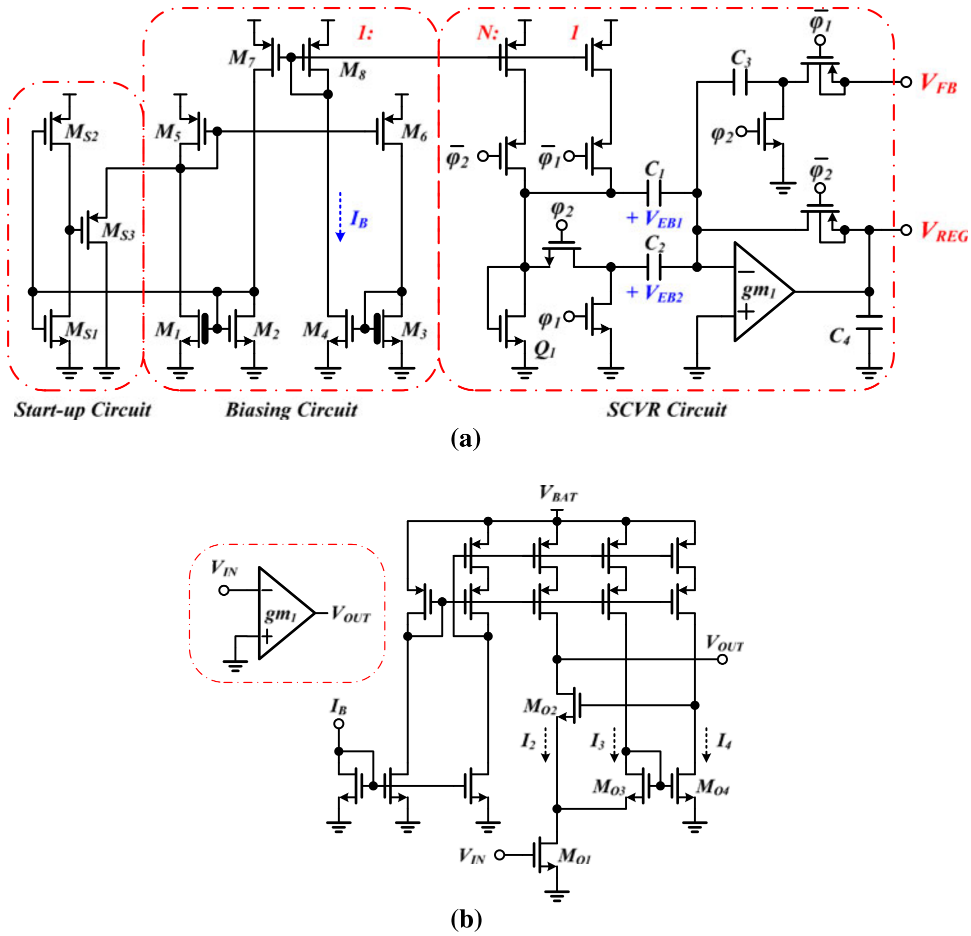


Fig. 7 **a** The complete schematic of SCVR circuit and **b** the high gain error amplifier

subthreshold regions can be approximated by (13) and (14), respectively.

$$I_{DS(Sat)} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad (13)$$

$$I_{DS(Sub)} = \mu_n V_T^2 \frac{W}{L}\exp\left(\frac{V_{GS} - V_{TH}}{mV_T}\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right] \quad (14)$$

where μ_n is the carrier mobility, C_{ox} is the oxide capacitance, λ is the channel length modulation parameter, m is the subthreshold swing parameter, V_T is the thermal voltage, W and L are the width and length of N-type MOSFET, respectively. The channel length modulation effect is neglected to derive the biasing current I_B as (15) according to the relationships $V_{GS1} = V_{GS2}$ and $V_{GS3} = V_{GS4}$.

$$I_B = \frac{\mu_n C_{ox}(W/L)_{M4}}{2(N-1)^2} m^2 V_T^2 \ln^2 \frac{(W/L)_{M3}}{(W/L)_{M1}} \quad (15)$$

where N is $\sqrt{(W/L)_{M4}/(W/L)_{M2}}$. The nano ampere of biasing current can be achieved in the design [5]. In the SCVR circuit, the switch with minimum size is used to eliminate the effect of charge injection. Furthermore, the nano ampere of biasing current is used to eliminate the voltage drop on the minimum size switches can be ignored. However, a high-gain error amplifier is needed to make sure the difference voltage generate the regulating signal V_{REG} without being affected by the offset voltage of the error amplifier as shown in Fig. 7(b). By means of the auto-zeroing technique, the offset voltage of the error amplifier can be cancelled in the switched-capacitor circuit [17]. Therefore, the error amplifier is designed by just a simple common-source cascode amplifier with gain-boosting technique for getting a high dc gain. Transistors M_{O3} and M_{O4} constitute a feedback loop to boost the output impedance and high gain. The feedback loop controls the value of the drain-source voltage of M_{O1}. The drain-source voltage of M_{O1} is equal to the difference between the gate-source voltages of M_{O3} and M_{O4} by (16).

$$V_{DS(M_{O1})} \approx \sqrt{\frac{2}{\mu_n C_{OX}}}\left(\sqrt{\frac{I_4}{(W/L)_{M_{O4}}}} - \sqrt{\frac{I_3}{(W/L)_{M_{O3}}}}\right) \quad (16)$$

According to (4), the term of C_1/C_2 is used to cancel the negative temperature coefficient of the voltage V_{EB}. The

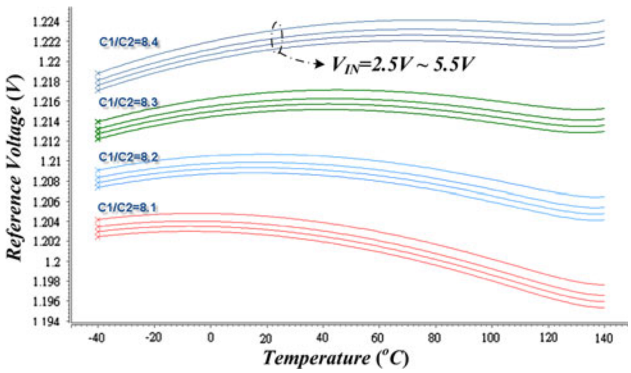


Fig. 8 The ratio of C_1/C_2 versus temperature and different supply voltage

simulation result of SCVR circuit is shown in Fig. 8. It shows four sets of capacitor ratio (C_1/C_2) under different supplying voltages. The ratio that makes the reference voltage almost constant at high temperature is the better choice since the operating temperature of the chip is often higher than the room temperature when the chip operates to deliver load current. Thus, the ratio $C_1/C_2 = 8.4$ is selected.

3.2 The buffer stage

The buffer stage is shown in Fig. 9 [18]. Transistors $M_{W1} \sim M_{W3}$ make the buffer stage to be turned off during phase ϕ_2 by the highest potential HV_{DD} in the whole charge-pump regulator. In order to speed up the transient response of the power MOSFETs, the transistor M_9 is used to pre-charge the gate capacitances of the power MOSFETs. When the output current is exported during the phase ϕ_1, the transistor M_9 is turned on to pre-charge the gate of the power MOSFET until the transistor M_7 can fully bias the transistor M_P. Transistors $M_2 \sim M_8$ function as the current mirrors for driving the power MOSFETs at the power stage. The input stage consists of the transistor M_1 and the resistor R_{Gm} as a simple V–I converter. The transconductance Gm can be expressed as (17) and be approximated as (18) by the assumptions that the resistor R_{Gm} is very smaller than the output resistance r_O of MOSFET and body effect and channel length modulation are ignored.

$$Gm = \frac{I_1}{V_{REG}} = \frac{gm_1 r_{o2}}{R_{Gm} + [1 + (gm_1 + gm_b)R_{Gm}]r_{o2}} \quad (17)$$

$$Gm \approx gm_1 \approx \mu_n C_{ox}\left(\frac{W}{L}\right)_{M1}(V_{REG} - V_{TH}) \quad (18)$$

The converted current I_1 is amplified to generate charging current by means of the connection of the current mirrors. The two current mirrors are composed of the transistors M_4, M_5, M_7, and M_P with the aspect ratios k_1 and k_2. Therefore, the overall transconductance of buffer stage can be approximated by (19).

$$\begin{aligned} Gm_{(all)} &= \frac{I_{CH}}{V_{REG}} = k_1 k_2 gm_1 \\ &= \mu_n C_{ox}\left(\frac{W}{L}\right)_{M1}\left(\frac{(W/L)_{M5}}{(W/L)_{M4}}\right)\left(\frac{(W/L)_{Mp}}{(W/L)_{M7}}\right) \\ &\quad (V_{REG} - V_{TH}) \end{aligned} \quad (19)$$

In (6), when the output resistance r_O of power MOSFET M_P is larger than the load resistance R_{LOAD}, the r_O in (6) can be eliminated. Thus, the dominate pole depends on the load resistance R_{LOAD}. Therefore, in order to eliminate the effect of output resistance r_O, the power MOSFET M_P must be operated in saturation region.

3.3 The dual-phase power stage

The dual-phase power stage is depicted in Fig. 10. The asymmetric structures are used to synchronize the regulating phase ϕ_1 of the SCVR circuit. In phase ϕ_1, the module 1 charges the energy on the flying capacitor C_{fly1}

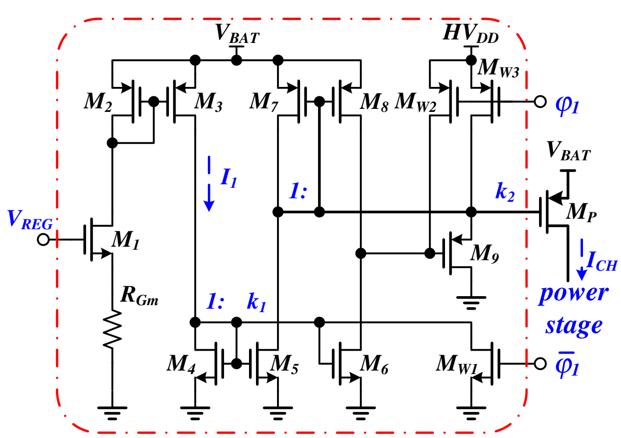


Fig. 9 The buffer stage

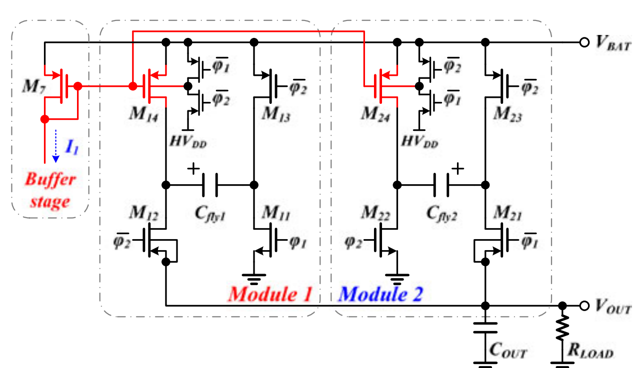


Fig. 10 The proposed asymmetric dual-phase charge pump regulator

by M_{14}. In the meanwhile, the transistor M_{24} in the module 2 delivers the charge on the flying capacitor C_{fly2} to the output load. During phase ϕ_2, the module 1 delivers storage energy of flying capacitor C_{fly1} to output load and the flying capacitor C_{fly2} is fully charged in module 2. In order to set the frequency of the output pole in a controllable range, the transistors M_{14} and M_{24} in Fig. 10 must be operated in saturation region. Therefore, the maximum voltage across the flying capacitor C_{fly} should be limited by (20) and the value of the flying capacitor C_{fly} can be decided by (21).

$$\Delta V_{C_{\mathrm{fly}},\mathrm{MAX}} = (V_{\mathrm{OUT}} - V_{\mathrm{SD,M12}}) - (V_{\mathrm{BAT}} - V_{\mathrm{SD,M13}}) \quad (20)$$

$$C_{\mathrm{fly}} = \frac{I_{\mathrm{LOAD,MAX}}}{f_{\mathrm{CLK}} \Delta V_{C_{\mathrm{fly}},\mathrm{MAX}}} \quad (21)$$

where the $V_{\mathrm{SD,M12}}$ and $V_{\mathrm{SD,M13}}$ are the different source-drain voltage levels of the power MOSFETs M_{12} and M_{13}, respectively. Owning to the limitation of maximum voltage across the flying capacitor, the output resistances of the transistors M_{14} and M_{24} in saturation region are almost constant and relatively large. Therefore, the location of the output pole will be dominated by the load resistance. The stability of the system is easy to be guaranteed. A small signal model in Fig. 11 is used to examine the current mode control methodology in the asymmetric dual-phase charge pump regulator. Using the state-space averaging analysis technique [19], the averaged state-space equation set can be derived:

$$\dot{x}_{\mathrm{av}} = A_{\mathrm{av}} x_{\mathrm{av}} + B_{\mathrm{av}} u \quad (22)$$

$$V_{\mathrm{OUT}} = C_{\mathrm{av}} x_{\mathrm{av}} + D_{\mathrm{av}} u \quad (23)$$

where

$$x_{\mathrm{av}} = [\, V_{\mathrm{C1}} \quad V_{\mathrm{C2}} \quad V_{\mathrm{C0}} \,]^{\mathrm{T}},$$

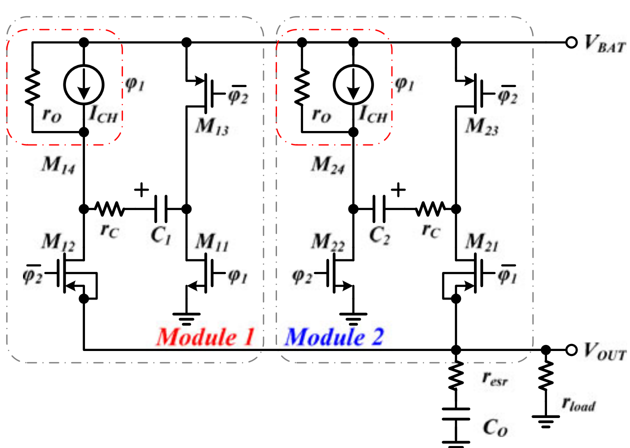


Fig. 11 The small signal mode of the asymmetric dual-phase charge pump regulator

$$u = [\, I_{\mathrm{CH}} \quad V_{\mathrm{BAT}} \,]^{\mathrm{T}},$$

$$R_1 = r_{\mathrm{O}} + r_{\mathrm{on}} + r_{\mathrm{C}},$$

$$R_2 = 2r_{\mathrm{on}} + r_{\mathrm{C}},$$

$$\beta_1 = (r_{\mathrm{esr}} + r_{\mathrm{load}})(r_{\mathrm{O}} + r_{\mathrm{on}} + r_{\mathrm{C}}) + r_{\mathrm{esr}} r_{\mathrm{load}},$$

$$\beta_2 = (r_{\mathrm{esr}} + r_{\mathrm{load}})(2r_{\mathrm{on}} + r_{\mathrm{C}}) + r_{\mathrm{esr}} r_{\mathrm{load}},$$

$$A_{\mathrm{av}} = \begin{bmatrix} \frac{-\beta_2 - (r_{\mathrm{esr}} + r_{\mathrm{load}}) R_1}{2\beta_2 R_1 C_1} & 0 & \frac{r_{\mathrm{load}}}{2\beta_2 C_1} \\ 0 & \frac{-\beta_1 - (r_{\mathrm{esr}} + r_{\mathrm{load}}) R_2}{2\beta_1 R_2 C_2} & \frac{r_{\mathrm{load}}}{2\beta_1 C_2} \\ \frac{r_{\mathrm{load}}}{2\beta_2 C_{\mathrm{O}}} & \frac{r_{\mathrm{load}}}{2\beta_1 C_O} & \frac{-(R_1 + r_{\mathrm{load}})\beta_2 - (R_2 + r_{\mathrm{load}})\beta_1}{2\beta_1 \beta_2 C_{\mathrm{O}}} \end{bmatrix},$$

$$B_{\mathrm{av}} = \begin{bmatrix} \frac{r_{\mathrm{O}}}{2R_1 C_1} & \frac{\beta_2 - R_1 (r_{\mathrm{esr}} + r_{\mathrm{load}})}{2R_1 \beta_2 C_1} \\ \frac{-r_{\mathrm{O}} (r_{\mathrm{esr}} + r_{\mathrm{load}})}{2\beta_1 C_2} & \frac{\beta_1 - R_2 (r_{\mathrm{esr}} + r_{\mathrm{load}})}{2R_2 \beta_1 C_2} \\ \frac{r_{\mathrm{O}} + r_{\mathrm{load}}}{2\beta_1 C_{\mathrm{O}}} & \frac{\beta_1 r_{\mathrm{load}} + \beta_2 r_{\mathrm{load}}}{2\beta_1 \beta_2 C_{\mathrm{O}}} \end{bmatrix},$$

$$C_{\mathrm{av}} = \begin{bmatrix} \frac{r_{\mathrm{esr}} r_{\mathrm{load}}}{2\beta_2} & \frac{r_{\mathrm{esr}} r_{\mathrm{load}}}{2\beta_1} & \frac{\beta_2 R_1 r_{\mathrm{load}} + \beta_1 R_2 r_{\mathrm{load}}}{2\beta_1 \beta_2} \end{bmatrix},$$

$$D_{\mathrm{av}} = \begin{bmatrix} \frac{r_{\mathrm{O}} r_{\mathrm{esr}} r_{\mathrm{load}}}{2\beta_1} & \frac{\beta_1 r_{\mathrm{esr}} r_{\mathrm{load}} + \beta_2 r_{\mathrm{esr}} r_{\mathrm{load}}}{2\beta_1 \beta_2} \end{bmatrix}$$

In order to obtain the static characteristic, let $\dot{x}_{\mathrm{av}} = 0$. Then, the value of V_{OUT} can be obtained:

$$V_{\mathrm{OUT}} = \left[C_{\mathrm{av}} \frac{-B_{\mathrm{av}}}{A_{\mathrm{av}}} + D_{\mathrm{av}} \right] u \approx r_{\mathrm{load}} I_{\mathrm{CH}} \quad (24)$$

The small signal transfer function T_{QP} can be expressed as (25), where I is unity matrix.

$$\frac{v_{OUT}(s)}{v_{REG}(s)} = \left[C_{av} \frac{B_{av}}{sI - A_{av}} + D_{av} \right] [1 \quad 0] \quad (25)$$

Since the asymmetric structures are used to synchronize the regulating phase ϕ_1 of the SCVR circuit, the state-space equation and the transfer function cannot be simplified. In order to check the frequency response of the current mode control methodology, the equation is calculated by the software of Matlab. According to the maximum and minimum load current, the range of load resistance R_{LOAD} is set from 100 Ω to 100 kΩ, the values of the flying capacitors C_{fly1} and C_{fly2} are 1 μF, and that of the output capacitor C_{OUT} is 10 μF. The Bode plot of the power stage is illustrated in Fig. 12. Obviously, the proposed power stage sets the location of the output pole in a narrow range effectively. Figure 13 shows the simulation result of load transient at V_{BAT} = 3 V during the load current is set between 1 mA and 50 mA. Figure 14 shows the comparison of output ripple in single and dual-phases charge pump regulator. The simulation result shows the ripple voltage of the dual-phase charge pump regulator has smaller output ripple than that of single-phase charge pump regulator. The output ripples are reduced to half those in single-phase design.

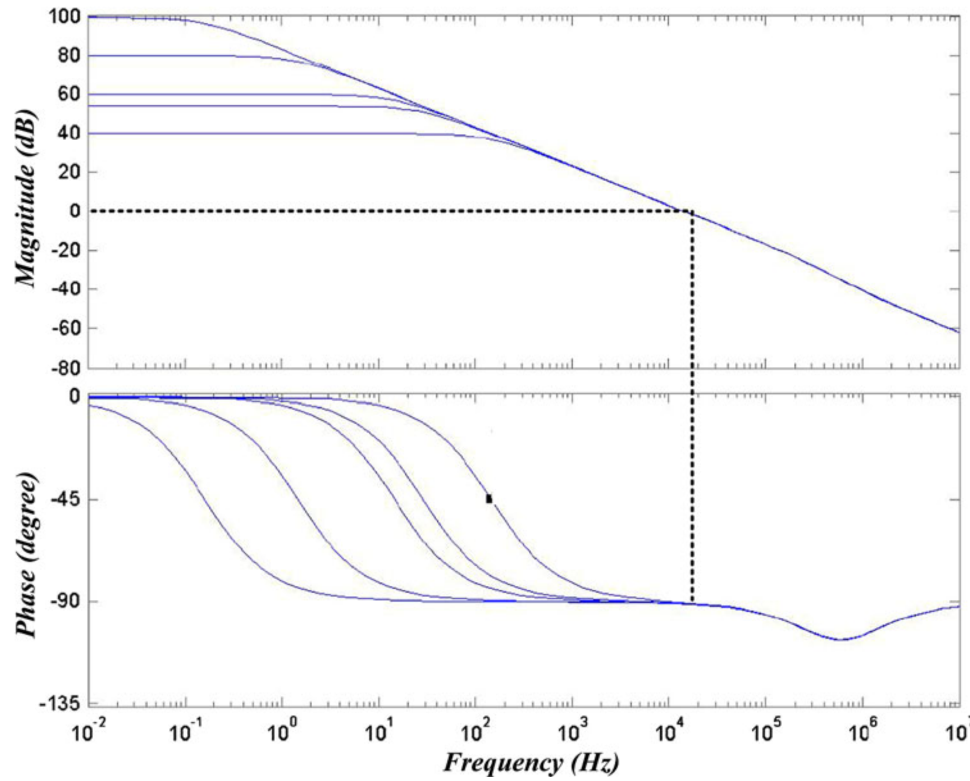


Fig. 12 Frequency response when the circuit forces the transistor in saturation region

3.4 The automatic body switch circuit

In order to avoid leakage current and potential latch-up of P-MOSFET, the ABS circuit as illustrated in Fig. 15 is necessary. The common-gate comparator is presented. The common-gate input stage is used to ensure the wide bandwidth for the characteristic of fast response and the simple current mirror is used to achieve low power consumption owing to limited I_B. Transistors M_4 and M_7 constitute the input pair that is used to detect the drain and source voltage of P-MOSFET. When the value of V_{OUT} is larger than that of V_{BAT}, the output V_O of common-gate comparator is changed from low to high. After the conversion of level shifter, the transistors M_{OUT1} and M_{OUT2} are turned on and the V_{OUT} is connected to HV_{DD} and HV_{CLK}.

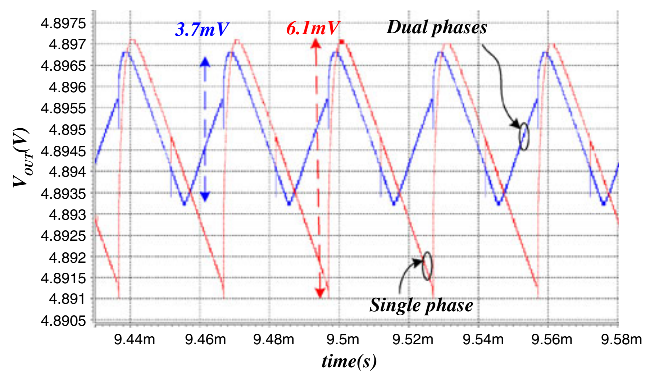


Fig. 14 The comparison of output ripples in single- and dual-phase charge pump regulator

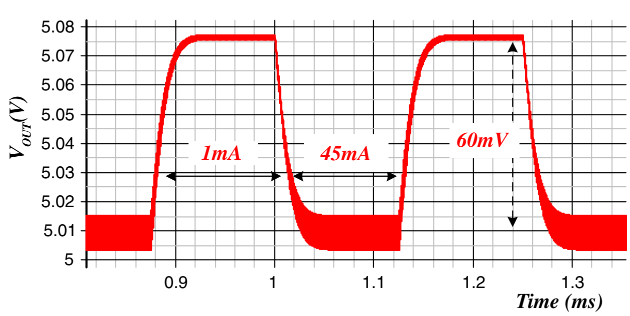


Fig. 13 The load transient at $V_{BAT} = 3$ V during the load current varies from 1 to 45 mA or vice versa

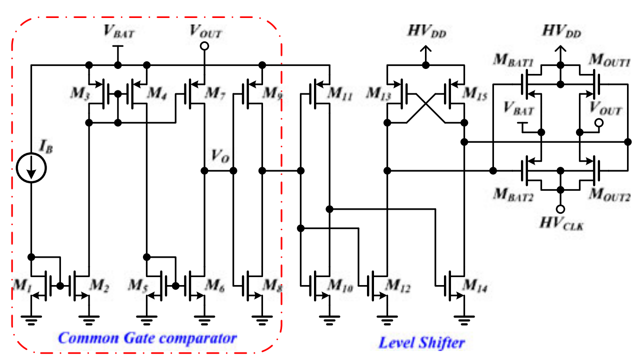


Fig. 15 The schematic of the ABS circuit

Contrarily, when the value of V_{OUT} is smaller than that of V_{BAT}, the HV_{DD} and HV_{CLK} are switched to connect to V_{BAT}. The experimental results in Fig. 16 not only demonstrate the power dissipation is smaller than that of the previous design [3] about 54% after the test of triangular and square waveforms, but also shows the fast response characteristic when V_{BAT} is close to V_{OUT}. There are two output nodes, HV_{DD} and HV_{CLK}, in this circuit. HV_{DD} supplies the power MOSFETs and HV_{CLK} supplies the driver circuit. The bulk terminals of the power MOSFETs are connected to the highest potential HV_{DD} in the chip to eliminate the reverse current. But the large source-bulk voltage will increase the threshold voltage of the power MOSFETs M_{14} and M_{24} because of the body effect. Figure 10 shows the additional bulk bias circuit at the power stage. The bulk terminals of transistors M_{14} and M_{24} are biased to their source terminals when M_{14} and M_{24} are turned on. Therefore, small size power MOSFETs have the same on-resistance due to the small V_{TH}. When M_{14} and M_{24} are turned off, their bulk terminals are biased to HV_{DD} to eliminate the reversed current.

4 Experimental results

The proposed dual-phase charge-pump circuit was fabricated in TSMC double-poly quadruple-metal 0.35-μm CMOS technology. The threshold voltages of n-MOSFET and p-MOSFET are 0.55 and 0.65 V, respectively. The chip micrograph is shown in Fig. 17 and the total silicon area is about 1820 * 1480 μm^2, including the testing pads. The dual-phase charge-pump circuit can operate from 2.9 to 4.9 V with a regulated output voltage of 5 V. The summary and the comparison of the performance are shown in Table 1.

Figure 18 shows the regulated output voltage. The waveforms of the two terminals of the charge-pump capacitor demonstrate the correctness of the proposed circuit. Owing to the large parasitic resistance, the regulated output voltage is about 5.0 V. Figure 19 shows the performance of load transient response when load current changes from 1 to 45 mA or vice versa. The output ripple is smaller than 10 $mV_{P\text{-}P}$, which is effectively reduced by the proposed dual-phase charge-pump circuit. The measured output ripple of the charge pump with voltage mode control methodology is about 70 $mV_{P\text{-}P}$. Thus, the output ripple of dual-phase charge pump is greatly smaller than that of the voltage mode charge pump. The response time is about 15 μs which is smoothly rising and falling to related regulated output voltage. It means that the phase margin is enough during the transient of load condition since the current mode control methodology is applied to the proposed dual-phase charge

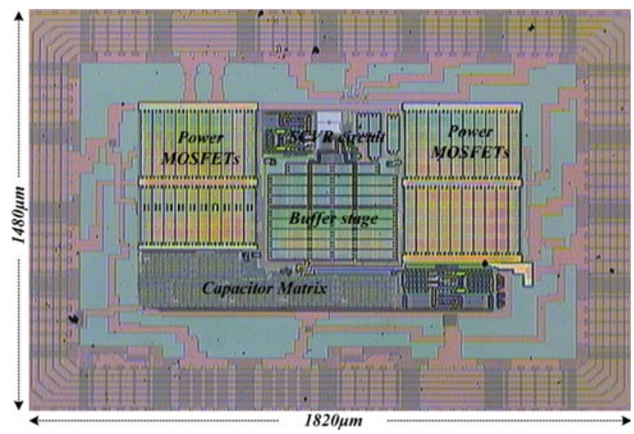
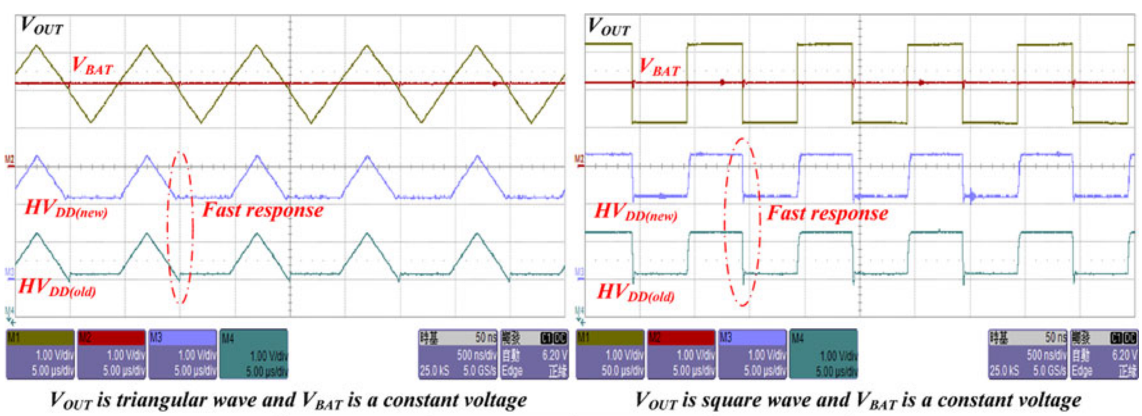


Fig. 17 The chip micrograph and the chip size is 1820 * 1480 μm^2



Input signal	Ma et al. 2007	This work	Reduction (%)
Triangular wave	54.36uW	25uW	54%
Square wave	56.33uW	24uW	54.39%

Fig. 16 The experimental results demonstrate the low power and high accuracy characteristics of the ABS circuit

Table 1 Summary of the performance

Specification	Proposed	[3]	[8]	[14]
Process	TSMC 0.35 μm CMOS	AMS 0.6 μm CMOS	3.3 V 0.13 μm CMOS	0.5 μm CMOS (2 poly)
Pumping capacitor	1 μF	1 μF		1 μF
Output capacitor	2.2 μF	2.2 μF	2 μF	10 μF
Switching frequency	2 MHz	0.5 MHz	0.4–0.6 MHz	90 kHz
Input voltage	2.9–4.9 V	1.5–2.5 V	3.3 V	1.8–3.5 V
Output voltage	5 V	3–5 V	4.5–5 V	3.3 V
Maximum I_{OUT}	48 mA	50 mA	30 mA	20 mA
Ripple ($V_{IN} = 3$ V)	30 mV/45 mA 10 mV/1 mA	56 mV/50 mA	33.8 mV/30 mA	57 mV/20 mA
Load regulation	1.7 mV/mA	–	–	9.3 mV/mA
Line regulation	9.3 mV/V	–	–	11 mV/V
Temperature drift	17.8 ppm/°C	–	–	–

pump. Furthermore, the over-shoot and under-shoot voltages in the proposed charge pump disappear during load transient compared to the load transient in voltage mode charge pump. The drop voltage is about 70 mV due to the large parasitic resistance of the bonding and PCB wires. In Fig. 20(a), it demonstrates the driving capability of the proposed circuit is about 48 mA. When the load current is higher than 48 mA, the output voltage is drastically decreased due to the unregulated results. When the load current is smaller than 48 mA, the efficiency is decreased and proportional to the increase of the input voltage, which is described by the charge-pump theory. The efficiency chart versus different supply voltage is shown in Fig. 20(b).

5 Conclusions

A dual-phase charge-pump circuit by means of the SCVR and the current mode control methodology is presented in this paper. The size of the regulated block in this structure is very small and the most area on silicon is the power device. It helps the design of the minimum size and low cost application. The low output ripple and high system stability of the dual-phase charge pump regulator are demonstrated by the test chip, which was fabricated by TSMC 0.35 μm 3.3/5 V 2P4 M CMOS technology. Owing to design of the buffer stage in current mode control methodology, the system can have better bandwidth and phase margin.

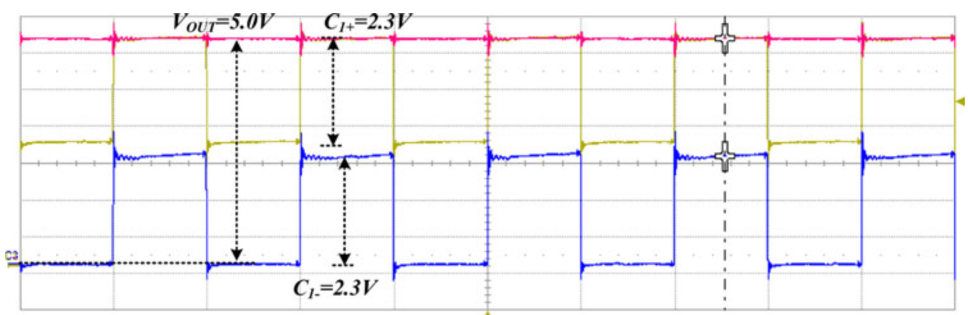


Fig. 18 The measured waveforms of V_{OUT} and the two terminals of the charge-pump capacitor when $V_{BAT} = 3$ V and $I_{OUT} = 20$ mA

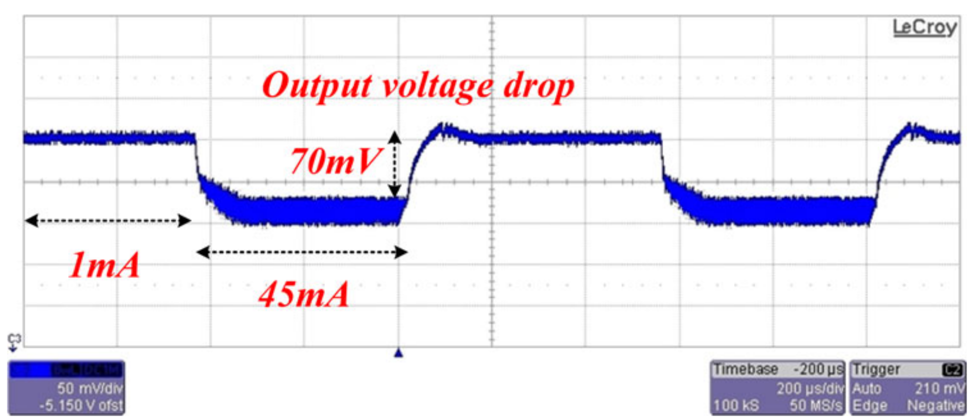
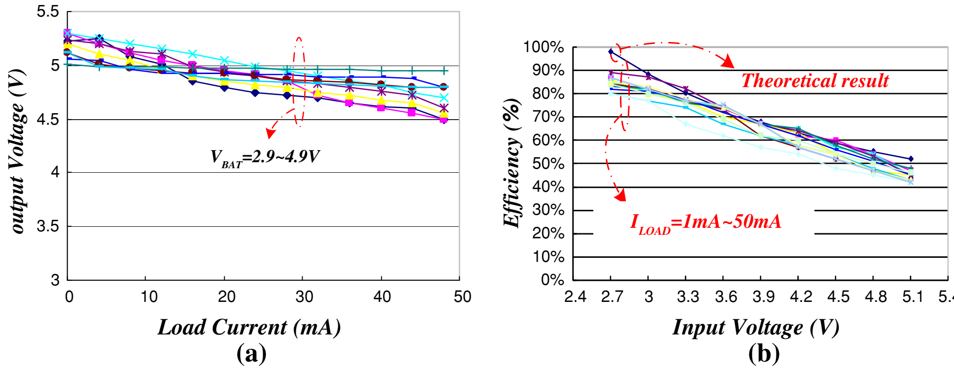


Fig. 19 The load transient waveform when $V_{BAT} = 3.0$ V and I_{LOAD} change from 1 to 45 mA, or vice versa

Fig. 20 The experimental result in different supply voltages and load conditions. **a** The output voltage versus load current at different supply voltage from $V_{BAT} = 2.9$ to 4.9 V and **b** the efficiency versus input voltage with different load current from $I_{LOAD} = 1$ to 50 mA



Therefore, the transient response and driving capability can be improved. Besides, only one closed-loop regulation is utilized to generate the dual-phase charge pump regulator in order to improve the power conversion efficiency. Besides, the proposed ABS circuit can efficiently drive the bulk of the power p-type MOSFETs to avoid leakage and potential latch-up. The input voltage range varies from 2.9 to 4.9 V and the output voltage is regulated at 5 V. Experimental results demonstrate this charge pump can provide 48 mA maximum load current without any oscillation problems.

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References

1. Simunic, T. (Ed.). (2002). Dynamic management of power consumption. In *Power aware computing* (pp. 101–125). Norwell, MA: Kluwer Academic Publishers.
2. Bedeschi, F., Boffino, C., Bonizzoni, E., Khouri, O., Pollaccia, G., Restal, C., & Torelli, G. (2006). A low-ripple voltage tripler. In *IEEE international symposium on circuits and systems (ISCAS)*, pp. 2753–2756.
3. Lee, H., & Mok, P. K. T. (2005). Switching noise and shoot-through current reduction techniques for switched-capacitor voltage doubler. *IEEE Journal of Solid-State Circuits, 40*, 1136–1146. doi:10.1109/JSSC.2005.845978.
4. Ying, T. R., Ki, W.-H., & Chan, M. (2003). Area-efficient CMOS charge pumps for LCD drivers. *IEEE Journal of Solid-State Circuits, 38*, 1721–1725. doi:10.1109/JSSC.2003.817596.
5. Min, K.-S., Kim, Y.-H., Ahn, J.-H., Chung, J.-Y., & Sakurai, T. (2002). CMOS charge pumps using cross-coupled charge transfer switches with improved voltage pumping gain and low gate-oxide stress for low-voltage memory circuits. In *IEEE international symposium on circuits and systems (ISCAS)*, Vol. 5, pp. 545–548.
6. Starzyk, J. A., Jan, Y.-W., & Qiu, F. (2001). A DC–DC charge pump design based on voltage doublers. *IEEE Transactions on Circuits and Systems I, 48*, 350–359. doi:10.1109/81.915390.
7. Wang, C.-C., & Wu, J.-C. (1997). Efficiency improvement in charge pump circuits. *IEEE Journal of Solid-State Circuits, 32*, 852–860. doi:10.1109/4.585287.
8. Lee, J.-Y., Kim, S.-E., Song, S.-J., Kim, J.-K. Kim, S., & Yoo, H.-J. (2006). A regulated charge pump with small ripple voltage and fast start-up. *IEEE Journal of Solid-State Circuits, 41*, 425–432. doi:10.1109/JSSC.2005.862340.
9. Bayer, E., & Schmeller, H. (2000). Charge pump with active cycle regulation-closing the gap between linear and skip modes. In *IEEE 31st annual power electronics specialists conference (APEC)*, Vol. 3, pp. 1497–1502.
10. Thiele, G., & Bayer, E. (2004). Current mode charge pump: Topology, modelling and control. In *IEEE 35th annual power electronics specialists conference (APEC)*, Vol. 5, pp. 3812–3817.
11. Gregoire, B. R. (2006). A compact switched-capacitor regulated charge pump power supply. *IEEE Journal of Solid-State Circuits, 41*, 1944–1953. doi:10.1109/JSSC.2006.875303.
12. Widlar, R. J. (1971). New developments in IC voltage regulators. *IEEE Journal of Solid-State Circuits, 6*, 2–7. doi:10.1109/JSSC.1971.1050151.
13. Kuijk, K. E. (1973). A precision reference voltage source. *IEEE Journal of Solid-State Circuits, 8*, 222–226. doi:10.1109/JSSC.1973.1050378.
14. Hsieh, C.-Y., Fan, P.-C., & Chen, K.-H. (2007). A dual phase charge pump with compact size. In *The 14th IEEE international conference on electronics, circuits and systems (ICECS)*, pp. 202–205.
15. Somasundaram, M. N., & Ma, D. (2006). Integrated low-ripple-voltage fast-response switched-capacitor power converter with interleaving regulation scheme. In *IEEE international symposium on circuits and systems (ISCAS)*, pp. 3129–3132.
16. Cabrini, A., Gobbi, L., & Torelli, G. (2005). A theoretical discussion on performance limits of CMOS charge pumps. In *Proceedings of the 2005 European conference on circuit theory and design*, Vol. 2, pp. II/35–II/38.
17. Cabrini, A., Fantini, A., & Torelli, G. (2006). High-efficiency regulator for on-chip charge pump voltage elevators. *Electronics Letters, 42*, 972–973. doi:10.1049/el:20061165.
18. Boffino, C., Cabrini, A., Khouri, O., & Torelli, G. (2005). High-efficiency control structure for CMOS flash memory charge pumps. In *IEEE international symposium on circuits and systems*, Vol. 1, pp. 121–124.
19. Chung, H., & Mok, Y. K. (1999). Development of a switched-capacitor DC/DC boost converter with continuous input current waveform. *IEEE Transactions on Circuits and Systems I, 46*, 756–759. doi:10.1109/81.768834.

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