Organic Electronics 9 (2008) 925–929

Contents lists available at ScienceDirect

Organic Electronics

journal homepage: www.elsevier.com/locate/orgel

Letter

Low-operating-voltage polymeric transistor with solution-processed low-*k* polymer/high-*k* metal-oxide bilayer insulators

Feng-Yu Yang [a,*], Kuo-Jui Chang [b], Meei-Yu Hsu [a], Cheng-Chin Liu [b]

[a] Materials and Chemical Research Laboratories, Industrial Technology Research Institute, Hsinchu 310, Taiwan
[b] Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 310, Taiwan

ARTICLE INFO

Article history:
Received 15 January 2008
Received in revised form 16 May 2008
Accepted 1 June 2008
Available online 18 June 2008

PACS:
81.07.Pr
85.30.Tv

Keywords:
Nanoparticle
Dielectric
Organic
Field-effect transistor

ABSTRACT

We have successfully demonstrated a polymeric semiconductor-based transistor with low-*k* polymer/high-*k* metal-oxide (TiO_2) bilayer as gate dielectric. The TiO_2 layers are readily processable from solution and cured at low temperature, instead of traditionally sputtering or high temperature sintering process, thus may suitable for a low-cost organic field effect transistors (FETs) manufacture. The low-*k* polymer capped on TiO_2 layer could further smooth the TiO_2 dielectric surface and suppress the leakage current from grain boundary of TiO_2 films. The resulting unpatented P3HT-OFETs could operate with supply voltage less than 10 V and the mobility and threshold voltage were 0.0140 cm^2/V s and 1.14 V, respectively. The on/off ratio was 1.0×10^3.

In the past decade, organic field-effect transistors (OFETs) have become of great interest for many attractive applications, such as radio-frequency identification tags, smart cards, flat panel displays, and chemical vapor sensors [1–4]. However, traditional OFETs were operated at high voltage (usually exceed 20 V) to output a high current, while in a typical low-end application, the available operating voltage will be very low. Since the field-induced current is proportional to the density of accumulated charge in the OFETs channel, it has been suggested that the use of high capacitance gate dielectrics will allow the necessary charge to accumulate at low voltage [5,6]. The production of low-operating-voltage OFETs with high capacitance gate dielectrics has already been reported by using ultrathin gate dielectric [7–10] or high-dielectric constant (high-*k*) inorganic metal-oxide gate dielectrics [11–15]. For example, Halik et al. [10] reported the pentacene-based FETs with self-assembled monolayer (SAM) as ultrathin gate dielectric, which operating at 2 V, with a field-effect mobility of 1 cm^2/V s. This approach shows promise, however, pathways for devices integration into large-volume coating process are less obvious. Alternatively, the high-*k* metal-oxide films, such as Al_2O_3, Ta_2O_5, and TiO_2, were usually deposited either by sputtering or by high temperature sintering process. Although low-voltage, high performance OFETs fabricated with pentacene using metal-oxide as gate insulators [11,14,15] have been demonstrated, the thermal deposition of pentacene and the sputtering process of metal-oxide were still not consistent with low-cost OFETs manufacture due to the requirement for expensive vacuum steps. Relatively little has been done with polymeric semiconductor with high-*k* metal-oxide as gate dielectric in OFETs [12,13]. Therefore, in order to fully enjoy the advantages of OFETs, namely, low-cost feature for large-area electronics, it is important to develop

* Corresponding author. Tel.: +886 3 5912643; fax: +886 3 5827694.
E-mail address: FengYuYang@itri.org.tw (F.-Y. Yang).

1566-1199/$ - see front matter © 2008 Elsevier B.V. All rights reserved.
doi:10.1016/j.orgel.2008.06.002

devices with polymeric semiconductor as well as high capacitance dielectrics which were all processed by solution method and cured at low temperature.

In this work, we have initially prepared soluble TiO_2 nano-particles as high-k gate dielectric on substrate at low temperature to enhance the capacitance of OFETs. For a high performance OFETs, generally, a low-k polymer at the insulator/semiconductor interface is desirable, as low interface polarity has been shown to increase carrier mobility [16,17]. In addition, the polymer could further smooth the TiO_2 dielectric surface and suppress the leakage current from grain boundary of TiO_2 films. Accordingly, a layer of the low-k polymer was spin-coated on top of the TiO_2 nano-particles film and a stacked structure (bilayer) of low-k/high-k dielectrics was fabricated in this study. With regioregular poly(3-hexylthiophene) (RR-P3HT) as active semiconductor, good FET characteristics were obtained at low drive voltage.

The polymer FETs were fabricated on N++ type low-resistance Si wafers as substrate and acts as a common gate electrode. An oleic acid surface-modified TiO_2 nanoparticles (TiO_2-oleic) with high solublility in chlorobenzene or toluene was solution-deposited on wafer as high-k gate dielectrics. This TiO_2-oleic was synthesized and modified from literatures [18]. The TiO_2-oleic were reported as anatase phase ($k = 31$) and were cylindrical in shape (20 nm in length and 4 nm wide, measured by transmission electron Microscopy (TEM), Fig. 1a). The high-k TiO_2-oleic layers were obtained by spin-coating of TiO_2-oleic solution (10 wt% in Cl–benzene) at 1000 rpm for 30 s, followed by a baking process at 120 °C in oven for 0.5hr. Subsequently, another layer of the cross-linking PVP ($k = 4.1$) was applied on TiO_2-oleic film to smoother the interface and as the low-k materials. The uniformity of the TiO_2-oleic film was examined by using scanning electron microscopy (SEM) imaging of fracture edge. As shown in Fig. 1b, the TiO_2 layer by solution process exhibit uniform film with homogeneous nano-particle dispersions, suggesting a good candidate for high-k insulator for OFETs devices.

The transistors with bilayer dielectric films with different thickness were fabricated (transisor 2: TiO_2-oleic (317 nm)/PVP (317 nm); transisor 4: TiO_2-oleic (317 nm)/PVP (85 nm)). The cross-linked PVP material (the top layer of bilayer dielectric) shows good dielectric performance and chemical resistance to many solvents and bases which typically found in positive photoresist developers, indicating that the cross-linked PVP in this study were suitable for use in photolithography and wet etching process. Hence, we defined the region of electrodes with channel width/length = 1000 um/10 um on top of the PVP layer by photolithography/Pt-deposition (20 nm)/lift-off process (acetone), leading to a patterned source and drain electrode with fine accuracy and the surface of underlying PVP films remain intact. Before spin-deposition of P3HT, the PVP films were further treated with octyltrichlorosilane (OTS) or hexamethyldisilazane (HMDS) as a SAM modification layer [19]. After spin-coating of the P3HT (3 mg/1 mL in toluene, 500 rpm, 60 s) as semiconductor, a bottom gate, bottom contact configuration of the unpatterned P3HT-OFETs was fabricated and shown in Fig. 2. All current–voltage (I–V) measurements for our OFETs were performed

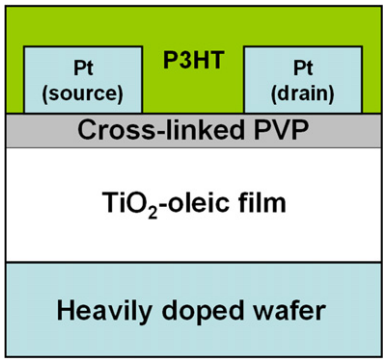

Fig. 2. Devices structure of bottom gate, bottom contact configuration OFETs in this study.

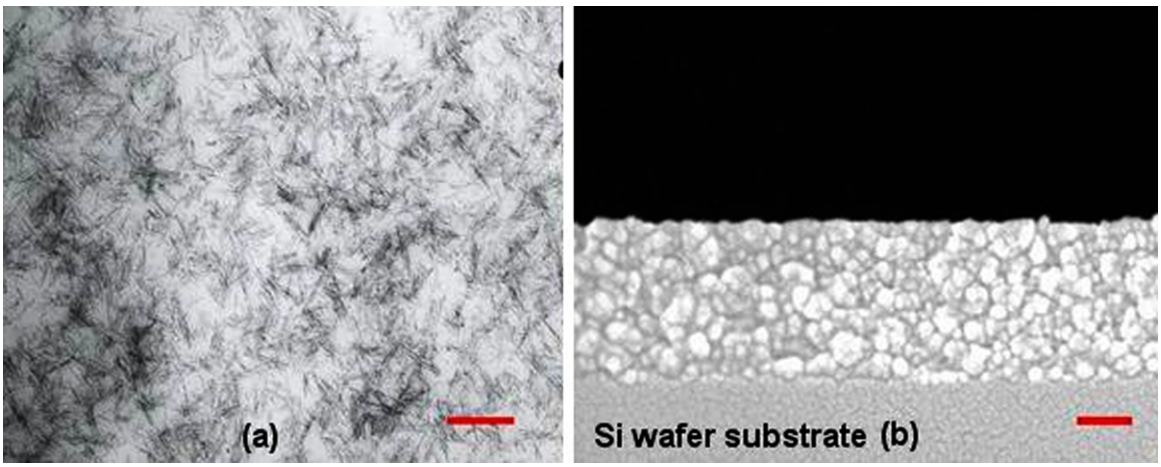

Fig. 1. (a) TEM image of TiO_2-oleic nano-particle (b) cross-sectional SEM image of TiO_2-oleic layer. All scale bars are 100 nm.

Table 1
Summary of dielectric properties (100 kHz) and field effect transistor data

Sample	Condition	Oleic-TiO_2 (nm)	PVP (nm)	C_{ox} (nF/cm^2)	u cm^2/V s	On/off ratio	Ss V/dec	V_t (V)
Transistor 1	Operated at V_{ds} −40 V	–	580 (OTS-treated)	6.3	0.0074	7.90×10^3	5.50	−4.46
Transistor 2		317	317 (OTS-treated)	10.0	0.0260	2.96×10^3	2.60	−6.33
Transistor 3		317	317 (HMDS-treated)	10.0	0.0028	1.90×10^3	4.26	1.54
Transistor 2	Operated at V_{ds} −10 V	317	317(OTS-treated)	10.0	0.0072	5.40×10^2	1.44	1.26
Transistor 4		317	85 (OTS-treated)	28.0	0.0140	1.00×10^3	1.89	1.14

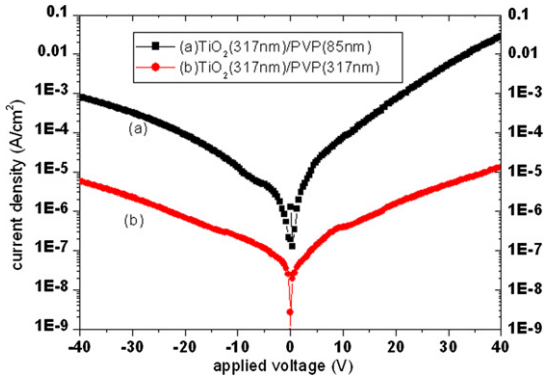

Fig. 3. Leakage currents of the bilayer film: (a) (TiO_2-oleic (317 nm)/PVP (85 nm)) and (b) (TiO_2-oleic (317 nm)/PVP (317 nm)).

with semiconductor parameter analyzer (4156 C, Agilent) at room temperature in air. To characterize leakage currents and capacitances of TiO_2-oleic/PVP films, we have made a capacitor structure (MIM) by sandwiching the bilayer materials between indium tin oxide (ITO) and Au electrode. The effective gate capacitances (C_{ox}) were measured by capacitance analyzer (590 CV, Keithley) at 100 k MHz and listed in Table 1. We found that transisor 2 and transisor 4 exhibit the capacitances of 10 nF/cm^2 and 28 nF/cm^2, respectively, which are close to the theoretical values for serially connected capacitor layers.

The current-density–voltage (J–V) characteristics of these MIM structures (ITO/TiO_2-oleic (317 nm)/PVP (317 nm)/Au and ITO/TiO_2-oleic (317 nm)/PVP (85 nm)/Au) were investigated and shown in Fig. 3. With a thicker capped layer of cross-linked PVP, the TiO_2-oleic (317 nm)/PVP (317 nm) have lower current densities (10^{-5} A/cm^2 at 40 V) than that

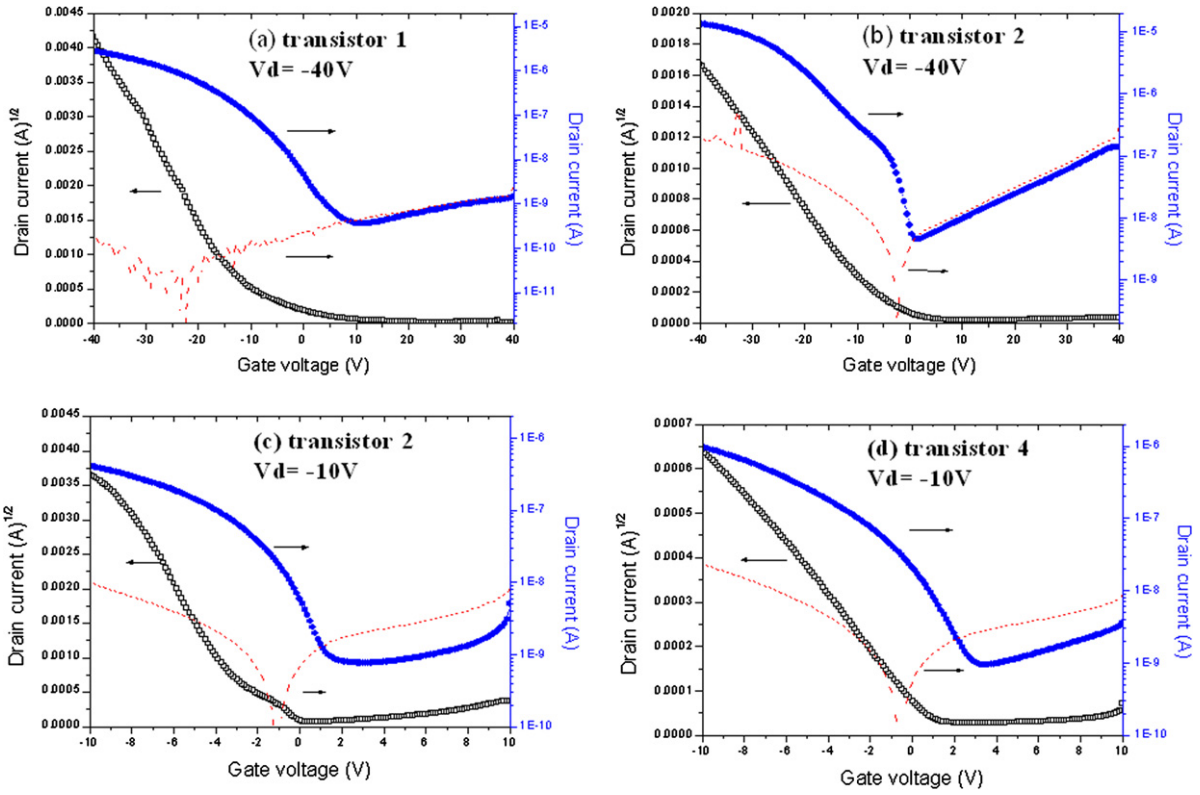

Fig. 4. Transfer characteristics (solid line) and the leakage current (dashed line) of (a) transistor 1 (insulator: PVP (580 nm)) with V_d = −40 V (b) transistor 2 (insulator: TiO_2-oleic (317 nm)/PVP (317 nm)) with V_d = −40 V (c) transistor 2 with V_d = −10 V (d) transistor 4 (insulator: TiO_2-oleic (317 nm)/PVP (85 nm)) with V_d = −10 V.

of TiO_2-oleic (317 nm)/PVP (85 nm) (10^{-3} A/cm^2 at 40 V) by two orders of magnitude. Although the current density of 10^{-3} A/cm^2 (at 40 V) is high, the TiO_2-oleic (317 nm)/PVP (85 nm) film have an acceptable current density of 10^{-5} A/cm^2 (at 10 V), a value good enough for a gate insulator for OFETs operation within 10 V. It should be noted that the bilayer dielectric structure is necessary in this study because the MIM structure of ITO/TiO_2-oleic (317 nm)/Au show high leakage current, thus not able to be an insulator solely in this study.

The surface roughness of the dielectric layers was characterized by an atomic force microscope ((AFM) Nanoscope IIIa, digital Instruments). The root-mean-square (rms) roughness of the TiO_2-oleic film on silicon wafer is 1.72 nm. When top-coating layer (PVP) was applied on TiO_2-oleic film, the rms was further reduced to 0.61 nm which was close to that of SiO_2 surface on Si substrate.

All of the electrical parameters of the OFETs in this study were listed in table 1. The devices of transistor 1, 2, and 3 were operated at V_{ds} = −40 V, V_{gs} = 40 V to −40 V. In addition, for low voltage operating, the electric properties of transistor 2 and transistor 4 were measured within 10 V. The carrier mobility u and the threshold voltage V_t were determined by using the following Eq. (1):

$$\sqrt{I_{D,SAT}} = \sqrt{\frac{W\mu C_{OX}}{2L}}(V_G - V_t) \quad (1)$$

Where $I_{D,SAT}$ is the saturated drain current, C_{ox} is the gate capacitance per unit area, W and L are the conducting channel width and length, V_G denotes the gate applied voltage. The mobility was extracted from the slope of the linear plots of the square root of the drain current versus the gate voltage (Fig. 4).

All of the transfer characteristics of P3HT-OFETs in this study are shown in Fig. 4. As to the transistor 2 with OTS-treated insulator, the mobility in the saturation region and the threshold voltage were 0.0260 cm^2/V s and −6.33 V, respectively. The on/off ratio was about 2.96×10^3. This mobility and on/off ratio were similar to unpatterned P3HT-based OFETs with SiO_2 as gate dielectric [6]. For the HMDS-treated transistor 3, the mobility and the threshold voltage were 0.0028 cm^2/V s and 1.54 V, respectively, with on/off ratio 1.9×10^3. It is obviously that devices with OTS-treated insulator show better performance than HMDS one. Transistor 1 was the device with single layer of cross-linked PVP as gate dielectric. The mobility and the threshold voltage are 0.0074 cm^2/V s and −4.46 V, respectively, with on/off ratio 7.90×10^3. The mobility of transistor 1 was about 4 times lower than that of transistor 2.

To achieve high performance, low operating voltage OFETs, transistor 2 and transistor 4 were tested within 10 V (V_{ds} = −10 V, V_{gs} = 10 V to −10 V). The transfer characteristics are shown in Fig. 4c and d and output characteristics are shown in Fig. 5. The transistor 2 with capacitance of 10 nF/cm^2 exhibited mobility of 0.0072 cm^2/V s and the threshold voltage was 1.26 V. The on/off ratio was 5.4×10^2. On the other hand, the transistor 4 (capacitance of 28 nF/cm^2) had twice the field-induced current at the same gate voltage as shown in Fig. 5b. The mobility of transistor 4 was better than for transistor 2, namely, 0.0140 cm^2/V s and the threshold voltage was 1.14 V with on/off ratio 1.0×10^3. According to the work by Wang et al., [13] they demonstrated P3HT-OFETs with sputtered TiO_2 and bilayer SiO_2/TiO_2 as gate insulators which operate at 10 V and show mobility of 0.005 cm^2/V s and 0.032 cm^2/V s, respectively. Although transistors with lower mobility were obtained in our cases, this is the first example of polymeric semiconductor based FETs that were made by a simple, solution-processable TiO_2 gate dielectric which fabricate at low temperature.

We have also investigated the hysteresis of the P3HT-OFETs with bilayer TiO_2-oleic/PVP gate insulators. The gate-to-source voltage (V_{GS}) is continuously swept in steps of 0.12 V, starting from 10 V, passing through −10 V, and finally arriving at 10 V. The maximum difference of V_G for a constant current in the forward and reverse scans was designated as the amount of hysteresis (ΔV_{hys}) [20]. The polymer gate dielectric OFETs usually result in large hysteresis in the I–V characteristics. In our cases, the transistor 4 with thin PVP (85 nm) and the transistor 2 with thicker PVP (317 nm) both show the similar hysteresis behavior and the ΔV_{hys} is 4.10 V and 4.24 V, respectively, as shown in Fig. 6. The parameters of both the two OFETs include carrier mobility, subthreshold slope, and on/off ratio are unaffected by the hysteresis. It is believed that OFETs with

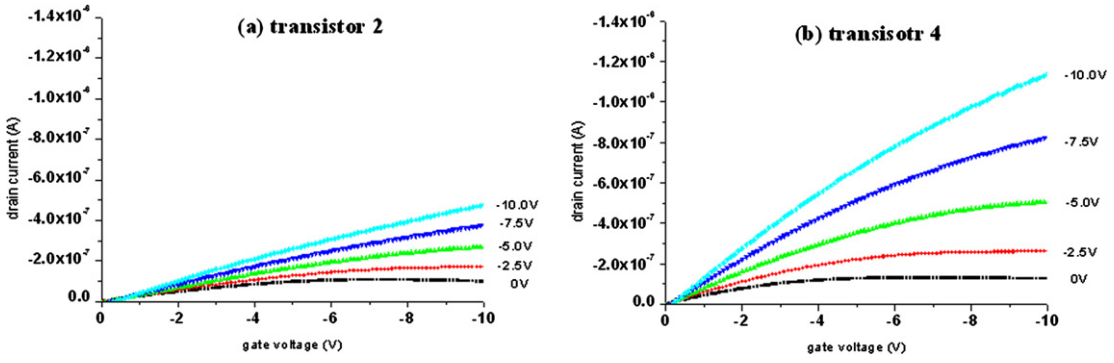

Fig. 5. ID-VG transfer curves of OFETs with bilayer dielectrics. (a) transistor 2 (TiO_2-oleic (317 nm)/PVP (317 nm)) and (b) transistor 4 (TiO_2-oleic (317 nm)/PVP (85 nm)).

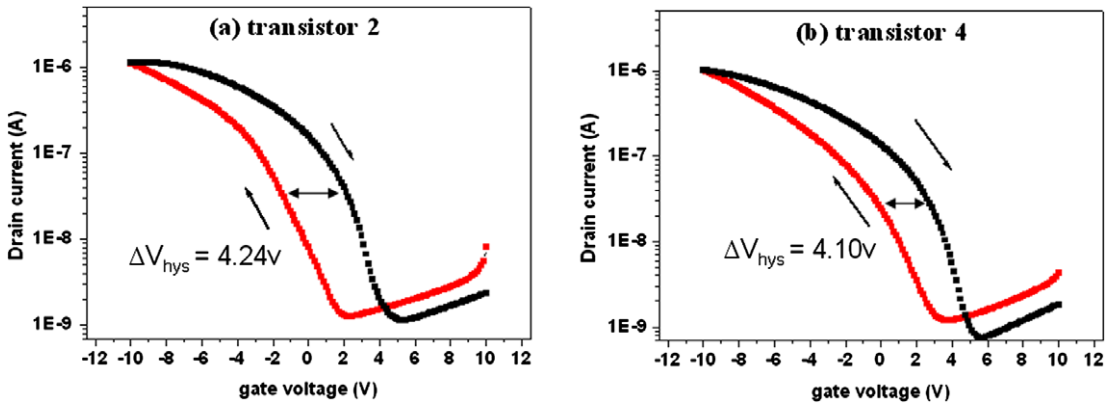

Fig. 6. The Hysteresis behavior of OFETs with bilayer dielectrics. (a) transistor 2 (TiO_2-oleic (317 nm)/PVP (317 nm)) and (b) transistor 4 (TiO_2-oleic (317 nm)/PVP (85 nm)).

hysteresis may arise from the migration of the negative ions in the PVP gate insulator and surface polarization [21,22].

In conclusion, we have successfully demonstrated a polymeric semiconductor-based transistor with low-*k* polymer/high-*k* metal-oxide (TiO_2) bilayer as gate dielectric. The metal-oxide (TiO_2) layers are readily processable from solution and cured at low temperature, instead of traditionally sputtering or high temperature sintering process, thus may suitable for a low-cost OFETs manufacture. The low-*k* polymer capped on TiO_2 layer could further smooth the TiO_2 dielectric surface and suppress the leakage current from grain boundary of TiO_2 films. The resulting unpatented P3HT-OFETs could operate with supply voltage less than 10 V and the mobility and threshold voltage were 0.0140 cm^2/V s and 1.14 V, respectively. The on/off ratio was 1.0×10^3.

References

[1] H. Sirringhaus, T. Kawase, R.H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, E.P. Woo, Science 290 (2000) 2123.
[2] L.-L. Chua, J. Zaumseil, J.-F. Chang, E.C.W. Ou, P.K.H. Ho, H. Sirringhaus, R.h. Friend, Nature 434 (2005) 194.
[3] B. Crone, A. Dodabalapur, Y.-Y. Lin, R.W. Filas, Z. Bao, A. LaDuca, R. Sarpeshkar, H.E. Katz, W. Li, Nature 403 (2000) 521.
[4] J.H. Burroughes, D.D.C. Bradley, A.R. Brown, R.N. Marks, K. Mackay, R.H. Friend, P.L. Burns, A.B. Holmes, Nature 347 (1990) 539.
[5] L. Herlogsson, X. Crispin, N.D. Robinson, M. Sandberg, O.-J. Hagel, G. Gustafsson, M. Berggren, Adv. Mater. 19 (2007) 97.
[6] A. Facchetti, M.H. Yoon, T.J. Marks, Adv. Mater. 17 (2005) 1705.
[7] L.L. Chua, P.K.H. Ho, H. Sirringhaus, R.H. Friend, Appl. Phys. Lett. 84 (2004) 3400.
[8] M.H. Yoon, H. Yan, A. Facchetti, T.J. Marks, J. Am. Chem. Soc. 127 (2005) 10388.
[9] S.Y. yang, S.H. Kim, K. Shin, H. Jeon, C.F. Park, Appl. Phys. Lett. 88 (2006) 173507.
[10] M. Halik, H. Klauk, U. Zschieschang, G. Schmid, C. Dehm, M. Schutz, S. Maisch, F. Effenberger, M. Brunnbauer, F. Stellacci, Nature 431 (2004) 963.
[11] C.D. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, J.M. Shaw, Science 283 (1999) 822.
[12] L.A. Majewski, R. Schroeder, M. Grell, Adv. Funct. Mater. 15 (2005) 1017.
[13] G. Wang, D. Moses, A.J. Heeger, H.-M. Zhang, M. Narasimhan, R.E. Demaray, J. Appl. Phys. 95 (2004) 316.
[14] J. Lee, J.H. Kim, S. Im, Appl. Phys. Lett. 29 (2003) 2689.
[15] C.S. Kim, S.J. Jo, S.W. Lee, W.J. Kim, H.K. Baik, Appl. Phys. Lett. 88 (2006) 243515.
[16] J. Veres, S.D. Ogier, G. Lloyd, D.M. de Leeuw, Chem. Mater. 16 (2004) 4543.
[17] J. Veres, S.D. Ogier, S.W. Leeming, D.C. Cupertino, S.M. Khaffaf, Adv. Funct. Mater. 13 (2003) 199.
[18] P.D. Cozzoli, A. Kornowski, H. Weller, J. Am. Chem. Soc. 125 (2003) 14539.
[19] S.C. Lim, S.H. Kim, J.H. Lee, M.K. Kim, D.J. Kim, T. Zyung, Synthetic Met. 148 (2005) 75.
[20] Y.H. Noh, S.Y. Park, S.M. Seo, H.H. Lee, Org. Electronics. 7 (2006) 271.
[21] J. Jang, S.H. Han, SID Int. Symp. Digest Tech. Papers 37 (2006) 108.
[22] S.Y. Park, M. Park, H.H. Lee, Appl. Phys. Lett. 85 (2004) 2283.