Temperature Coefficient of Poly-Silicon TFT and Its Application on Voltage Reference Circuit With Temperature Compensation in LTPS Process

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***Abstract*—The temperature coefficient (TC) of n-type polycrystalline silicon thin-film transistors (poly-Si TFTs) is investigated in this paper. The relationship between the TC and the activation energy is observed and explained. From the experimental results, it is also found that TC is not sensitive to the deviation of the laser crystallization energy. On the contrary, channel width can effectively modulate the TC of TFTs. By using the diode-connected poly-Si TFTs with different channel widths, the first voltage reference circuit with temperature compensation for precise analog circuit design on glass substrate is proposed and realized. From the experimental results in a low-temperature poly-Si process, the output voltage of voltage reference circuit with temperature compensation exhibits a very low TC of 195 ppm/°C, between 25 °C and 125 °C. The proposed voltage reference circuit with temperature compensation can be applied to design precise analog circuits for system-on-panel or system-on-glass applications, which enables the analog circuits to be integrated in the active-matrix liquid crystal display panels.**

***Index Terms*—System on glass, system on panel, temperature coefficient (TC), thin-film transistor (TFT), voltage reference circuit.**

I. Introduction

POLYCRYSTALLINE silicon thin-film transistors (poly-Si TFTs) with the increased carrier mobility have been widely used in active-matrix liquid crystal displays (AMLCDs), which integrated the corresponding peripheral driving circuitry on panel [1], [2]. The CPU, memory, timing controller, digital-to-analog converter, and driving buffer had been implemented on glass substrate with the low-temperature poly-Si (LTPS) TFT process. LTPS AMLCDs integrated with driver and control circuits on glass substrate have been practically applied in portable systems, such as mobile phone, digital camera, notebook, etc. [3], [4]. However, even with the advanced crystallization technologies such as the excimer laser annealing (ELA) or the sequential laser solidification process, it is still observed that the carrier transport in poly-Si TFTs is dominated by the thermionic emission effect [5], [6]. The energy barriers at grain boundaries confine the carrier movement, reduce the field-effect mobility, and make the device characteristics strongly dependent on temperature. As a result, to reduce the impact of temperature variation on the performance of analog circuits in the LTPS process is a very important design challenge.

The voltage reference circuit with temperature compensation is the key design in analog circuits to provide a stable voltage reference with low sensitivity to temperature and supply voltage [7]–[10]. The voltage reference circuit with temperature compensation has been widely used in analog and digital circuits, such as DRAM, Flash memory, analog-to-digital converter, and so on. Although the voltage reference circuit with temperature compensation is important to provide a stable output voltage, the LTPS voltage reference circuit with temperature compensation on glass substrate was never reported in the past. The conventional CMOS voltage reference circuit with temperature compensation incorporated with BJTs or p-n junction diodes is a great challenge for LTPS process, since the characteristics of the poly-Si BJTs or the poly-Si p-n junction diodes are still unknown or lack of investigation. On the contrary, the characteristics of LTPS TFT devices are strongly dependent on temperature even if the devices are operated in saturation region [5], [6]. Therefore, the LTPS voltage reference circuit with temperature compensation can be realized by using only the LTPS TFT devices on glass substrate.

In this paper, the temperature coefficient (TC) of LTPS TFT devices is first analyzed. The relationship between the activation energy and the TC is investigated. Then, the influences from the laser energy density of the ELA process on the TC of TFT devices are discussed. Followed by the investigation on the channel width effect to the TC, a combination of a narrow-width device and a wide-width device is proposed to generate a positive TC by an appropriate circuit arrangement. The positive TC can be used to compensate the negative TC of TFT devices to achieve the design of a stable output voltage with low sensitivity to the temperature. Finally, this concept has been demonstrated with the first on-glass voltage reference circuit with temperature compensation in LTPS process.

Manuscript received March 13, 2008; revised July 1, 2008. Current version published September 24, 2008. This work was supported in part by the National Science Council, Taiwan, R.O.C., under Project NSC96-2221-E-009-127-MY2, by the AU Optronics Corporation, Taiwan, and by the Ministry of Economic Affairs, Taiwan, under Project MOEA-96-EC-17A-O7-S1-046. The review of this paper was arranged by Editor H.-S. Tae.

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Digital Object Identifier 10.1109/TED.2008.2003087

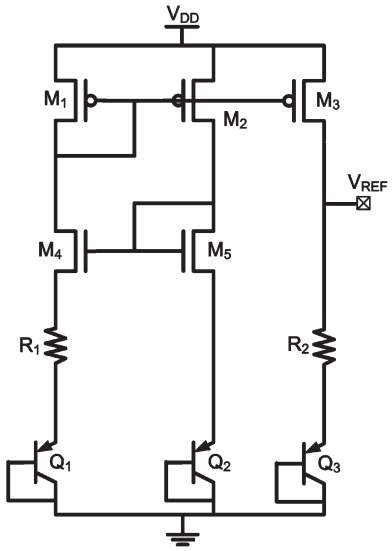

Fig. 1. Traditional voltage reference circuit with temperature compensation in CMOS technology.

Without additional laser trimming after fabrication, the new proposed bandgap voltage reference circuit has been verified on the glass substrate with the output voltage of 6.87 V at room temperature. The TC of voltage reference circuit with temperature compensation output voltage is 195 ppm/°C under VDD power supply of 10 V when the temperature varies from 25 °C to 125 °C.

II. Traditional Voltage Reference Circuit With Temperature Compensation in CMOS Technology

A traditional implementation of voltage reference circuit with temperature compensation in CMOS technology is shown in Fig. 1 [11]. In this circuit, the output voltage ($V_{\rm REF}$) is the sum of a base–emitter voltage ($V_{\rm EB}$) of BJT Q3 and the voltage drop across the upper resistor R2. The BJTs (Q1, Q2, and Q3) are typically implemented by the diode-connected vertical parasitic p-n-p bipolar junction transistors in CMOS process with the current proportional to $\exp(V_{\rm EB}/V_T)$, where $V_T(=kT/q)$ is the thermal voltage. Under constant current bias, $V_{\rm EB}$ is strongly dependent on V_T as well as temperature. The current mirror is designed to bias $\rm Q_1$, $\rm Q_2$, and $\rm Q_3$ with identical current. Then, the voltage drop on the resistor R_1 can be expressed by

$$V_{R1} = V_T \ln\left(\frac{A_1}{A_2}\right) \tag{1}$$

where A_1 and A_2 are the emitter areas of $\rm Q_1$ and $\rm Q_2$. It is noted that V_{R1} exhibits a positive TC when A_1 is larger than A_2. Moreover, since the current that flows through R_1 is equal to the current that flows through R_2, the voltage drop on the resistor R_2 can be expressed by

$$V_{R2} = \frac{R_2}{R_1} V_T \ln\left(\frac{A_1}{A_2}\right). \tag{2}$$

Hence, the output voltage of the traditional voltage reference circuit with temperature compensation can be written as

$$V_{\rm REF} = V_{\rm EB3} + \frac{R_2}{R_1} V_T \ln\left(\frac{A_1}{A_2}\right). \tag{3}$$

The second item in (3) is proportional to the absolute temperature (PTAT), which is used to compensate the negative TC of $V_{\rm EB3}$. In general, the PTAT voltage comes from the thermal voltage V_T with a TC of about $+0.085$ mV/°C in CMOS technology, which is quite smaller than that of $V_{\rm EB}$. After multiplying the PTAT voltage with an appropriate factor (R_2/R_1) and summing with $V_{\rm EB}$, the voltage reference circuit with temperature compensation would result in a very low sensitivity to temperature. Consequently, if a proper ratio of resistors is kept, the output voltage $(V_{\rm REF})$ with a very low sensitivity to temperature can be obtained.

From the analysis on traditional voltage reference circuit with temperature compensation, it is known that the realization of voltage reference circuit with temperature compensation in CMOS process strongly depends on the TC of BJTs ($\rm Q_1$, $\rm Q_2$, and $\rm Q_3$). In other words, the exponential term $\exp(V_{\rm EB}/V_T)$ in the I–V relationship of BJTs makes it possible to obtain a PTAT voltage from the voltage difference of a large-area BJT and a small-area BJT. The voltage across MOSFETs was not sensitive to temperature; thus, MOSFETs were seldom used in voltage reference circuit with temperature compensation directly. A pure MOSFET voltage reference circuit with temperature compensation was realized only when the MOSFETs are biased in subthreshold region [9]. Unlike the MOSFETs, the characteristics of LTPS TFTs are strongly dependent on temperature even when the devices are operated in above threshold region [5], [6]. Therefore, it is expected that the voltage reference circuit with temperature compensation can be realized by using only the LTPS TFT devices on glass substrate.

III. TFT Fabrication

For device analysis, the typical top-gate coplanar self-aligned n-type poly-Si TFTs with 1.25-μm-length LDD structure in a 3-μm LTPS process were used in this paper. First, the buffer layer was deposited on the glass substrate. Then, the undoped 50-nm-thick a-Si layer was deposited and crystallized by XeCl excimer laser with a laser energy density varied from 340 to 420 mJ/cm^2. The recrystallized poly-Si films were patterned into the active islands. Afterward, the 60-nm-thick oxide layer was deposited as the gate insulator. Then, the 200-nm-thick molybdenum was deposited and patterned as the gate electrode. The $\rm n^-$ doping was performed self-aligned to the gate electrode. The $\rm n^+$ source/drain region was defined by an additional mask. The dopants were activated by thermal process. After the deposition of nitride passivation and the formation of contact holes, the 550-nm-thick titanium/aluminum/titanium trilayer metal was deposited and patterned as the metal pads. The channel lengths of TFT devices are all kept as 6 μm while the channel widths are designed from 30 to 6 μm in the on-glass voltage reference circuit with temperature compensation.

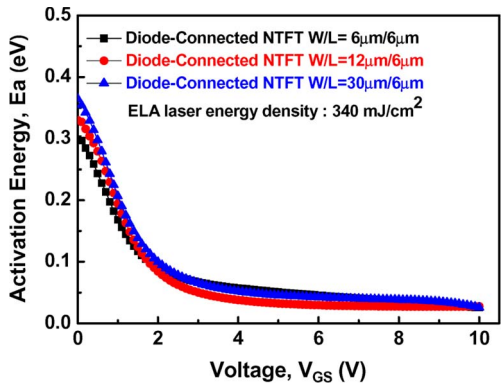

Fig. 2. Activation energy as a function of $V_{\rm GS}$ for diode-connected NTFTs with W/L of 6 μm/6 μm, 12 μm/6 μm, and 30 μm/6 μm.

IV. Measured Results and Temperature Model

Since the temperature response of the LTPS devices is mostly influenced by the thermionic emission effect with an activation energy associated with the grain boundary barrier height, the relationship between the activation energy and the TC is first investigated in this paper. As shown in Fig. 2, the activation energy (E_a) extracted from the Arrhenius plot of the drain current is depicted as a function of the gate bias $(V_{\rm GS})$. The drain bias $(V_{\rm DS})$ is equal to $V_{\rm GS}$ for the diode-connected TFT devices. Devices with three different channel widths are measured in Fig. 2. Devices are fabricated in the same run with identical crystallization laser energy density. It is found that, similar to the three-terminal LTPS devices, E_a of the diode-connected devices is strongly dependent on $V_{\rm GS}$. Under small gate bias, E_a is high. When $V_{\rm GS}$ is increased, E_a decreases drastically. It is well known that, for the three-terminal LTPS TFTs, the measured activation energy represents the grain boundary energy barrier of the poly-Si film which is sensitive to the poly-Si thin-film properties [5], [6]. Channel width has no influence on the thin-film properties; thus, devices with different channel widths exhibit similar E_a characteristics as those measured in Fig. 2.

Then, to extract the TC, the setup to measure $V_{\rm GS}$ of the fabricated devices under the bias of three different current levels (1, 10, and 50 μA) is shown in Fig. 3(a). The measured $V_{\rm GS}$ of the fabricated device with a channel width of 30 μm is shown as a function of temperature in Fig. 3(b). As shown in Fig. 3(b), $V_{\rm GS}$ is decreased while the temperature increases. An almost linear relationship between $V_{\rm GS}$ and temperature can be observed in Fig. 3(b), where the slope represents the TC. For the diode-connected NTFT with a channel width of 30 μm under different current levels, the TC is negative. Additionally, the magnitude of TC decreases when the bias current is increased. When the bias current increases from 1, 10, to 50 μA, the TC varies from -6.04, -5.04, to -2.96 mV/°C. It is noted that for one identical diode-connected device, the increase of bias current gives rise to the increase of operation voltage. As a result, the larger bias current makes the devices operated under larger $V_{\rm GS}$ with smaller E_a and smaller magnitude of TC. This result clearly demonstrates the relationship between the activation energy and the TC. Furthermore, the aforementioned discussion can be expressed by the following derivation.

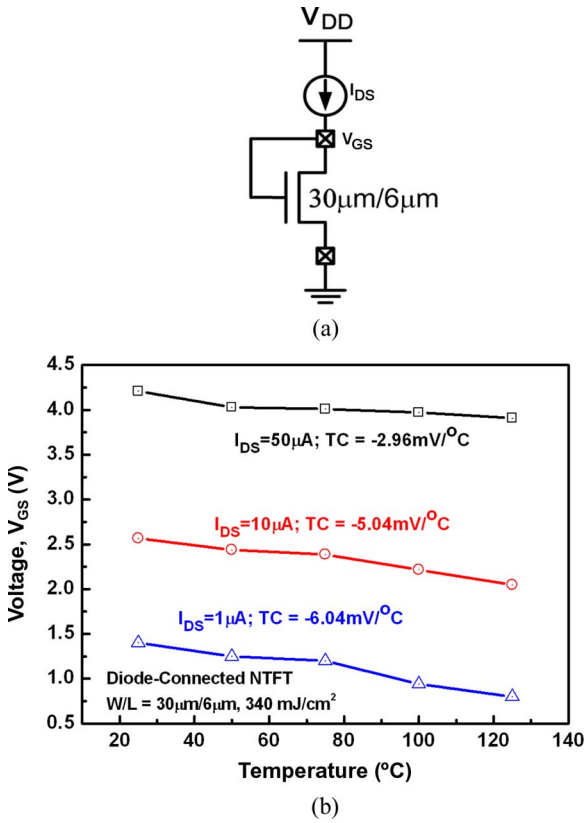

Fig. 3. (a) Setup to measure $V_{\rm GS}$ under the bias of $I_{\rm DS}$. (b) Relationship between $V_{\rm GS}$ and temperature under three different current levels (1, 10, and 50 μA).

For LTPS TFTs, the drain current $I_{\rm DS}$ of devices operated in saturation region can be expressed as [12], [13]

$$I_{\rm DS} = \frac{W}{2L}\mu_0 C_{\rm ox}(V_{\rm GS} - V_{\rm TH})^2 \exp\left(-\frac{V_B}{V_T}\right) \tag{4}$$

where μ_0 is the carrier mobility within the grain, L denotes the effective channel length, W is the effective channel width, $C_{\rm ox}$ is the gate oxide capacitance per unit area, $V_{\rm TH}$ is the threshold voltage of TFT device, and $V_{\rm GS}$ is the gate-to-source voltage of TFT device. V_B is the potential barrier at grain boundaries which is associated with the crystallization quality of the poly-Si film. When the activation energy is extracted from the Arrhenius plot of the drain current, E_a is equal to qV_B. Under small $V_{\rm GS}$, V_B is large. When the $V_{\rm GS}$ increases, V_B decreases rapidly. When the device in circuit is operated under small $V_{\rm GS}$, the drain current $I_{\rm DS}$ of device is dominated by the exponential term and can be simplified by

$$I_{\rm DS} = W\alpha \exp\left(-\frac{V_B}{V_T}\right) \tag{5}$$

where α is only weakly dependent on $V_{\rm GS}$ but is insensitive to temperature. Then, the equation of V_B can be derived as

$$V_B = V_T \ln\left(\frac{W\alpha}{I_{\rm DS}}\right) = \frac{kT}{q}\ln\left(\frac{W\alpha}{I_{\rm DS}}\right). \tag{6}$$

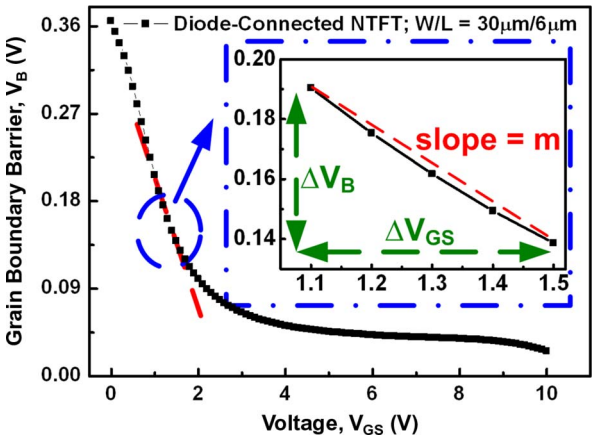

Fig. 4. Dependence between potential barrier of grain boundary V_B and gate-to-source voltage $V_{\rm GS}$ of diode-connected NTFT.

When there is a variation of temperature ΔT, the corresponding variation on V_B is

$$\Delta V_B = \frac{k\Delta T}{q} \ln\left(\frac{W\alpha}{I_{\rm DS}}\right). \tag{7}$$

Fig. 4 shows the measured dependence between potential barrier of grain boundary V_B and gate-to-source voltage $V_{\rm GS}$ of diode-connected NTFT with device dimension W/L of 30 μm/6 μm, whereas the laser energy density is kept at 340 mJ/cm^2. As shown in Fig. 4, the variation of V_B is related to the variation of $V_{\rm GS}$. Assume that the variation of $V_{\rm GS}(\Delta V_{\rm GS})$ is very small, and a negative linear approximation can be given between ΔV_B and $\Delta V_{\rm GS}$ as

$$\Delta V_{\rm GS} = -\frac{1}{m}\Delta V_B = -\frac{k\Delta T}{mq} \ln\left(\frac{W\alpha}{I_{\rm DS}}\right) \tag{8}$$

where m is the absolute slope of the linear approximation between ΔV_B and $\Delta V_{\rm GS}$ in Fig. 4. Finally, the TC can be found as

$$\text{TC} = \frac{\Delta V_{\rm GS}}{\Delta T} = -\frac{k}{mq} \ln\left(\frac{W\alpha}{I_{\rm DS}}\right) = -\frac{\Delta V_B}{m\Delta T}. \tag{9}$$

Even though the increase of V_B accompanies with the increase of m, the variation of V_B can be more significant than that of m under a proper design.

The activation energy, as well as the grain boundary barrier, should be related to the grain structure and the grain boundary property. It is therefore presumed that the laser energy density of the ELA process influences the grain structure and affects the TC of the devices. Fig. 5(a) shows the activation energy of the diode-connected devices with the poly-Si film crystallized under different laser energies (340, 400, and 420 mJ/cm^2). The channel width of the TFT device studied in Fig. 5(a) is 30 μm. The activation energy is found to be reduced with increasing laser energy density. As a result, the TC of the devices with higher laser energy density is also smaller than those with lower laser energy density, as shown in Fig. 5(b). However, the influence of laser energy density on the TC is not significant. When the laser energy density changes $\pm$10%, the TC changes only about $\pm$2.75%. The reason can be explained by identifying

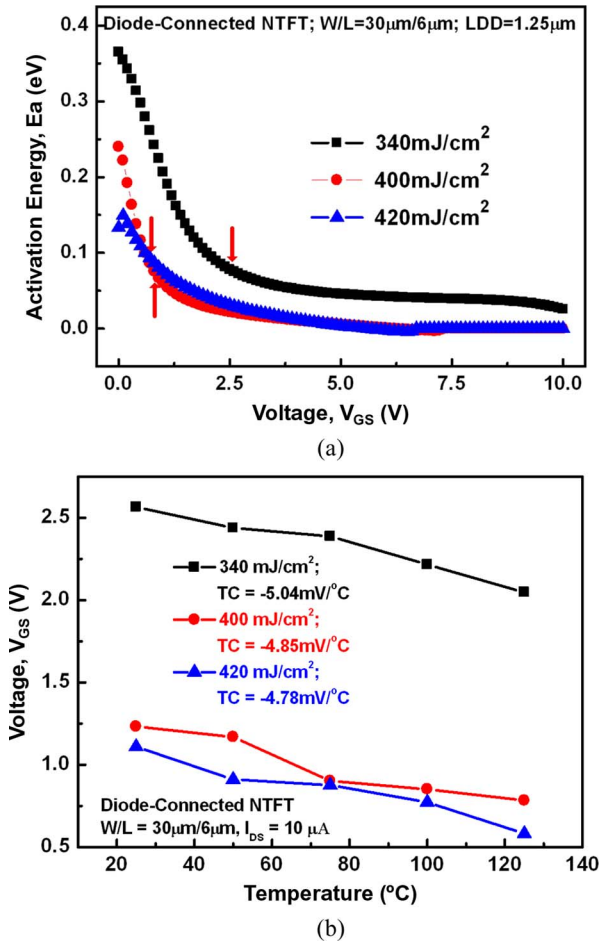

Fig. 5. (a) Activation energy as a function of $V_{\rm GS}$ for diode-connected NTFTs with poly-Si film crystallized by laser energy density as 340, 400, and 420 mJ/cm^2. (b) Relationship between $V_{\rm GS}$ and temperature under identical $I_{\rm DS}$ of 10-μA. Devices W/L are 30 μm/6 μm.

the biasing points of three devices in Fig. 5(a). The operation voltages of three devices under the bias of 10-μA $I_{\rm DS}$ are indicated by the arrow symbols in Fig. 5(a). It is found that the activation energies of the three biasing points are similar. This makes the TC insensitive to the deviation of the laser energy density in the ELA process. Similar results can be also observed for the devices with small channel width of 6 μm in Fig. 6(a) and (b), where the laser energies for poly-Si film crystallized are also 340, 400, and 420 mJ/cm^2.

The influence of the channel width on the TC, however, is found to be significant. When the diode-connected devices are biased under a constant current of 10 μA, $V_{\rm GS}$ of TFT devices with channel widths of 6 and 30 μm is shown as a function of temperature in Fig. 7, whereas the laser energy density is kept at 400 mJ/cm^2. Obviously, the wide-channel-width device exhibits more negative TC than the narrow-channel-width device. From Fig. 2, it has been observed that the channel width has only little influence on the device activation energy. However, when all the devices are biased by identical current source, the wide-channel-width devices are operated under small $V_{\rm GS}$, and the narrow-channel-width devices are operated under large $V_{\rm GS}$. When $V_{\rm GS}$ is reduced, the activation energy is drastically enlarged, as shown in Fig. 2. As a result, the absolute value

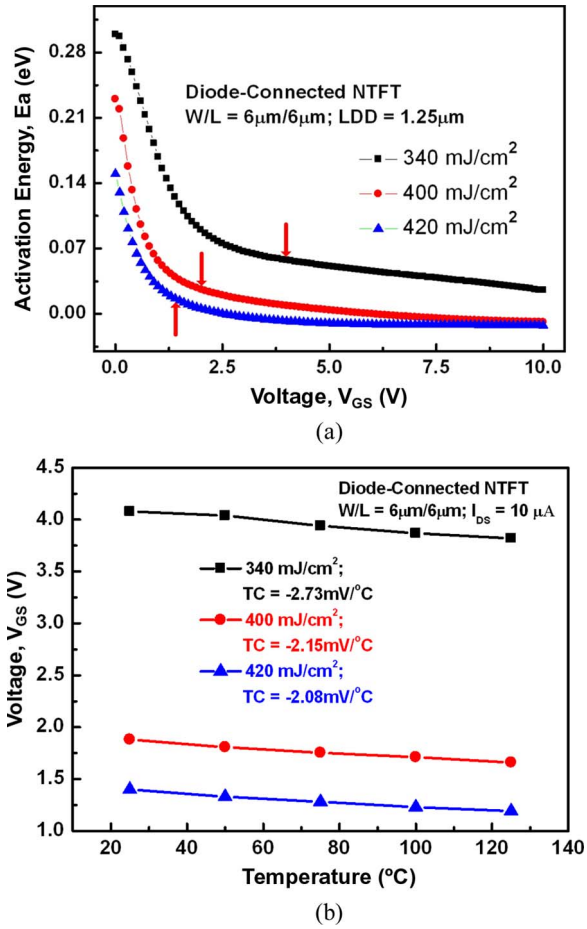

Fig. 6. Activation energy as a function of $V_{\rm GS}$ for diode-connected NTFTs with poly-Si film crystallized by laser energy density as 340, 400, and 420 mJ/cm^2. (b) Relationship between $V_{\rm GS}$ and temperature under identical $I_{\rm DS}$ as 10 μA. Devices W/L are 6 μm/6 μm.

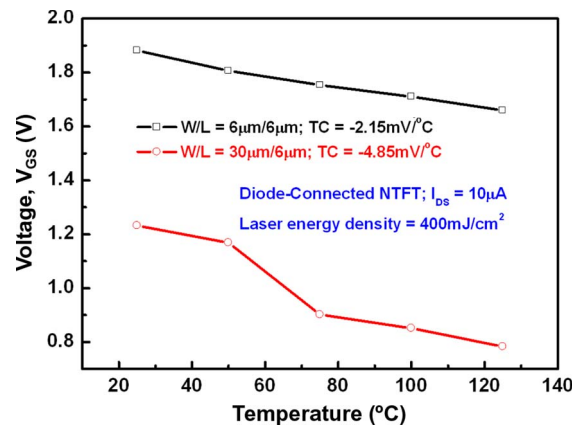

Fig. 7. Relationship between $V_{\rm GS}$ and temperature of devices with different channel widths under identical $I_{\rm DS}$ of 10 μA.

of the TC is significantly enlarged by increasing the channel width. Such a phenomenon can be also explained by (9).

Finally, the TC of the diode-connected NTFT devices biased under a 10-μA current is shown in Fig. 8. The influences of channel width and crystallization laser energy on the TC of the diode-connected NTFT devices are compared. It can be concluded that the influence of ELA laser energy density or

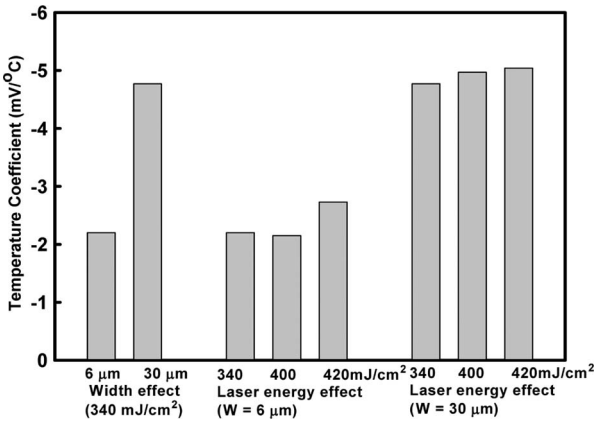

Fig. 8. TC of the diode-connected NTFT devices biased under a 10-μA current source to investigate the influences of channel width and crystallization laser energy on the TC of the diode-connected NTFT devices.

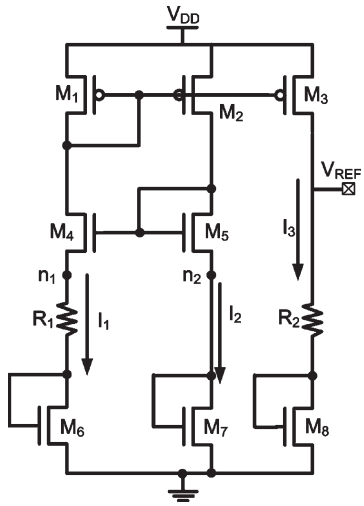

Fig. 9. Implementation of the new proposed voltage reference circuit with temperature compensation in a 3-μm LTPS process.

the poly-Si thin-film property on the TC is relatively small. This makes the voltage reference circuit with temperature compensation not sensitive to the deviation of the laser annealing process in the LTPS technology. On the contrary, changing the device channel width can effectively change the TC of the diode-connected device. This enables the designer to modulate the TC of the diode-connected devices easily.

V. Application on Voltage Reference Circuit With Temperature Compensation in LTPS Technology

The difference of TCs between the wide-channel-width device and the narrow-channel-width device is very useful if a positive TC can be extracted from the $V_{\rm GS}$ of the wide-channel-width device to the $V_{\rm GS}$ of the narrow-channel-width device. This positive TC can be used to compensate the negative TC in the $V_{\rm GS}$ of TFT devices.

A. Implementation

The new proposed voltage reference circuit with temperature compensation designed and fabricated by a 3-μm LTPS technology is shown in Fig. 9. In this circuit, the TFTs M_1, M_2,

M_3, M_4, and M_5 are biased in saturation region. The diode-connected NTFT devices M_6, M_7, and M_8, which replace the diode-connected BJTs in traditional CMOS voltage reference circuit with temperature compensation (Fig. 1) [11], are also biased in saturation region. The nodes n_1 and n_2 are designed to have equal potential by the current mirror circuit.

The channel width of $M_6(W_6)$ is larger than that of $M_7(W_7)$; thus, the TC of M_6 is more negative than that of M_7. The voltage drop on the resistor $R_1(V_{R1})$ therefore exhibits a positive TC. If the dependence of m on $V_{\rm GS}$ is neglected, the variation of $V_{R1}(\Delta V_{R1})$ as a function of ΔT can be expressed as

$$\Delta V_{\rm R1} = \frac{k\Delta T}{mq}\ln\left(\frac{W_6}{W_7}\right) = \frac{k\Delta T}{mq}\ln N. \tag{10}$$

Obviously, ΔV_{R1} is proportional to the absolute temperature (PTAT). Hence, a PTAT loop is formed by M_6, M_7, and R_1. The PTAT current variation ΔI_1 can be written as

$$\Delta I_1 = \frac{k\Delta T}{mqR_1}\ln N \tag{11}$$

where $N\ (= W_6/W_7)$ is the channel width ratio of M_6 and M_7. The current mirror, which is composed of M_1, M_2, and M_3, imposes equal currents in these three branches I_1, I_2, and I_3 of the circuit. The output voltage $(V_{\rm REF})$ is the sum of a gate–source voltage of TFT M_8 $(V_{\rm GS8})$ and the voltage drop across the upper resistor (V_{R2}). Therefore, the output voltage variation $(\Delta V_{\rm REF})$ of the new proposed voltage reference circuit with temperature compensation can be expressed as

$$\Delta V_{\rm REF} = \Delta I_3 R_2 + \Delta V_{\rm GS8} = \frac{R_2}{R_1}\frac{k\Delta T}{mq}\ln N + \Delta V_{\rm GS8} \tag{12}$$

where R_1 and R_2 are the resistances shown in Fig. 9. The first item in (12) with positive TC is proportional to the absolute temperature (PTAT), which is used to compensate the negative TC of $\Delta V_{\rm GS8}$. After multiplying the PTAT voltage with an appropriate factor (proper ratio of resistors) and summing with $\Delta V_{\rm GS8}$, the output voltage of voltage reference circuit with temperature compensation would result in a very low sensitivity to temperature.

The proposed voltage reference circuit with temperature compensation has been fabricated in a 3-μm LTPS technology. Fig. 10 shows the chip photo of the new proposed voltage reference circuit with temperature compensation fabricated on glass substrate. The chip size of the proposed voltage reference circuit with temperature compensation is $400 \times 380\ \mu{\rm m}^2$. The resistances R_1 and R_2 implemented by the poly resistance are also included into the layout.

B. Measurement Results

The threshold voltage of TFT devices in a 3-μm LTPS technology is $V_{\rm thn} \approx V_{\rm thp} \approx 1.25$ V at 25 °C. The total gate area of M_6 is 480 $\mu{\rm m}^2$, and that of M_7 is 80 $\mu{\rm m}^2$ in this fabrication. The resistors in this chip, formed by poly resistors, have minimum process variation to improve the accuracy of resistance ratio. The power supply voltage $V_{\rm DD}$ is set to 10 V,

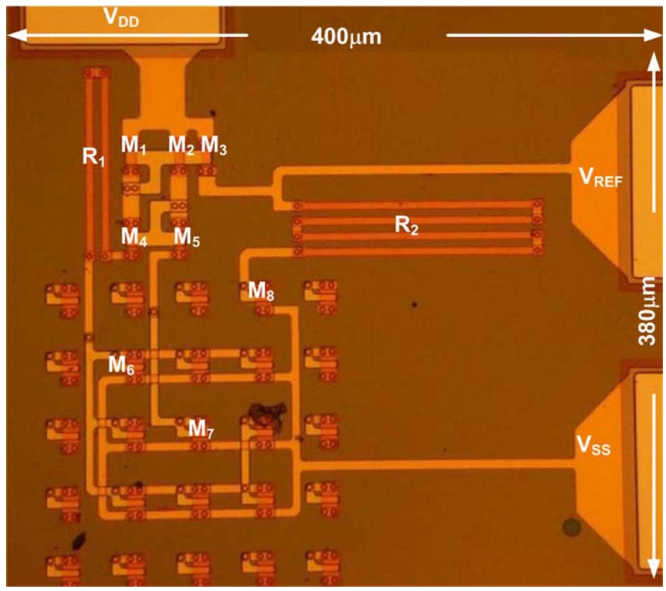

Fig. 10. On-glass circuit photograph of the new proposed voltage reference circuit with temperature compensation fabricated in a 3-μm LTPS process.

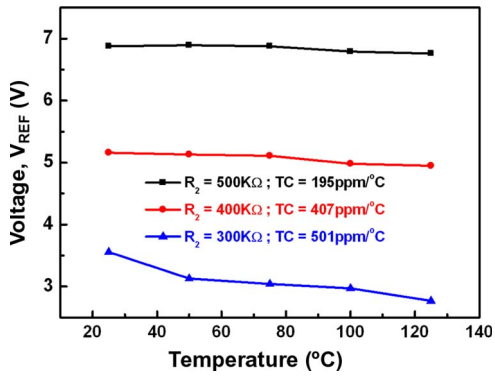

Fig. 11. Measured output voltage $V_{\rm REF}$ of the fabricated voltage reference circuit with temperature compensation under different resistance of R_2 without laser trimming after fabrication.

and the total operating current is 8.97 μA. The measured results of the output voltage $V_{\rm REF}$ from 25 °C to 125 °C are shown in Fig. 11, where the R_2 is drawn with different values in the test chips. As R_2 is equal to 500 kΩ, the measured TC of the fabricated voltage reference circuit with temperature compensation on glass substrate is around 195 ppm/°C without laser trimming after fabrication, whereas the output voltage $(V_{\rm REF})$ is kept at 6.87 V.

VI. Conclusion

The TC of TFT devices in LTPS technology is strongly dependent on the activation energy of the devices. With a suitable control, higher activation energy gives rise to higher absolute value of the TC. The influence of the laser energy density in ELA process on the TC of the devices is not significant. On the other hand, the bias current level and the channel width have a strong impact on the device TC. As a result, the TC of devices can be controlled by regulating the channel width of the devices. With an appropriate circuit design, a positive TC can be generated by using the voltage drop between devices

that have different TCs (different channel widths). Then, the positive TC can be used to compensate the negative TC from the devices. The first voltage reference circuit with temperature compensation has been successfully verified in a 3-μm LTPS process. The measured reference output voltage is 6.87 V with a TC of 195 ppm/°C. The proposed voltage reference circuit with temperature compensation consumes an operating current of only 8.97 μA under the supply voltage of 10 V on glass substrate. This new voltage reference circuit with temperature compensation can be used to realize precise analog circuits in LTPS process for system-on-glass applications.

ACKNOWLEDGMENT

The authors would like to thank C.-H. Kuo, C.-H. Li, Y.-J. Hsieh, W.-M. Huang, K.-C. Lin, C.-C. Shih, C.-C. Chiu, and Dr. C.-Y. Liu for their valuable technical suggestions and the AU Optronics Corporation, Taiwan, R.O.C., for the fabrication support of on-glass devices and circuits.

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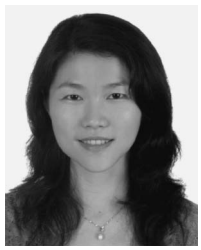

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