A Multicell Linear Power Amplifier for Driving Piezoelectric Loads

Shyr-Long Jeng and Yung-Cheng Tung

***Abstract*—A multicell amplifier is developed by connecting floating signal modules in series to drive piezoelectric devices. The amplifier generates a high voltage gain by summing the individual module gains. The bandwidth equals that of a single module. The multicell amplifier provides a means of achieving high power and can divide the total power dissipation among the modules, because each module delivers the same output voltage and current. A prototype circuit that consists of six floating signal modules exhibits precise linear operation over a wide range of input frequencies and capacitive loads. The circuit provides a $\pm$200-V output swing with a corner frequency of around 100 kHz at a driving capacitive load of 0.1 μF. The slew rate is as high as 115 V/μs, and the maximum output current is $\pm$2.6 A. The practicality and performance of the presented modular implementation concepts were verified by the close match between the simulated and experimental results.**

***Index Terms*—Piezoelectric device, power amplifiers, switching amplifiers.**

I. Introduction

PIEZOELECTRIC devices or actuators have been used as positioners or driving motors in many fields such as optics, precision machining, and fluid control, as well as in optical disk drives, because they offer compactness, high energy density, rapid response, and controllable displacement down to nanometers or less. Such actuators are assembled from thin laminar wafers of ceramic material, which are electrically connected in parallel. Increasing the voltage increases the length of the stack to a maximum strain for a typical maximum input voltage. The applied voltage depends on the thickness of the ceramic and on its material properties. It typically ranges from a few tens of volts to a few hundred volts. The reactive powers induced by the highly capacitive characteristics of the actuators will detrimentally affect the driving amplifiers.

Several approaches have been proposed to reduce the inherent hysteretic nonlinearity by driving piezoelectric actuators with charge or current, rather than voltage [1]–[5]. Saturation and distortion occur when the output voltage reaches the power supply rails. A popular scheme is to short the loading circuit, or periodically discharge the loading capacitance and reset the dc voltage to ground during handling. The resulting loads induce an undesirable high-frequency disturbance and considerably distort the control signal that is applied to the piezoelectric load.

Voltage amplifiers are often used to drive piezoelectric actuators because they can precisely generate any waveform. Two topologies of amplifiers have been realized for driving piezoelectric actuators [6], [7]. One is based on switching, and the other is a linear amplifier.

A. Switching Amplifier

In a switching amplifier [8]–[13], a setup stage is initially adopted to generate the constant high voltage required by the piezoelectric actuator. The second stage is a half- or a full-bridge, which delivers the output voltage to the actuator as dictated by the reference signal. The output voltage is synthesized by appropriately controlling the power transistors using a pulsewidth modulator (PWM). The switches of the power transistors cause a ripple voltage on top of these mean waveforms. This ripple voltage acts as a disturbance signal on the actuator, causing high-frequency excitation and undesired heating in the actuator. The ripple noise may be reduced by increasing the switching frequency. However, increasing the switching frequency increases the number of transistor switches, as well as the switching losses in the power transistors, during the same operating time interval. The switching frequency is typically held constant in a PWM controller and is set to be between a few kilohertz and a few hundred kilohertz. The bandwidth of the switching amplifier is limited because the signal frequency must be much lower than the switching frequency. The benefit of the switching amplifier is that it can establish an electric field in the actuator with minimal power loss and can recycle reactive energy back to the power source.

B. Linear Amplifier

The linear amplifier has higher bandwidth, slew rate, and linearity than a switching amplifier. It also has less noise. However, the linear amplifier consumes more power than the switching amplifier when it is driving capacitive loads [6]. Montane *et al.* [14] found an integrated driving solution based on a full custom design of a high-voltage operational amplifier (op-amp), which is compatible with the relevant high-density packaging constraints. An attractive method [15], [16] involves a combination of op-amps and MOSFETs. The current driving capacity can readily be increased. This method requires appropriate protection circuits to reduce excessive change rates and to operate transistors in the safe working region. A bridge

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configuration [17], which employs two high-voltage op-amps connected in a bridge circuit, can deliver an output voltage swing that is double that delivered by a single device. Stiebel and Janocha [18] proposed a hybrid amplifier, which combines the high efficiency of a switching amplifier with the output signal accuracy of an analog amplifier. The advantage of the circuit is that power losses may be kept in tolerable limits, although the total actuator current flows through the analog final stage. Savicki [19] and Condon and Savicki [20] presented an amplifier that comprises a stack of series-connected charge-storage capacitors serving as an effective multiple power supply source for driving a large capacitive load. The recovered energy is stored in the series-connected capacitors to be reused during the subsequent load charge cycle, thus reducing the net energy required from the power supply per complete cycle. Henderson *et al.* [21] presented a series resonant circuit, in which a relatively low-voltage square-wave signal can generate a high-voltage sinusoidal output voltage. MOSFET power transistors that rapidly and efficiently switch on and off with high current capacity and excellent efficiency are readily available. A limitation on the resonant circuit is that it must be operated at a fixed frequency to yield a pure sinusoidal output waveform.

II. Multicell Amplifier

The multicell amplifier described herein provides greater flexibility and wider bandwidth than those that rely on high-voltage op-amps. The circuit is easily implemented by connecting floating signal modules in series. These modules are realized using IC-style op-amps. When configured in this way, the multicell amplifier can deliver output voltage swings that are the sums of the swings of individual modules. As the overall gain is increased by adding floating signal modules, the bandwidth does not change. The gain–bandwidth product multiplies. The power dissipated by the amplifier increases with frequency because capacitors draw more current at higher frequencies. The output of each floating signal module can deliver the same current to the load. The maximum output power may be dissipated by each module.

A. Floating Signal Module

As presented in Fig. 1, a floating signal module comprises an isolation amplifier and a pair of difference amplifiers that are connected in a cascade form. The isolation amplifier can electrically isolate a signal source from an output stage, whose potential differs from the ground potential of the signal source. A differential output voltage established on the other side of the isolation barrier yields a balanced amplifier and directly connects to the input terminals of the next stage. A pair of difference amplifiers connected in a bridge configuration is adopted as the second output stage. The upper difference amplifier is connected in a noninverting configuration, whereas the lower difference amplifier is connected in an inverting configuration. The output swing across the load is, therefore, double the swing that would be produced by a single difference amplifier. Any nonlinearity becomes symmetrical, reducing the second harmonic distortion to less than that associated with a single difference amplifier.

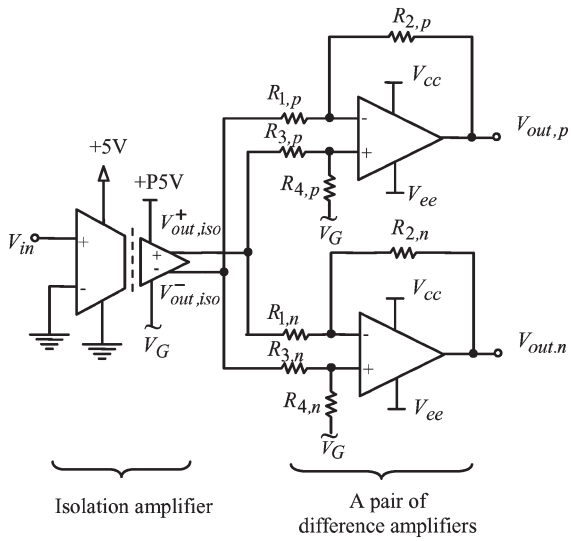

Fig. 1. Floating signal module.

The output voltage of the upper difference amplifier in the noninverting configuration is

$$V_{\mathrm{out,p}} = A_{\mathrm{iso,d}} A_{\mathrm{cl,d,p}} V_{\mathrm{in}} + \frac{1}{2} A_{\mathrm{iso,cm}} A_{\mathrm{cl,cm,p}} V_{\mathrm{in}} + V_G \quad (1)$$

where $A_{\mathrm{iso,d}}$ and $A_{\mathrm{iso,cm}}$ are the differential- and common-mode gains of the isolation amplifier, respectively, $A_{\mathrm{cl,d}}$ and $A_{\mathrm{cl,cm}}$ are the differential- and common-mode voltage gains of the difference amplifier, respectively, and V_G is the ground potential. An analogous analysis of the inverting configuration achieves similar results, producing the negative differential-mode output voltage and the same common-mode voltage when the two difference amplifiers are identical. Thus

$$V_{\mathrm{out,n}} = -A_{\mathrm{iso,d}} A_{\mathrm{cl,d,n}} V_{\mathrm{in}} + \frac{1}{2} A_{\mathrm{iso,cm}} A_{\mathrm{cl,cm,n}} V_{\mathrm{in}} + V_G. \quad (2)$$

The subscripts after the comma, i.e., p and n, refer to the noninverting and inverting configurations, respectively. The overall output of the floating signal module is

$$\begin{aligned} V_{\mathrm{out}} &= V_{\mathrm{out,p}} - V_{\mathrm{out,n}} \\ &= (A_{\mathrm{cl,d,p}} + A_{\mathrm{cl,d,n}}) A_{\mathrm{iso,d}} V_{\mathrm{in}} \\ &\quad + \frac{1}{2} (A_{\mathrm{cl,cm,p}} - A_{\mathrm{cl,cm,n}}) A_{\mathrm{iso,cm}} V_{\mathrm{in}}. \end{aligned} \quad (3)$$

The output signal is independent on the ground pin, which is the key to the flexibility of the floating signal module.

B. Cascaded Multicell Amplifier

The cascaded multicell amplifier shown in Fig. 2 consists of familiar floating signal modules in a cascaded connection. Each floating signal module is made from low-voltage devices and provides both positive and negative analogous voltage levels. In the following, the superscript i refers to the ith cell of a floating signal module. The isolated bipolar power sources are required to provide sufficient power to the floating signal module and to deliver a specified power to a load. Previous results indicate

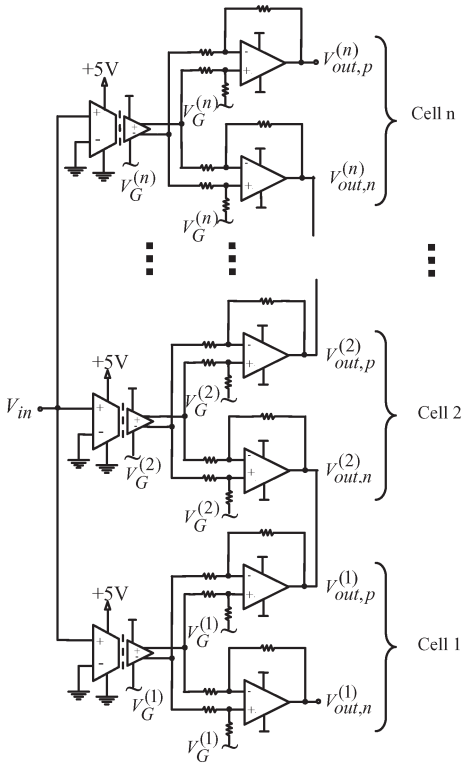

Fig. 2. Multicell structure of the piezoelectric amplifier.

that each floating signal module yields two output voltages $V_{\mathrm{out,p}}^{(i)}$ and $V_{\mathrm{out,n}}^{(i)}$, which are equal in magnitude but antiphase. The noninverting output terminal of the $(i-1)$th cell of the floating signal module is directly connected to the inverting output terminal of the ith cell of the floating signal module, i.e.,

$$V_{\mathrm{out,p}}^{(i-1)} = V_{\mathrm{out,n}}^{(i)}. \tag{4}$$

Substituting (1) and (2) into (4) and rearranging the terms yields

$$V_G^{(i)} = V_G^{(i-1)} + A_{\mathrm{iso,d}}^{(i)} A_{\mathrm{cl,d,n}}^{(i)} V_{\mathrm{in}} + A_{\mathrm{iso,d}}^{(i-1)} A_{\mathrm{cl,d,p}}^{(i-1)} V_{\mathrm{in}} - \frac{1}{2} A_{\mathrm{iso,cm}}^{(i)} A_{\mathrm{cl,cm,n}}^{(i)} V_{\mathrm{in}} + \frac{1}{2} A_{\mathrm{iso,cm}}^{(i-1)} A_{\mathrm{cl,cm,p}}^{(i-1)} V_{\mathrm{in}}. \tag{5}$$

The maximum output voltage between the noninverting output terminal of the ith cell of the floating signal module and the inverting output terminal of the first cell of the floating signal module is

$$V_{\mathrm{out,p}}^{(i)} - V_{\mathrm{out,n}}^{(1)} = A_{\mathrm{iso,d}}^{(i)} A_{\mathrm{cl,d,p}}^{(i)} V_{\mathrm{in}} + \frac{1}{2} A_{\mathrm{iso,cm}}^{(i)} A_{\mathrm{cl,cm,p}}^{(i)} V_{\mathrm{in}} + V_G^{(i)} + A_{\mathrm{iso,d}}^{(1)} A_{\mathrm{cl,d,n}}^{(1)} V_{\mathrm{in}} - \frac{1}{2} A_{\mathrm{iso,cm}}^{(1)} A_{\mathrm{cl,cm,n}}^{(1)} V_{\mathrm{in}} - V_G^{(1)}. \tag{6}$$

Solving the ground potential among each cell circuit by recursively commutating from (5) enables (6) to be rewritten as

$$V_{\mathrm{out,p}}^{(i)} - V_{\mathrm{out,n}}^{(1)} = \sum_{k=1}^{i} \left(A_{\mathrm{cl,d,p}}^{(k)} + A_{\mathrm{cl,d,n}}^{(k)} \right) A_{\mathrm{iso,d}}^{(k)} V_{\mathrm{in}} + \sum_{k=1}^{i} \left(A_{\mathrm{cl,cm,p}}^{(k)} - A_{\mathrm{cl,cm,n}}^{(k)} \right) A_{\mathrm{iso,cm}}^{(k)} V_{\mathrm{in}}. \tag{7}$$

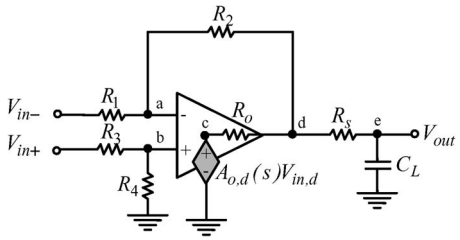

Fig. 3. Equivalent circuit of the difference amplifier with nonzero output resistance and capacitive load.

Clearly, when difference amplifiers in floating signal modules match on each cell, common-mode signals formed by the internal op-amp devices or tolerances among discrete resistors may appear almost constant at the noninverting and inverting terminals. The final term in (7) is the net common-mode signal and approaches zero. The differential-mode signal represented by the first term in (7) is double that which would be generated by the noninverting or inverting single output voltages. The synthesized voltage waveform may be specified as a sum of output voltages of floating signal module cells. Any number of floating signal modules may have, in general, any number of cells.

III. Frequency Response Due to Capacitive Loads

Capacitive loads commonly cause problems, partly because they can greatly reduce the output bandwidth and slew rate, but primarily because the phase lag generated in the feedback loop can cause the amplifier to oscillate. The frequency response of the difference amplifier in the output portion is initially studied to determine the stability of the multicell amplifier with the capacitive loads. The open-loop output resistance R_o is the factor that most strongly influences the variation in output performance with the capacitive load. Fig. 3 presents the equivalent circuit of the difference amplifier. An external resistor R_s is placed between the output of the difference amplifier and the load. The resistor isolates the op-amp output and the feedback network from the capacitive load, potentially eliminating the oscillation or reducing ringing. The combination of the isolation resistor and the load capacitor introduces a pole to increase stability by increasing the phase margin of the overall system. The equivalent circuit has a finite open-loop gain and a nonzero output resistance. The open-loop input resistance between the two input terminals of the op-amp is assumed to be ideal and, thus, is assumed to be very large in most cases. Rearranging terms in Kirchhoff's current law equations for nodes a, b, c, d, and e yields

$$V_o = \left(\frac{R_4/R_3}{(1+R_4/R_3)} \left(A_{\mathrm{o,d}} + \frac{A_{\mathrm{o,cm}}}{2} \right) + \frac{R_2/R_1}{(1+R_2/R_1)} \left(A_{\mathrm{o,d}} - \frac{A_{\mathrm{o,cm}}}{2} - \frac{R_0}{R_2} \right) \right) \frac{V_{\mathrm{in,d}}}{2M'} + \left(\frac{R_4/R_3}{(1+R_4/R_3)R_o} \left(A_{\mathrm{o,d}} + \frac{A_{\mathrm{o,cm}}}{2} \right) - \frac{R_2/R_1}{(1+R_2/R_1)} \left(A_{\mathrm{o,d}} - \frac{A_{\mathrm{o,cm}}}{2} - \frac{R_0}{R_2} \right) \right) \frac{V_{\mathrm{in,cm}}}{M'} \tag{8}$$

where

$$M' = \left(1 + \frac{A_{\mathrm{o,d}}}{1 + R_2/R_1} - \frac{A_{\mathrm{o,cm}}}{2(1 + R_2/R_1)} + \frac{R_o}{R_1 + R_2} + \frac{R_o}{R_s + 1/C_L s}\right)(1 + R_s C_L s).$$

A. Differential-Mode Gain in Single Difference Amplifier

The open-loop common-mode gain $A_{\mathrm{o,cm}}(s)$ is neglected because a linear op-amp can readily reject a common-mode signal. The two resistance ratios R_2/R_1 and R_4/R_3 must exactly be equal to enable the difference amplifier to reject a large common-mode signal and to simultaneously generate an output that is exactly proportional to the difference between the two input signals. Therefore, the overall differential-mode gain expressed in the first part of (8) is reduced to

$$A_{\mathrm{cl,d}}(s) \approx \frac{R_2}{R_1}\frac{1}{(1 + R_s C_L s)} \times \frac{R_o \| (R_1 + R_2) \| (R_s + 1/C_L s)}{(R_o \| (R_1 + R_2) \| (R_s + 1/C_L S) + Z_{\mathrm{cl,o}})} \quad (9)$$

where the closed-loop output impedance $Z_{\mathrm{cl,o}}$ of the difference amplifier, to a good approximation, is given by

$$Z_{\mathrm{cl,o}}(s) \approx \frac{(1 + R_2/R_1)R_o}{A_{\mathrm{o,d}}(s)}. \quad (10)$$

$R_1 + R_2$ is typically in the kilohm range, and the two resistances R_o and R_s are both on the order of 10 Ω. The effective resistance of combinations of R_o and R_s is smaller than that of $R_1 + R_2$. Therefore, (9) can be rewritten as

$$A_{\mathrm{cl,d}}(s) \approx \frac{R_2}{R_1}\frac{1}{(1 + R_s C_L s)}\frac{R_o \| (R_s + 1/C_L s)}{((R_o \| (R_s + 1/C_L s)) + Z_{\mathrm{cl,o}})}. \quad (11)$$

The frequency response of the open-loop differential-mode gain $A_{\mathrm{o,d}}(s)$ for a linear op-amp device can be characterized by inserting a dominant pole, as follows:

$$A_{\mathrm{o,d}}(s) = \frac{A_{\mathrm{o,d}}(0)}{1 + s/\omega_{\mathrm{o,d}}} \quad (12)$$

where $A_{\mathrm{o,d}}(0)$ is the low-frequency differential-mode gain, and $\omega_{\mathrm{o,d}}$ is the corresponding dominant pole frequency. Substituting (10) and (12) into (11) and rearranging terms yields

$$A_{\mathrm{cl,d}}(s) = \frac{R_2}{R_1}\frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (13)$$

where the natural frequency ω_n and the damping ratio ξ are defined by

$$\omega_n^2 = \frac{A_{\mathrm{o,d}}(0)\omega_{\mathrm{o,d}}}{(1 + R_2/R_1)(R_o + R_s)C_L} \quad (14)$$

and

$$\xi = \frac{R_s}{2}\sqrt{\frac{C_L A_{\mathrm{o,d}}(0)\omega_{\mathrm{o,d}}}{(1 + R_2/R_1)(R_o + R_s)}} + \frac{1 + (R_o + R_s)\omega_{\mathrm{o,d}} C_L}{2}\sqrt{\frac{(1 + R_2/R_1)}{(R_o + R_s)C_L A_{\mathrm{o,d}}(0)\omega_{\mathrm{o,d}}}}. \quad (15)$$

Since $A_{\mathrm{o,d}}(0)$ typically greatly exceeds $1 + R_2/R_1$, negative feedback drives the closed-loop output impedance $Z_{\mathrm{cl,o}}$ in (10) to some low value at a low frequency. The third term on the right side of (11), which is expressed in an impedance divider format, approaches unity. The limiting low frequency of the differential-mode gain, which is given by (11), is R_2/R_1. As the frequency increases, the open-loop gain declines, but $Z_{\mathrm{cl,o}}$ increases. The factor of the impedance divider in the differential-mode gain expression of (11) becomes less than one. An explicit pole introduced by the capacitive load C_L is important in the drop of the magnitude of the differential-mode gain with increasing frequency. This pole may dominate the high-frequency response when the amplifier is used to drive a heavy capacitive load. At a high frequency, the impedance of C_L declines and acts as a shunt between the output and ground. The differential-mode gain tends toward zero. The expression for the transfer function of the differential-mode gain is a second-order low-pass response, which is given by (13). The damping ratio in (15) characterizes the transient response of the two-pole amplifier. For a very low damping ratio, the response is oscillatory, whereas for a large damping ratio, the response does not oscillate. The desired performance depends on the value of the isolation resistor; a larger isolation resistor corresponds to a more damped pulse response.

B. Differential-Mode Gain in Multicell Amplifier

Equation (7) in the previous analysis reveals that the overall differential-mode gain is the sum of the individual cells of gain factors, i.e.,

$$A_{\mathrm{tot,d}}(s) = \sum_{k=1}^{i}\left(A_{\mathrm{cl,d,p}}^{(k)}(s) + A_{\mathrm{cl,d,n}}^{(k)}(s)\right)A_{\mathrm{iso,d}}^{(k)}(s). \quad (16)$$

The pole introduced by the isolation amplifier is assumed to be a low-frequency dominant pole, such that the poles of the difference amplifiers are far apart, and the isolation amplifier dominates the corner frequency of the overall differential-mode gain. As the overall gain is increased by increasing the number of cells of floating signal modules, the bandwidth is kept constant, and the gain–bandwidth product multiplied by the number of cells. Tradeoffs must be made between the gain and the bandwidth in the design of a floating single module. As the output swing of the difference amplifier increases, both the cells of the multicell amplifier used to reach the desired output swing and the corner frequency drop. The multicell amplifier can effectively operate with fewer cells when the

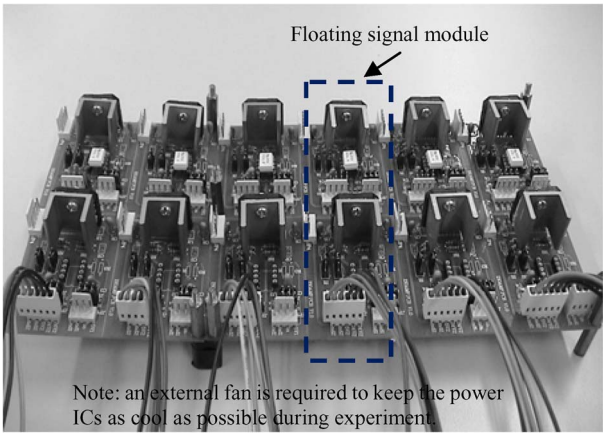

Fig. 4. Experimental setup.

TABLE I
MULTICELL LINEAR POWER AMPLIFIER SPECIFICATION

Multi-Cell Amplifier	Output Voltage	±200 V
	Maximum Output Current	±2.5 A
	Capacitive Load	0~0.1uF
	Number of Cells	6
	Isolated Power Supply Voltage	±24V
	Bandwidth	100kHz
Isolation Amplifier (IC: HCPL7800)	Input Voltage Swing	±200mV
	Gain	8
	Bandwidth	100kHz
Difference Amplifier (IC: LM4700)	Maximum Supply Voltage	±33V
	Output Dissipation	30W
	Maximum Output Current	2.9A
	Gain-Bandwidth Product	7.5MHz
	Open-Loop Gain	110dB
	Closed-Loop Gain(Resistor Ratio)	11
	Slew Rate	18V/μs

floating single module provides a higher voltage gain. The two poles introduced by capacitive loading and the difference amplifier gain move toward the dominant pole of the isolation amplifier and reduce the bandwidth as the gain factor increases. Evaluating the overall bandwidth requirement and preserving signal integrity during amplification are critical to design. The benefit of reducing the cell greatly outweighs the disadvantage of reducing the bandwidth.

IV. SIMULATIONS AND EXPERIMENTAL RESULTS

The practicality and performance of the previously described modular implementation concepts were experimentally confirmed using six floating signal modules, which were interconnected in a cascaded six-cell amplifier.

A. Experimental Layout

Fig. 4 displays a photograph of the experimental setup. Table I presents abbreviated data for the prototype amplifier. HCPL-7800 is a fixed-gain isolation amplifier that electrically isolates input and output signals. The full-power bandwidth associated with the slew rate is about 1.85 MHz. The maximum output current is approximately ±2.5 A for power supply

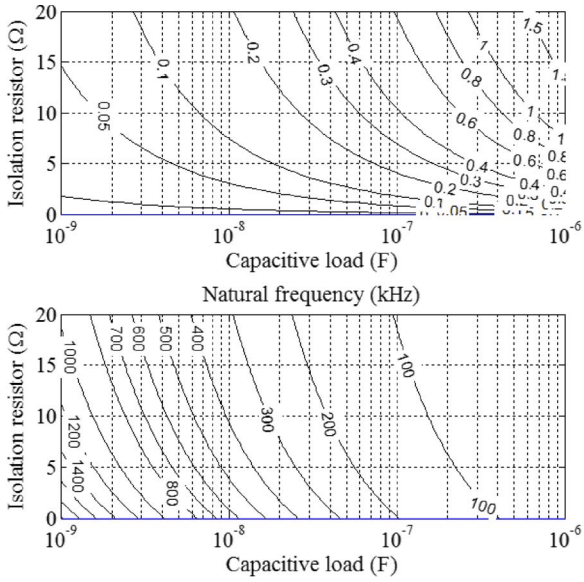

Fig. 5. Contour plots of the damping ratio and nature frequency.

voltages of ±20 V. The input signal of the power amplifier in the floating signal module is varied between +1.6 and −1.6 V. The maximum possible output swing of the difference amplifier is a function of the resistor ratio R_2/R_1 when the equal ratios R_4/R_3 and R_2/R_1 are determined. The output saturation that generates large distortion in linear applications must be prevented by adjusting the feedback gain using a resistor ratio R_2/R_1 of 11. When the input voltage is ±200 mV, the output swing of the six-cell amplifier may reach ±200 V, which is the design value.

Fig. 5 plots the simulated results. The figure has two contour plots of the damping ratio ξ and the natural frequency ω_n as functions of two independent variables—capacitive load and isolation resistance. The following parameters are used: $R_o = 6\ \Omega$, $R_2/R_1 = 11$, and $A_{\mathrm{o,d}}(0)\omega_{\mathrm{o,d}} = 1.85$ MHz. The isolines correspond to constant damping ratios and natural frequencies given by (14) and (15). The two contour plots indicate that the damping ratio increases with the capacitive load and the isolation resistance, but the natural frequency declines. The required isolation resistance mainly depends on the output impedance of the amplifier; values from 5 to 50 Ω typically suffice to prevent local resonances [22], [23].

The isolation resistance may increase the dissipation of the reactive energy. When the load is driven by a sinusoidal signal, the energy stored in the capacitor during the first half of the cycle is returned to the amplifier during the second half of the cycle as heat. The output signal will slightly be attenuated in a manner determined by the ratio of the isolation resistance to the total output resistance. A larger isolation resistance can dissipate more reactive energy in the output capacitive load, such that the op-amp output is more stable. However, a smaller resistance corresponds to lower gain attenuation. An isolation resistor with a moderate resistance of 10 Ω is adopted as a compromise among large local resonance, high stability, and low gain attenuation. Therefore, the contour plot in Fig. 5 reveals that the damping ratio is about 0.4 at a capacitive load of 0.1 μF, which is also satisfactory.

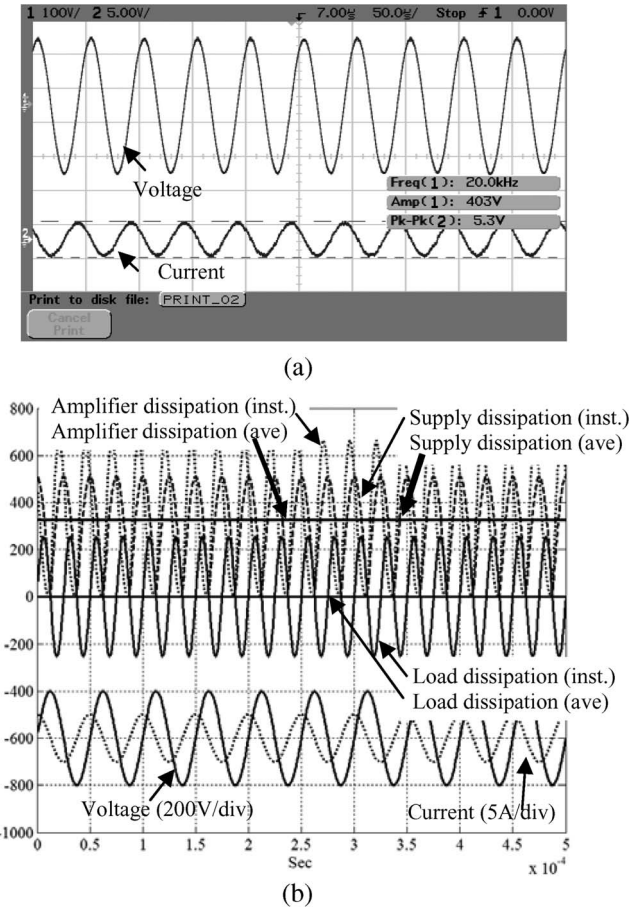

Fig. 6. Six-cell amplifier due to a 20-kHz sinusoidal input signal. (a) Time response. (b) Power dissipation.

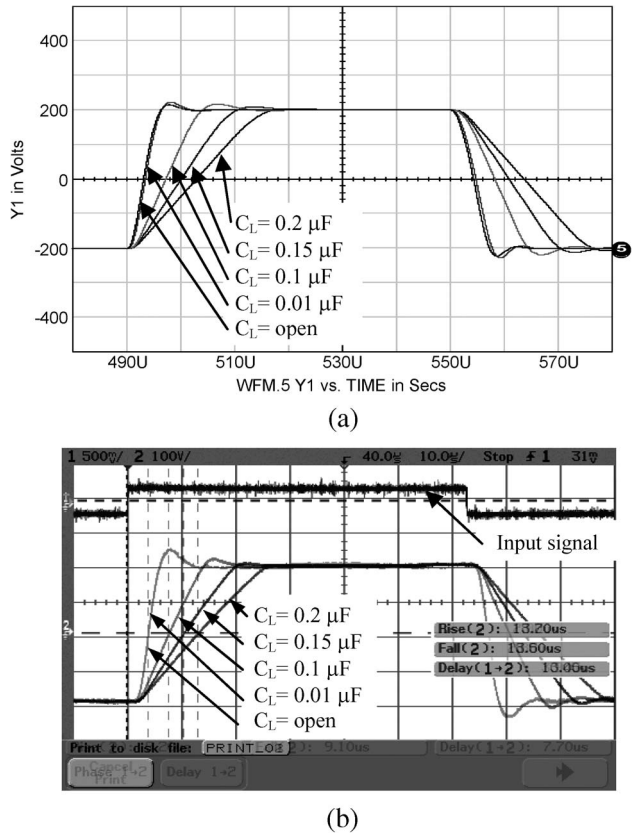

Fig. 7. Rise and fall times of the six-cell amplifier under various capacitive loads. (a) IsSpice analysis results. (b) Experimental results.

TABLE II
RESPONSE ESTIMATES

CL	Rise Time	Fall Time	Slew Rate
0.20μF	18.2 ms	18.5 ms	17.6 V/ms
0.15μF	13.7 ms	13.6 ms	23.3 V/ms
0.10μF	9.2 ms	9.1 ms	34.7 V/ms
0.01μF	2.9 ms	2.8 ms	110 V/ms
Open	2.8 ms	2.7 ms	115 V/ms

B. Time-Domain Response

Fig. 6 plots the time-domain response of the multicell amplifier excited by a sinusoidal wave signal of 20 kHz with a floating output of ±200 V across the 0.1-μF capacitive load. The output current requirement is

$$I_{\text{out}} = 2\pi f_{\max} V C_L = 2\pi(20\text{e}3)(\pm 200)(0.1\text{e}-6) = \pm 2.51 \text{ A}. \quad (17)$$

The figure reveals that the output peak-to-peak current in the experiment is approximately 5.3 A. The maximum power dissipation requirement [24] is

$$P_{\text{ave,max}} = 4V_s^2 f_{\max} C_L = 4(200)^2(20\text{e}3)(0.1\text{e}-6) = 326.6 \text{ W}. \quad (18)$$

Fig. 6(b) presents the simulation results of the power dissipation analysis. Solid, dashed, and dotted curves represent the powers that are instantaneously delivered from the amplifier to the load, from the supply unit to the amplifier, and dissipated from the amplifier, respectively. The portion of reactive power flow that is associated with the pure capacitive load returns to the amplifier in each cycle. The reactive power averaged over a complete cycle of the ac waveform is zero. The mean power dissipation requirement of an amplifier, which is the difference between the power delivered from the supply unit and that delivered to the load, is 326.6 W. This 326.6 W of dissipated power has nothing to do with mechanical work. It is merely wasted in the electronics as heat.

Fig. 7 plots a typical pulse response for various capacitive loads. The curve marked "C_L = open" is the response when the capacitive load C_L is neglected; the curve marked with capacitive values plots the circuit response if the amplifier is adopted with a capacitive load connected to its output. Most power amplifiers cannot easily drive highly capacitive loads very effectively, and attempting the same normally causes oscillations or ringing on the square-wave response. The $C_L \leq 0.1$ μF curves exhibit slight peaking. This peaking is caused by a large input signal at a high frequency that exceeds the slew rate of the output amplifier. The time-response characteristics are almost identical when the capacitive loads are less than 0.01 μF. Table II lists the rise and fall times for various capacitive loads. These times are based on the current that the output stage can deliver or sink. The slew rates measured from 10%

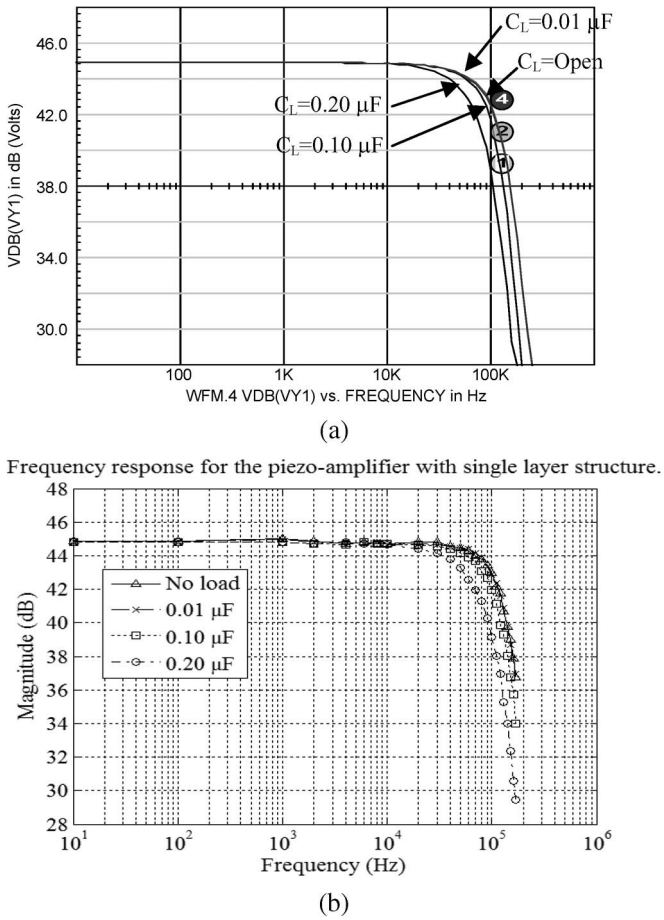

Fig. 8. Frequency response of the piezoelectric amplifier with a single cell. (a) IsSpice analysis results. (b) Experimental results.

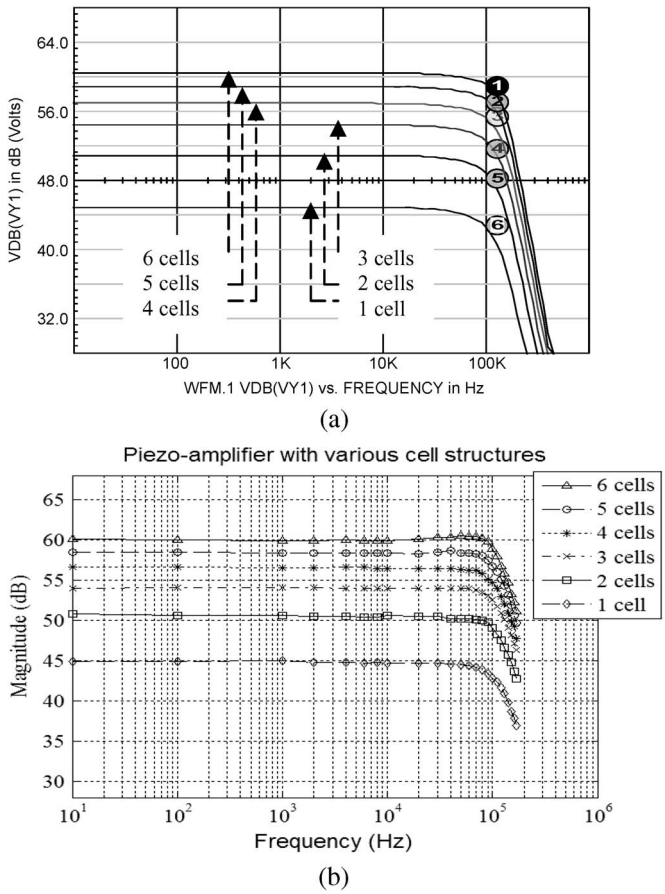

Fig. 9. Frequency response of the piezoelectric amplifier with different cells. (a) IsSpice analysis results. (b) Experimental results.

to 90% of the full-scale voltage swing is controlled by the current available to charge and discharge a high-impedance node capacitor. The experiment and IsSpice simulation yield closely matching results.

C. Frequency-Domain Response

Fig. 8 plots the frequency responses of a floating signal module, which were determined by the IsSpice analysis and experimentally obtained for four values of capacitive loads. The results show that the corner frequency is on the order of 100 kHz. The three curves for capacitive loads of 0.1 μF, 0.01 μF, and open conditions are fairly close together and roll off at -40 dB/dec, indicating that the response involves more than one pole. As the capacitive load increases to $C_L = 0.2\ \mu$F, the output impedance at a high frequency declines; the corner frequency drastically declines, and the slope becomes steeper than -40 dB/dec. Two dominant poles are present near the corner frequency of 100 kHz in the circuit. Therefore, the signals change from a flat response to an about -40 dB/dec drop in gain. The first pole is on the isolation amplifier, and the second pole is on the difference amplifier. The corner frequency of the isolation amplifier presented in the data sheet is 100 kHz. The LM4700 op-amp with a gain–bandwidth product of 7.5 MHz is connected in the difference amplifier configuration with a low-frequency closed-loop gain of 11. The corner frequency given by the gain–bandwidth product rule is about 681 kHz. The full-power bandwidth (FPBW) is the maximum frequency over which the output can dynamically swing without significant distortion. At a lower frequency, the FPBW is limited by the output swing of the amplifier; at a higher frequency, the response is limited by the slew rate of the amplifier. The LM4700 slew rate is $\mathrm{SR} = 18\ \mu\mathrm{s/V}$, and the desired peak output voltage is $V_{\mathrm{op}} = 17$ V. The FPBW based on the slew rate limitation is $\mathrm{SR}/(2\pi V_{\mathrm{op}}) = 168.52$ kHz, which is much smaller than the bandwidth under small-signal nonslew rate-limiting conditions and is close to 100 kHz. The analysis favorably compares with the experimental results. When the capacitive load exceeds 0.1 μF, the bandwidth is no longer determined by the internal op-amp, but rather than by the external capacitive load. Additionally, the pole introduced by the capacitive load dominates the frequency response. The corner frequency obtained by the time constant associated with the isolation resistance and capacitive load is approximately 99 kHz, which exceeds the value presented in Fig. 8. The low-frequency differential-mode gain is about 44.9 dB, which agrees with experimental results.

Fig. 9 displays a Bode plot of the voltage gains of the multicell amplifier, accounting for the stack cells. The capacitive load is 0.01 μF. These curves show that the overall gain increases with the floating signal modules. The multicell amplifier has a fixed bandwidth that is close to 100 kHz. The slope of the rolloff at a high frequency is -40 dB/dec, which was theoretically

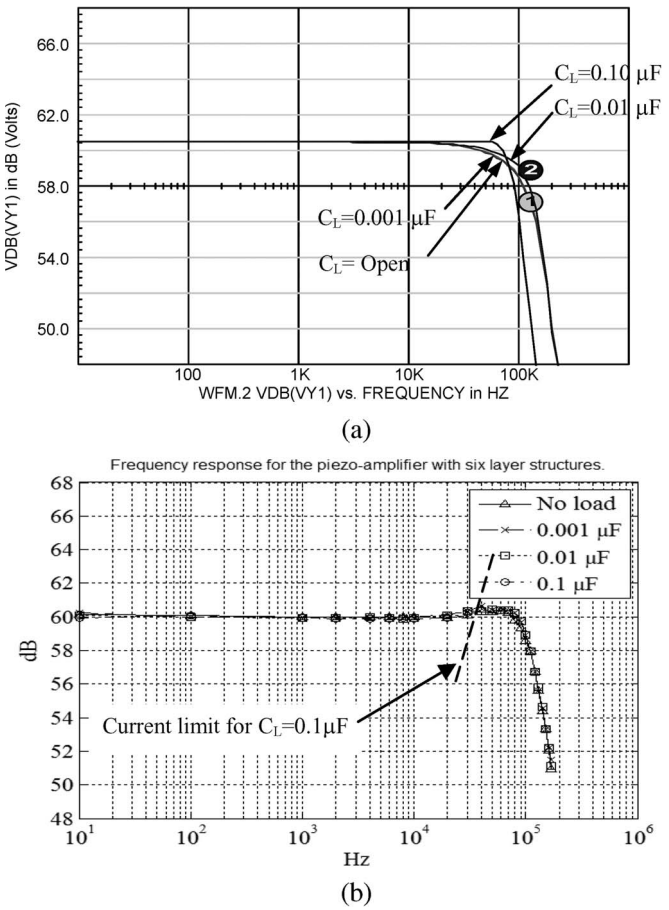

Fig. 10. Frequency response of the piezoelectric amplifier with six cells. (a) IsSpice analysis results. (b) Experimental results.

predicted. The experimental result demonstrates that the low-frequency gain is approximately 60 dB, which is slightly lower than the simulated result of 61 dB. The common-mode effect or the parameter tolerances among discrete components may explain the aforementioned gain loss. Fig. 10 presents a Bode plot of the voltage gains of the six-cell amplifier versus the capacitive load. The amplifier provides a maximum peak-to-peak current of 5 A. When a capacitive load of 0.1 μF is driven and reasonable power is maintained in each module, the maximum allowable frequency that corresponds to the maximum peak-to-peak current is about 20 kHz. As the capacitive load increases, more peaking is observed. These curves reveal that this capacitance would dominate the circuit response if a capacitor load of 0.1 μF or higher were connected to the output. The simulation results demonstrate this hypothesis.

D. Isolated Power Supply Unit

The advantage of the multicell configuration is its capacity to divide the total power dissipation among cells, because each cell amplifier provides the same loading current. Six isolated supply units that feed the individual floating signal module cell are adopted in the prototype amplifier setup. An extra amount of leakage current caused by the primary-to-secondary capacitances of the isolated power units increases the power dissipated by individual amplifier cells. Line filter safety capacitors

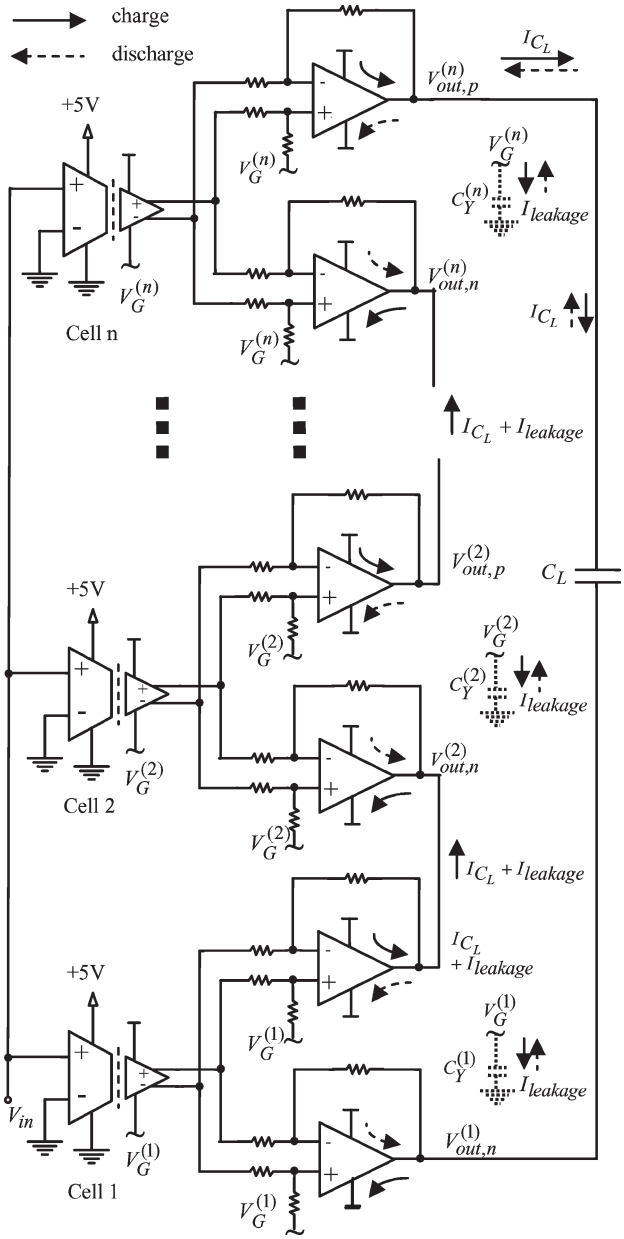

Fig. 11. Leakage currents due to the primary-to-second capacitances of the isolated power supply units.

(or an ac interference suppression capacitor), which improve the reliability, safety, and performance of the power supply unit, are important in the multicell circuit. Type-Y safety capacitors are typically adopted between the ac line and ground, between the ac neutral and ground, and between the primary and secondary circuits. Y capacitors directly contribute to increasing the total leakage current in the ground lead. When the input signal is positive, the output current flows from the noninverting amplifier of the $(i-1)$th cell to the inverting amplifier of the ith cell, as presented in Fig. 11. The ground potential of the ith cell of the isolated power supply unit has a positive voltage of $V_{\mathrm{out,p}}^{(i-1)} - V_{\mathrm{out,n}}^{(i)}$ above the ground potential of the $(i-1)$th cell. The safety capacitor Y, with capacitance $C_Y^{(i)}$, is charged and discharged as a bipolar input signal is applied, adding to the output loads of the inverting amplifier of the ith cell and the noninverting amplifier of the $(i-1)$th cell. The leakage

currents are proportional to the driving frequency and occur in the internal cells. The topmost noninverting amplifier in the nth cell and the bottommost inverting amplifier in the first cell are unaffected because the output currents directly flow into the external load. The surplus power dissipated because of leakage currents increases the temperature of ICs. These leakage currents can be reduced by introducing a low capacitive input/output coupling or inserting a common-mode choke into the output of the switch-mode power supply unit [11].

V. Conclusion

Multicell amplifiers can be realized using low-voltage, high-current, and high-power MOSFET devices or costly IC power amplifiers to achieve high output power. The multicell topology enables the output voltage of the piezoelectric amplifier to be increased while maintaining the module's output swing limits. The multicell portion divides the total power dissipation among all of the modules, such that the higher system output power of each module does not exceed its individual power dissipation capacity. As compared to the achievable technical specifications, the realization effort and production cost are comparatively low. The drawback of the multicell circuit topology is that many isolated switching-mode power supply units are required to feed the individual cell of power. In applications that involve driving capacitive loads, the peak output current of the amplifier limits the useful bandwidth of the amplifier. The maximum capacitive load depends on both the slew rate of the amplifier and the maximum output current. The isolation resistance increases the damping ratio and reduces the output ringing. The experimental data presented herein correspond to an adjustment for a capacitive load of 0.1 μF. The advantages of the multicell amplifier include the approximately constant corner frequency and the high common-mode rejection ratio, which offer the accuracy and linearity required for piezoelectric applications. Strong electrical isolation keeps high voltages away from equipment and reduces the risk of electrical shock. The feasibility and reliability of the amplifier were demonstrated both experimentally and by simulation.

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