

determined by the 3-dB AR, is about 540 MHz or 20.8% (2.33–2.87 GHz) and 480 MHz or 19.6% (2.21–2.69 GHz) with minimum AR of 0.87 dB at 2.6 GHz and 0.88 dB at 2.45 GHz, respectively, for  $L_t = 0$  and  $L_t = 19$  mm. Both of the CP bandwidths are larger than 19%. It is evident that the length of the protruded metallic strips has larger effect on the port isolation level, but has less effect on the CP bandwidth. As for the antenna with  $L_t = 19$  mm, both impedance matching (referred to 10 dB return loss) and low coupling level (referred to 20 dB isolation) are achieved within the CP operating band.

Figure 4 shows the measured far-field radiation patterns of the antenna with length of  $L_t = 19$  mm at 2.45 GHz in the LHCP and RHCP operation. It is observed that the cross-polarization levels are about 26 dB in the broadside direction in both states. The maximum radiation direction of the antenna displaces a little from the  $z$ -axis. It should be noted that the backside radiation pattern is a mirror image of the front pattern, and the polarization senses of both sides are opposite to each other. The antenna radiates almost the same amount of energy into both sides.

#### 4. CONCLUSION

A novel design of broadband dual CP square slot antenna has been investigated and successfully implemented. Two orthogonal modes of the proposed antenna are excited in series through the coupling between the T-junction and the T-shaped strip. By loading the four metallic strips at the slot corners, high port isolation level is achieved. The measured 3-dB AR bandwidth is 480 MHz or 19.6% and the isolation between two ports is better than 20 dB over the band. The proposed antenna has excellent dual CP characteristics and is suitable for polarization diversity operation.

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## 11.8 GHZ GAINP/GAAS HBT DYNAMIC FREQUENCY DIVIDER USING HLO-FF TECHNIQUE

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**ABSTRACT:** An integrated GaInP/GaAs heterojunction bipolar transistor (HBT) dynamic frequency divider based on HLO-FF (high-speed latching operating flip-flop) structure is demonstrated at 4.1–11.8 GHz. In this experiment, a conventional static frequency divider using the same cut-off-frequency device is also fabricated for comparison. By biasing the HBT transistors around the peak of  $f_T$  and optimizing the  $I_{read}/I_{latch}$  ratio, the maximum operating frequency of the HLO-FF is greatly improved due to higher slew-rate and smaller voltage swing. The speed of HLO-FF is faster about 48% than that of static structure. The core current is 13 mA at the supply voltage of 5 V. © 2008 Wiley Periodicals, Inc. *Microwave Opt Technol Lett* 50: 2642–2645, 2008; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.23740

**Key words:** frequency divider; GaInP/GaAs HBT; emitter coupled logic; static; HLO-FF

#### 1. INTRODUCTION

Recently, the personal wireless communication system is growing rapidly. The faster and accurate frequency synthesizer or phase-locked loops (PLL) system are required at the transceiver for more efficient usage of finite channels. A frequency divider plays an important role because it dominates the maximum operating frequency and power consumption of the frequency synthesizer or PLL system. In General, the static divider is already used in all kinds of applications, and its performance is also a benchmark for semiconductor processes [1, 2]. However, the fundamental physics properties of the devices,  $f_T$  and  $f_{max}$ , usually limit the maximum operating frequency of a static divider. Thus, intensive efforts are under way to improve the circuit structures and overcome the inherent limitations of device, such as HLO-FF [3, 4] and superdynamic structure [5–9].

In this work, a HLO-FF frequency divider is implemented in 2  $\mu\text{m}$  GaInP/GaAs HBT ( $f_T = 35$  GHz) technology, and another static frequency divider is also realized for comparison. The maximum operating frequency of a D-type Flip-Flop (D-FF) can be optimized by reducing voltage swing and increasing current density, simultaneously. However, the speed of D-FF can not be improved by only reducing latch-current for smaller voltage swing when the operating frequency is closed to the fastest speed. The related design issues and phenomena will be discussed and proven in this experiment.

The GaInP/GaAs HBT technology with the accurate 50- $\Omega$  sheet thin-film resistors and 0.36  $\text{fF}/\mu\text{m}^2$   $\text{Si}_3\text{N}_4$  MIM capacitors has less process variation. The semi-insulating GaAs substrate and low-base resistance can reduce the substrate loss, parasitic effect, and noise-immunity degradation, especially under the lower swing operation. Meanwhile, the GaInP/GaAs HBT ECL (emitter-couple logic), which can make current fully commutate in the several threshold voltage, is a great benefit to the high-speed and low-sensitivity design. The circuit design of HLO-FF frequency divider is included in the next section. Section 3 describes the circuit fabrication and performances.

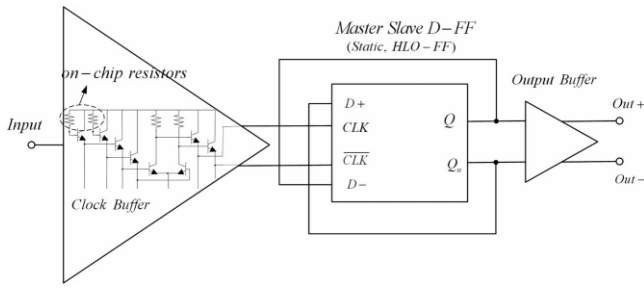


Figure 1 Block Diagram of the divide-by-two frequency divider

## 2. CIRCUIT DESIGN

The divide-by-two frequency divider is composed of a single-to-differential clock buffer, a D-type flip-flop and an output buffer, as shown in Figure 1. The D-type flip-flop is cascade by two-stage bi-level (series-gated) D-latch, which senses data and clock input simultaneously. For the divide-by-two function, the slave output is cross-connected to the master input. Every D-latch is composed of the differential pair and the cross-coupled regenerative pair. For the purpose of high-speed and low input sensitivity, emitter-couple logic (ECL) topology is employed. When signal swing is higher than  $4V_T$ , an ECL can provide the voltage gain more than 1, and easily differentiate logic levels.

As illustrated in Figure 2, the dash and solid lines indicate the current directions of the static and HLO-FF structures, respectively. In HLO-FF structure, the current paths of latch pairs are separated from that of read pairs. Latch current are usually chosen from one-half to one-third of the read current. During the latching period, the low logic-level is pre-pulled to  $V_{CC} - I_{latch} \times R_L$ . The smaller voltage-swing makes the cross-point of the differential signal shift forward about  $\Delta t$  in the next read-period, as illustrated in Figure 3(a). The shorter transitional period implies that the operating frequency can be prompted. Therefore, the HLO-FF can operate at the higher frequency.

Since the speed of the clock pair is twice as high as the other pairs, the current density will be biased at the peak of cut-off frequency ( $f_T$ ). The sizes of read ( $Q_3-Q_4$ ) and latch ( $Q_5-Q_6$ ) transistors are chosen as the half of clock pair. It not only reduces the output capacitance contributed by latch pairs [5], but also keeps read pairs operating near the peak of  $f_T$ . For the specified output swing, the value of  $R_L$  must be reduced as the increasing  $I_{read}$ . The storage ability of the latch pairs becomes weak unless the latch

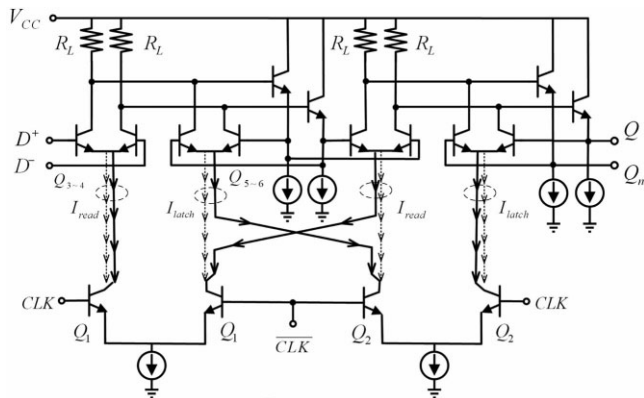


Figure 2 Schematic of the Static and HLO-FF D-type flip-flops. ----- Current path of the Static type ( $I_{latch} = I_{read}$ ), \_\_\_\_\_ Current path of the HLO-FF type ( $I_{latch} < I_{read}$ )

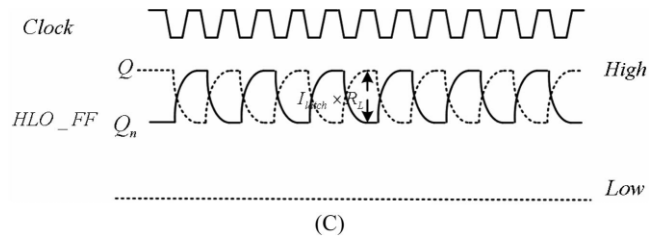
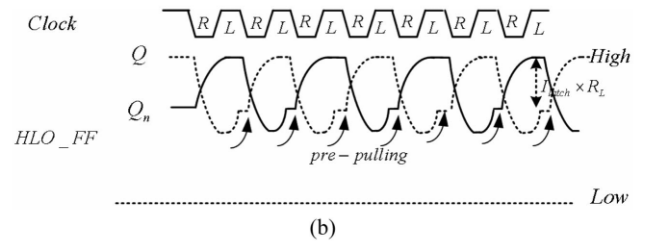
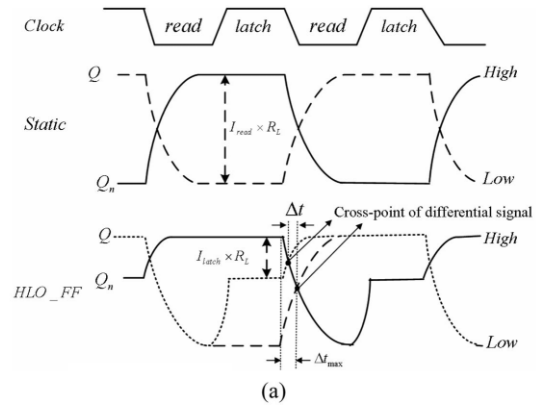
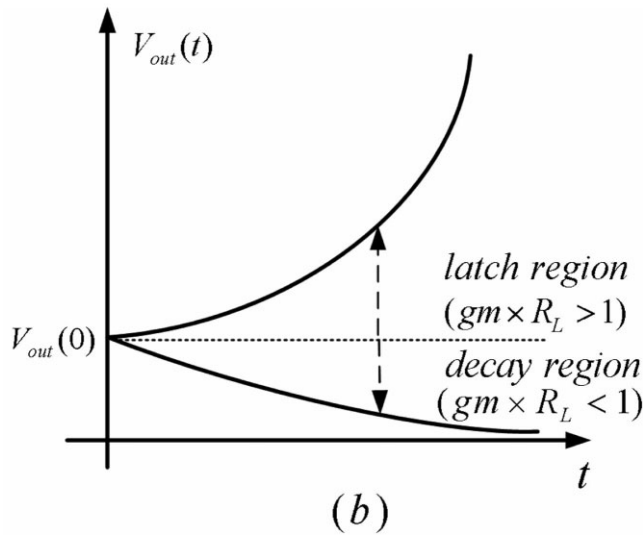
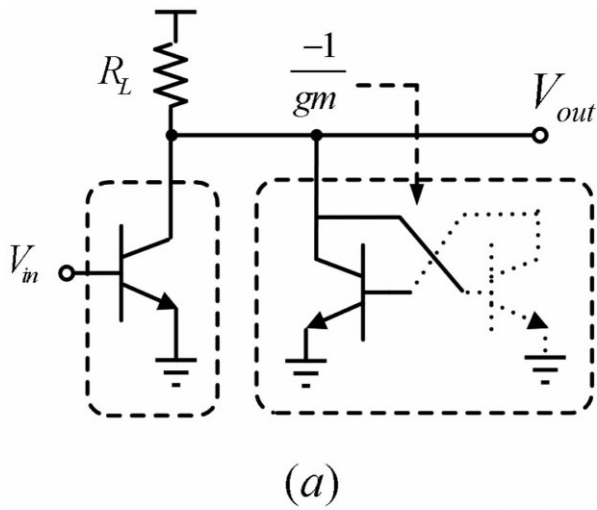


Figure 3 The timing diagrams of the Static and HLO-FF D-type flip-flops at (a) low-frequency, (b) high-frequency and (c) nearly maximum operating frequency

current is raised to compensate the smaller cross-loop gain caused by the decreasing of  $R_L$ . Figure 4 shows the D-latch half-circuit and its output resistance of  $R_L/(1-gm \times R_L)$ . If the negative transconductance ( $-gm$ ) of the latch pair is larger than positive conductance ( $1/R_L$ ), the initial logic level can be amplified and then stored. It also implies that  $I_{latch}$  must be larger than  $V_T/R_L$ , otherwise the latch pair fails to store the logic level, as illustrated in Figure 4(b).

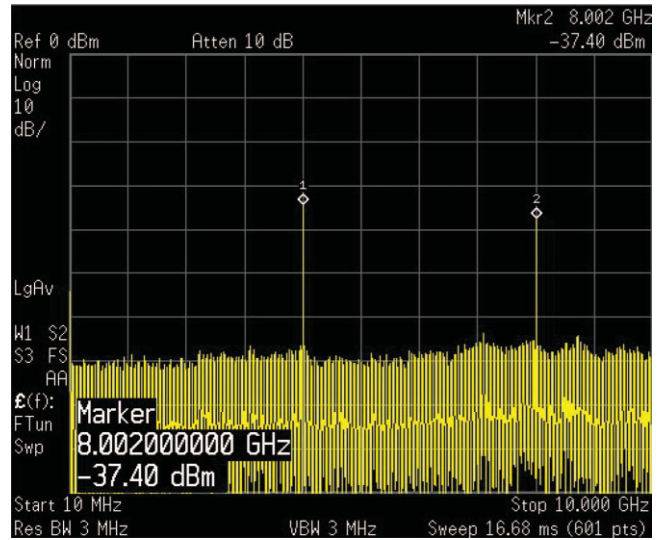
In Figure 3(b), the logic level in the read-period does not reach full voltage swing at higher frequency due to the finite slew-rate. When operating near the maximum frequency, the voltage swing will be like the waveform of Figure 3(c). Except smaller voltage swing, it is similar to the condition of static structure. If boosting operation to much higher frequency, voltage-swing and slew-rate are still the keys of design issue. The former has a limitation in maximum shifting amount of cross-point,  $\Delta t_{max}$ , which occurs under zero latch-current. But, the behavior of the HLO-FF gradually becomes more dynamic, so as to make the bandwidth-ratio narrower. On the other hand, the speed of HLO-FF will be limited under the voltage swing,  $I_{latch} \times R_L$ , unless the slew-rate is increased to obtain shorter transition-time again. The highest slew-rate of HBT depends on whether the HBT is biased at maximum  $f_T$  or not, especially the transistors of read or clock pairs. Briefly, there exists an optimization ratio of  $I_{latch}/I_{read}$  between the speed and bandwidth ratio under the specified voltage swing.



**Figure 4** (a) A half-circuit of the read and latch pairs and (b) the trend of the latch machine

### 3. MEASUREMENT RESULTS

For comparison, the static and HLO-FF frequency dividers are simultaneously fabricated in  $2\ \mu\text{m}$  GaInP/GaAs HBT technology, whose peak value of  $f_T$  is around 35 GHz. Although the transistors

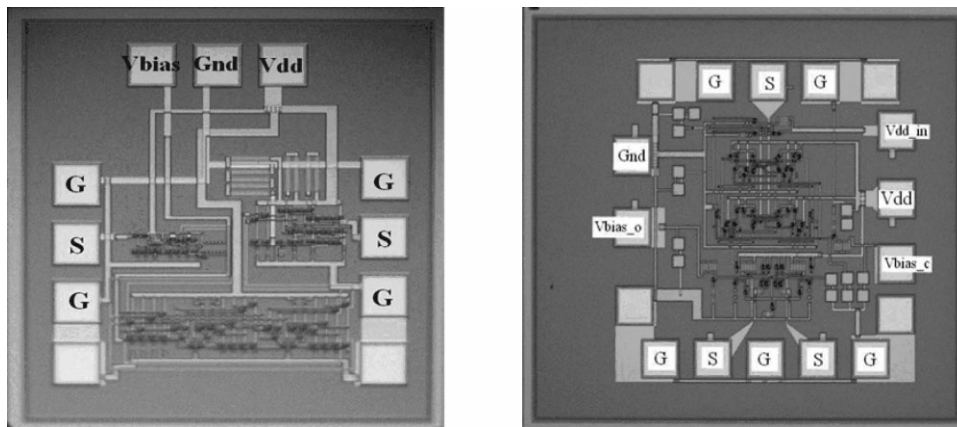


**Figure 6** Measured output spectrum of the Static frequency divider with the maximum frequency of 8.0 GHz. [Color figure can be viewed in the online issue, which is available at [www.interscience.wiley.com](http://www.interscience.wiley.com)]

of read and clk pairs are biased near maximum  $f_T$ , these must avoid entering the high current density region, where small-signal current gain and  $f_T$  will be reduced due to Kirk-effect. Figure 5 shows die photos of GaInP/GaAs HBT Static and HLO-FF frequency dividers, whose sizes including probing pads are  $0.85 \times 0.83\ \text{mm}^2$  and  $0.77 \times 0.75\ \text{mm}^2$ , respectively.

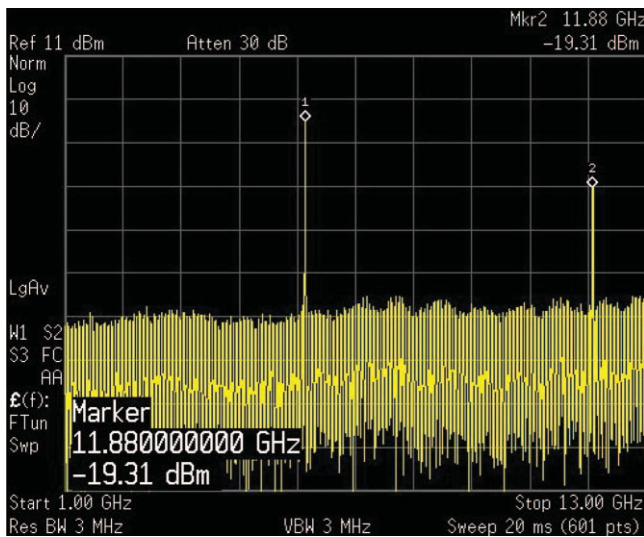
In HLO-FF core circuit, the emitter size of the clock transistors,  $Q_1$ , with the double of read current is chosen as  $2 \times 4\ \mu\text{m}^2$ . The other HBT devices,  $Q_2$ – $Q_6$ , used in the D-type flip-flop are  $2 \times 2\ \mu\text{m}^2$ . At the supply voltage of 5 V, the transistors  $Q_1$ ,  $Q_2$  and read pairs with 0.278, 0.297, and 0.275  $\text{mA}/\mu\text{m}^2$  operate near the peak of  $f_T$ . As the ratio of  $I_{\text{latch}}/I_{\text{read}}$  is reduced to 0.53, the operating frequency of the HLO-FF frequency divider is up to 11.8 GHz.

However, the size of all transistors in static D-FF is  $2 \times 4\ \mu\text{m}^2$ . The maximum frequency is only 8 GHz because of extra capacitance contributed by larger latch transistors, lower current density in read-pairs, and higher voltage-swing during latching period. Their spectrums at maximum operating frequency are shown in Figures 6 and 7, respectively. The speed of the HLO-FF structure is obviously faster than that of static



**Figure 5** Die photos of the Static (left) and HLO-FF (right) D-type frequency dividers





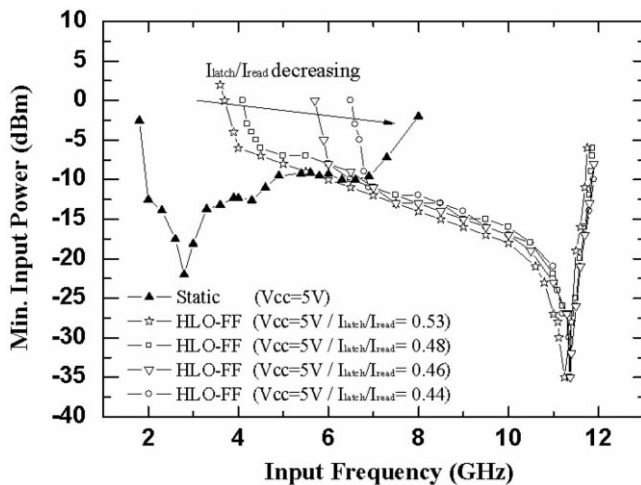
**Figure 7** Measured output spectrum of the HLO-FF frequency divider with the maximum frequency of 11.8 GHz. [Color figure can be viewed in the online issue, which is available at [www.interscience.wiley.com](http://www.interscience.wiley.com)]

structure at the cost of fewer low-frequency operating range. The core circuits of the static and HLO-FF frequency dividers consume 12.1 and 13 mA at the supply voltage of 5 V, respectively. Figure 8 shows the measured input sensitivity. The HLO-FF and static frequency dividers operate from 4.1 to 11.8 GHz and from 1.8 to 8 GHz, respectively. The improved amount of maximum frequency is increased to 48%.

Another interesting phoneme is that low-frequency boundary is shrunk quickly when reducing  $I_{latch}/I_{read}$  ratio. But, maximum frequency is merely raised about 150 MHz. The latter means that the forward shifting of cross-point by reducing  $I_{latch}$  is almost close to  $\Delta t_{max}$ , and reaches the limit of speed. If requiring higher-speed operation, it is not enough to only reduce  $I_{latch}$  for smaller voltage-swing without considering size ratio and technology limitation.

#### 4. CONCLUSION

This article describes the design and performance of the dynamic frequency divider based on HLO-FF structure in the 2  $\mu\text{m}$  GaInP/GaAs HBT technology. By basing current density and reducing



**Figure 8** Measured sensitivity of the GaInP/GaAs HBT Static and HLO-FF frequency dividers

latching voltage swing, the operating frequency of divide-by-two function is from 4.1 to 11.8 GHz under the optimized  $I_{latch}/I_{read}$  of 0.53 and the supply voltage of 5 V. On the other hand, the static frequency divider using identical HBT only operates up to 8 GHz. As the compared results, HLO-FF is greatly faster than static structure, and the improved amount of maximum frequency can be up to 48%.

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