Improvement of Resistive Switching Characteristics in $SrZrO_3$ Thin Films With Embedded Cr Layer

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***Abstract*—The stabilization of the resistive switching properties is necessary to realize the memory application of the $SrZrO_3$(SZO)-based resistive switching devices. During continuous resistive switching cycle, broad variations of the resistive switching parameters of the SZO-based memory devices can be improved by a thin embedded Cr layer. The Cr metal layer is proposed to diffuse into and dope the SZO thin film to produce the space charge region, further reducing the effective resistive switching region. Hence, the good stabilization of the resistive switching properties can be obtained in the SZO films with embedded Cr layer.**

***Index Terms*—Nonvolatile memory (NVM), resistive random access memory (RRAM), resistive switching, stabilization, $SrZrO_3$.**

I. INTRODUCTION

NEXT-GENERATION nonvolatile memories (NVMs), such as ferroelectric random access memory, magnetic random access memory, and resistive random access memory (RRAM), are being developed due to the scaling limitations of the current Flash memory. Among them, RRAM utilizes different resistance values to store the digital data and has the merits of low-power consumption, simple-stack structure, high-speed operation, and high-density integration, which is a promising candidate for future commercial application.

Resistive switching phenomena in binary metal oxides and perovskite materials are observed including NiO, TiO_2, Nb_2O_5, Ta_2O_5, ZrO_2, Al_2O_3, Cu_2O, $SrZrO_3$(SZO), $SrTiO_3$, $La_{0.7}Ca_{0.3}MnO_3$, and $Pr_{0.7}Ca_{0.3}MnO_3$ [1]–[19]. During the successive resistive switching, however, the resistance values of ON-state (R_{ON}) and OFF-state (R_{OFF}), and the required voltages to switch into OFF-state (V_{OFF}) and vice versa (V_{ON}) are fluctuating, which might lead to severe control and readout hazards after a long-term operation. Many methods have been proposed for the binary metal oxides to suppress the variations, such as reducing the active device area by plug-bottom electrode [3], inserting IrO_2 buffer layer to stabilize the local oxygen migrations [4], creating the locally strong electric field by process control [5], reducing the effective film thickness by Ni migration [6], and modifying the resistive switching characteristics by Ti top electrode [16], [17]. As for the perovskite materials in RRAM application, the resistive switching variations are presented as well [15], however, there is no study reported about how to solve this problem.

A novel and simple method is proposed to modify the resistive switching properties by inserting an embedded Cr metal in the middle of the SZO films. By introducing an embedded Cr metal layer within the SZO thin films, the improved stabilization of the resistive switching characteristics and the related conduction mechanism are investigated in this letter.

II. EXPERIMENT

The detailed fabrication process of $LaNiO_3$(LNO)/Pt/Ti/SiO_2/Si substrates was reported in our previous study [15], and the SZO thin films used here are fabricated by the sol–gel method. The stoichiometric amount of the initial materials including strontium acetate (ALDRICH, 99.995%) and zirconium n-propoxide (ALDRICH 70 wt.% solution in 1-propanol) was dissolved in acetic acid (FLUKA, 99.8%) and acetylacetone (FLUKA, 99.5%). Acetic acid was used as solvent and heated at 80 °C for 10 min to remove the water. Then, the strontium acetate was added into the acetic acid. After being stirred at 80 °C for 30 min, the mixture dissolves in the solvent. Subsequently, the acetylacetone and the zirconium n-propoxide were added into the above solution, which was further stirred at 80 °C for 60 min. The prepared 0.1-M precursor solution was spin-coated on the LNO/Pt/Ti/SiO_2/Si substrates to form the SZO film. After baked at 125 °C for 10 min, the as-deposited layer was heated at 200 °C for 10 min and then annealed at 400 °C for 30 min. The above steps were repeated to control the film thickness. To embed the Cr metal layer within the SZO-based device, three sequential layers of SZO/Cr/SZO (where the Cr layer was deposited by e-beam evaporation) with the thicknesses of 20/5/20 nm, respectively, were fabricated on the LNO/Pt/Ti/SiO_2/Si substrates. Postannealing process was carried out at 600 °C in O_2 ambient for 60 s. Finally, a 300-nm-thick Al top electrode (with the diameter of 250 μm defined by the metal mask) was evaporated to complete the SZO-based

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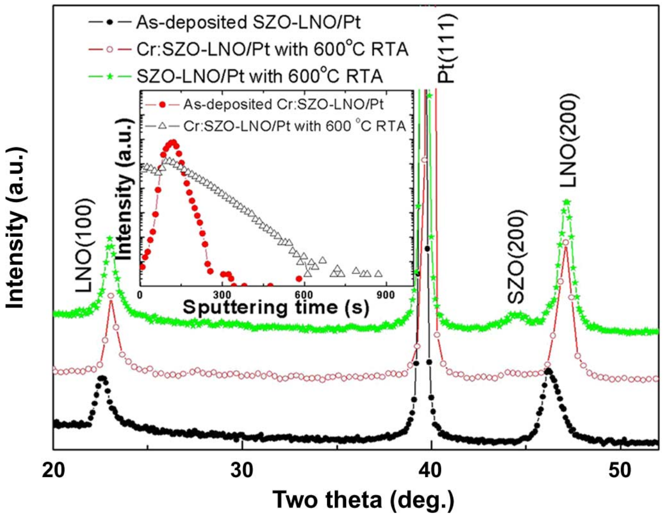

Fig. 1. XRD patterns of as-deposited SZO thin film and of these with/without embedded Cr layer after 600-°C annealing. The inset shows Cr diffused into SZO thin film after 600-°C annealing as compared with that without annealing.

device with Cr metal embedded (Al/Cr:SZO–LNO/Pt). Because the proposed resistive switching phenomenon occurred within the SZO film, the same SZO film thickness (40 nm) was mainly employed for the reference device without Cr metal embedded (Al/SZO–LNO/Pt). Agilent 4155C semiconductor parameter analyzer was used to measure the current–voltage (*I–V*) characteristics of the SZO-based device by applying voltage bias on Al top electrode with Pt bottom electrode common.

III. RESULTS AND DISCUSSION

Fig. 1 shows the X-ray diffraction patterns of the as-deposited SZO film, the Cr:SZO–LNO/Pt with 600-°C RTA, and the SZO–LNO/Pt with 600-°C RTA. The as-deposited SZO is amorphous, but the SZO (200) peak of the SZO–LNO/Pt and the Cr:SZO–LNO/Pt appears after 600-°C annealing, where the peak intensity of the Cr:SZO–LNO/Pt is lower than that of the SZO–LNO/Pt. The pure SZO film has better crystallinity than the Cr:SZO film. The bipolar and reproducible *I–V* characteristics of both Al/SZO–LNO/Pt and Al/Cr:SZO–LNO/Pt devices are demonstrated in Fig. 2(a). The resistance ratio between two memory states of these two memory devices is over 1000 times. Moreover, similar nonpolar resistive switching, as shown in our previous report [15], can also be performed in these two devices here. Before performing any resistive switching, a high-voltage forming process about -10 V is necessary to activate the Al/SZO–LNO/Pt device. As for the Al/Cr:SZO–LNO/Pt device, it indicates that the embedded Cr layer diffuses into the SZO film after annealing, based on the result of secondary ion mass spectrometry analysis (as shown in the inset of Fig. 1), leading to the forming process which is unnecessary (because the *I–V* curve of the forming process coincides with that of the ON process).

In Fig. 2(b) and (c), the distributions of the $R_{\rm ON}$, $R_{\rm OFF}$, $V_{\rm ON}$, and $V_{\rm OFF}$ during the first 50 successive resistive switching cycles in both Al/SZO–LNO/Pt and Al/Cr:SZO–LNO/Pt devices are presented by circle and by triangle, respectively. The quantitative values, mean value (standard deviation), of $R_{\rm ON}$, $R_{\rm OFF}$, $V_{\rm ON}$, and $V_{\rm OFF}$ of the Al/Cr:SZO–LNO/Pt device are 872.77 (20.76) Ω, 3.34×10^6 (1.06×10^6) Ω, 4.69 (0.10) V, and 2.14 (0.30) V, respectively; those of the Al/SZO–LNO/Pt device are 28.15 (25.07) Ω, 1.07×10^8 (1.57×10^8) Ω, 6.31 (1.64) V, and 1.24 (0.30) V, respectively. The Al/SZO–LNO/Pt devices are apparently less stable as compared with the Al/Cr:SZO–LNO/Pt. Moreover, large variations of $R_{\rm ON}$ and $R_{\rm OFF}$ of the SZO-based memory device have been observed in our previous study [15]. To rule out the SZO film thickness effects, the Al/SZO–LNO/Pt devices with various SZO thicknesses from 20 to 60 nm are also investigated. All of them exhibit large variations of $R_{\rm ON}$, $R_{\rm OFF}$, $V_{\rm ON}$, and $V_{\rm OFF}$, which have the similar curves as shown in Fig. 2(b) and (c). It further convinces that the resistive switching characteristics of the Al/Cr:SZO–LNO/Pt devices are stabilized by embedding Cr layer.

On the basis of the experimental results in this study and the other reported works [3]–[6], [16], it is commonly observed that the sharp distributions of the $R_{\rm ON}$, $R_{\rm OFF}$, $V_{\rm ON}$, and $V_{\rm OFF}$, i.e., lowering the resistive switching variation, are corresponding with smaller resistance ratio between ON-state and OFF-state, and with smaller $R_{\rm OFF}$ (usually, accompanying with larger $R_{\rm ON}$). It indicates that the effective resistive switching region is reduced, stabilized, and confirmed. In spite of the decrease in the resistance ratio, it still provides enough memory margin for RRAM application. Moreover, comparing the Al/Cr:SZO–LNO/Pt device with the Al/SZO–LNO/Pt device, the values of $R_{\rm ON}$ and $V_{\rm OFF}$ increase, but those of $R_{\rm OFF}$ and $V_{\rm ON}$ reduce, which are the same tendencies as reported in our previous report in $Ti/ZrO_2/Pt$ device [17]. We proposed that the interface layer formed between Ti and ZrO_2 can serve as a series resistance, modify the oxygen content, and reduce the effective resistive switching region. Such an interface layer is believed to be formed in our Al/Cr:SZO–LNO/Pt device as well, which further influences the carrier conduction mechanism described in the following section.

The conduction mechanisms for the ON-state and the OFF-state in the Al/SZO–LNO/Pt device are Ohmic conduction and Frenkl–Poole emission, respectively, which have been shown in our previous studies [13]–[15]. The double-logarithmic scale plots of the *I–V* curve for both positive and negative bias regions in the Al/Cr:SZO–LNO/Pt device are shown in Fig. 3, and the conduction mechanism can be described well by the space charge limited current (SCLC) theory [19]. In low voltage and negative bias region, Ohmic conduction $(s = 1)$ is observed due to the thermal-free carriers exceeding the injected ones. Then, the trap-unfilled SCLC $(s = 2)$ is observed, and after an abrupt current increase (caused by forming the conducting filaments and trapping the injected charges), the trap-filled SCLC $(s = 2)$, sequentially, appears in the voltage-decreasing scan. Finally, the ON-state is attained and obeys the Ohmic conduction as shown in Fig. 3. For OFF process in the positive bias region, the conduction mechanism obeying SCLC theory accompanying with rupturing the conducting filaments is also observed. Similar conduction behavior was reported in $Mo/Cu_xO/Pt$ devices [19]. A defected interface layer is believed to be formed due to the interdiffusion between the Cr metal and

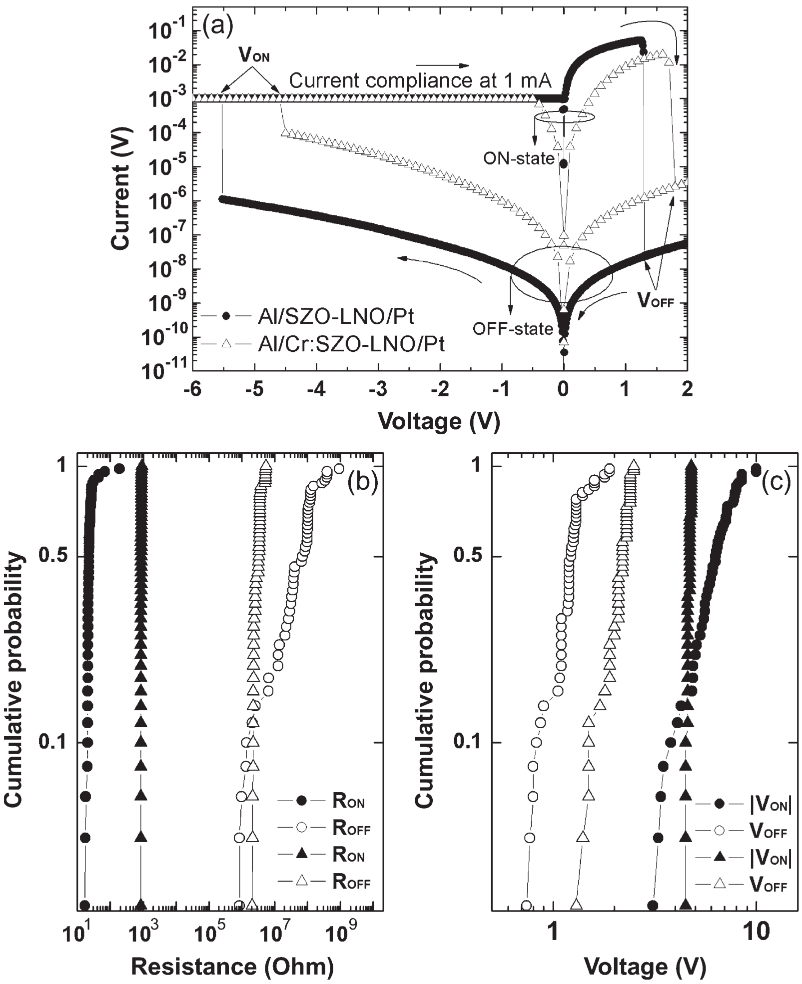

Fig. 2. (a) *I–V* characteristics of both Al/SZO–LNO/Pt and Al/Cr:SZO–LNO/Pt devices where the arrows indicate the voltage sweeping direction. (b) and (c) Distributions of the R_{ON}, R_{OFF}, V_{ON}, and V_{OFF} in both Al/SZO–LNO/Pt (presented by circle) and Al/Cr:SZO–LNO/Pt (presented by triangle) devices during 50 successive resistive switching cycles.

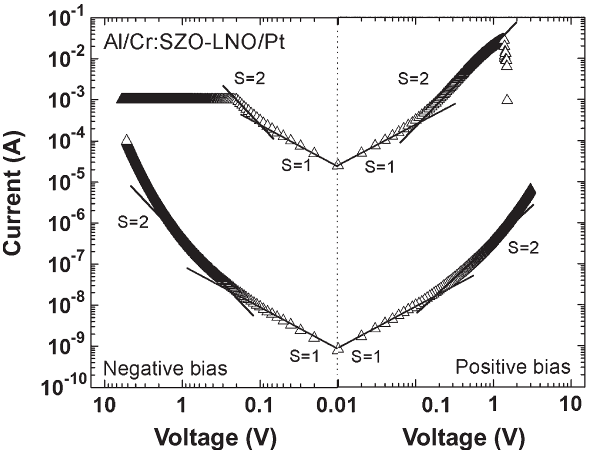

Fig. 3. *I–V* characteristics of both positive and negative bias regions of the Al/Cr:SZO–LNO/Pt device plotted in a double-logarithmic scale. Both ON-state and OFF-state are included on this plot.

the SZO film. Such an interface layer leads to the formation of the space charge region in the Al/Cr:SZO–LNO/Pt device, which is one of the reasons why the aforementioned electrical characteristics occur.

In addition to the space charge region formed, the Cr metal might also dope and diffuse into the SZO thin films, and all have influences on the oxygen content, the trap states, and even the oxygen and trap distributions, leading to the reduction of the effective resistive switching region and the stabilization of the resistive switching properties. Further study to investigate and to characterize the correlations among the embedded metal layer, the middle space charge region, and the resistive switching characteristics is under progress.

IV. CONCLUSION

In summary, the effects of the embedded Cr metal on the resistive switching properties of our SZO devices are demonstrated. The space charge region created within the SZO thin film is due to the reaction between the Cr metal and the SZO film. The SCLC theory is employed to well explain the conduction behaviors of the device. The Cr metal is also proposed to dope and diffuse into the SZO thin film to further reduce the effective resistive switching region and modify the SZO thin film. As a result, the good stabilization of the resistive switching characteristics can be obtained by this simple method in Al/Cr:SZO–LNO/Pt device, showing promising potential for next-generation NVM application.

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