Investigation of the Polarity Asymmetry on the Electrical Characteristics of Thin Polyoxides Grown on N^+ Polysilicon

Shye Lin Wu, *Member, IEEE,* Chun Yuan Chen, Ta Yow Lin, Chung Len Lee, *Senior Member, IEEE,* Tan Fu Lei, and Mong Song Liang, *Member, IEEE*

***Abstract*— The polarity asymmetry on the electrical characteristics of the oxides grown on n^+ polysilicon (polyoxides) was investigated in terms of the oxidation process, the doping level of the lower polysilicon layer, the oxidation temperature and the oxide thickness. It was found that the thin polyoxide prepared by using a low-temperature wafer loading and N_2 pre-annealing process, has a smoother polyoxide/polysilicon interface and exhibits a lower oxide tunneling current, a higher dielectric breakdown field when the top electrode is positively biased, a lower electron trapping rate and a larger charge-to-breakdown than does the normal polyoxide. The polarity asymmetry is also strongly dependent on the doping level of the lower polysilicon layer, the oxidation temperature and the oxide thickness. It was found that only the thinner polyoxides ($\leq$240Å) grown on the heavily-doped polysilicon film (30 Ω/sq) by using the higher-temperature oxidation process ($\geq$950 °C) conduct a less oxide tunneling current when the top electrode is positively biased.**

I. Introduction

THERMAL oxides grown on n^+polysilicon (referred to as polyoxides) have been widely used as the interlayer dielectrics for nonvolatile memories, such as EPROM, EEPROM, and Flash EEPROM [1]–[4]. However, due to the nonuniformity of the oxide thickness and the asperities at the polysilicon/polyoxide interface, the electrical properties, such as the dielectric breakdown field, the oxide leakage current, the electron trapping rate under a high field stressing and the charge-to-breakdown of polyoxides are inferior to those of oxides grown from single crystal silicon [5]–[11].

It has been reported that polyoxides exhibit a higher conductance and a lower dielectric breakdown field when the top electrode is positively biased [7]–[10]. This is attributed to the higher local field induced by the interface roughness at the bottom polyoxide/polysilicon interface, caused by the enhanced oxidation rate at grain boundaries [7]–[9]. On the other hand, Faraoner reported that the electrical characteristics and the effective barrier height of oxides grown on a textured polysilicon layer were nearly independent of the applied voltage polarity, due to the similar roughness of both the bottom and top polyoxide/polysilicon interfaces [11].

It has also been found that thin thermal oxides (~130 Å) grown on heavily phosphorus doped polysilicon layer by using a low-temperature wafer loading and N_2 pre-annealing process and oxidation at a high temperature (1000 °C), would exhibit a lower leakage current and a higher dielectric breakdown field as the top electrode under a positive biasing [12]. The possible explanation is that the low temperature wafer loading and N_2 pre-annealing process could reduce the thermal stress, the native oxide growth, and the oxidation rate [13]. This results in a smoother surface morphology of the polysilicon before oxidation and then induces a smoother polysilicon/polyoxide interface during the oxidation step.

In this paper, we investigate in detail the polarity asymmetry on the electrical characteristics of the textured polyoxides in terms of the oxidation process, the doping level of the lower polysilicon layer, the oxidation temperature and the oxide thickness.

II. Experimental Procedures

Thin polyoxide capacitors were fabricated on a 4000 Å polysilicon film deposited on a substrate with thermal oxidation of 1000 Å-thick oxide. The lower polysilicon layers (poly1) was deposited in an LPCVD system at 625 °C. After phosphorus doping with a $POCl_3$ source at 925 °C or 950 °C, the drive-in process was performed at 1000 °C in a dry $N_2 + O_2$ ambient. After removing the surface oxide, the sheet resistance of the polysilicon layer was measured to be about 90–110 Ω/sq (referred to as the lightly-doped polysilicon), 50–70 Ω/sq (referred to as the median-doped polysilicon) or 20–33 Ω/sq (referred to as the heavily-doped polysilicon). The wafers were loaded into the furnace at a low temperature (e.g., 600 °C) to reduce the thermal stress and minimize the native oxide growth [12]. Then, the temperature was gradually raised to 850 °C to 1000 °C in an N_2 ambient. After an N_2 pre-annealing stage for about 15 to 30 min, the polyoxides with a thickness of about 90–500 Å were grown at 850 °C to 1000 °C in a dry O_2 ambient or in a dry $O_2 + N_2$ ambient. This oxidation recipe is referred to as the special oxidation (SPO) process. The control samples were loaded into the furnace at 800 °C in an N_2 ambient and then oxidized at 1000 °C in a dry O_2 ambient without the N_2 pre-annealing stage for the same time as that of the SPO polyoxides. The process is referred to as the control oxidation (CTO) process. After the textured polyoxide formation, a second layer of

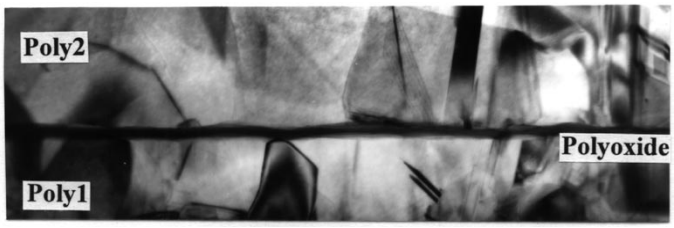
Manuscript received January 15, 1996; revised July 25, 1996. The review of this paper was arranged by Editor C.-Y. Lu.

S. L. Wu was with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. He is now with the Powerchip Semiconductor Corp., Hsinchu 30077, Taiwan, R.O.C.

C. Y. Chen, T. Y. Lin, C. L. Lee, and T. F. Lei are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

M. S. Liang is with the Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu 300, Taiwan, R.O.C.

Publisher Item Identifier S 0018-9383(97)00871-X.



(a)

(b)

Fig. 1. The TEM micrographs of (a) the SPO polyoxide and (b) the CTO polyoxide. The sheet resistance of poly1 is $\sim 30\ \Omega$/sq.

polysilicon (poly2) of about 4000 Å thick was deposited and doped by $POCl_3$ to the sheet resistance of about 20 Ω/sq. The thickness of the polyoxides were determined by the high-frequency (100 kHz or 1 MHz) capacitance–voltage (C–V) measurement by assuming the dielectric constant to be 3.9. The transmission electron microscopy (TEM) was used to examine the morphology of the polyoxide/polysilicon interface. The current–voltage (I–V) characteristics were measured by an HP4145B semiconductor parameter analyzer.

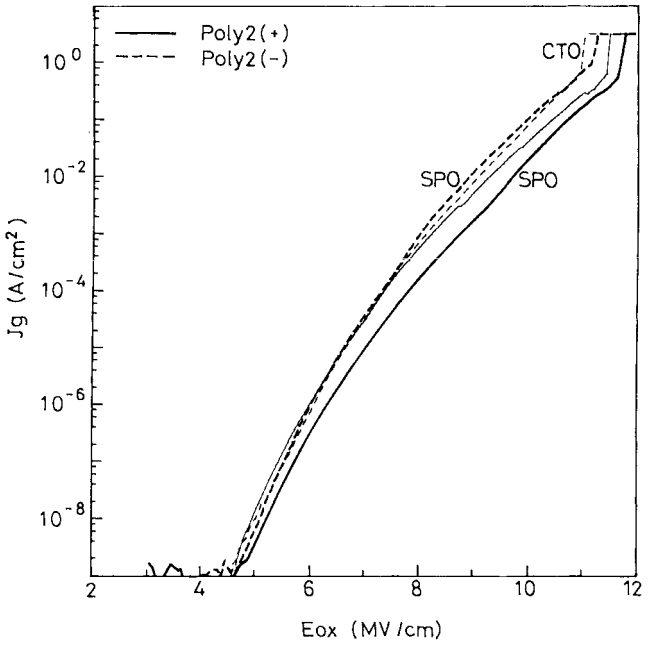
III. Results and Discussions

A. The Effect of Oxidation Process on Polarity Asymmetry

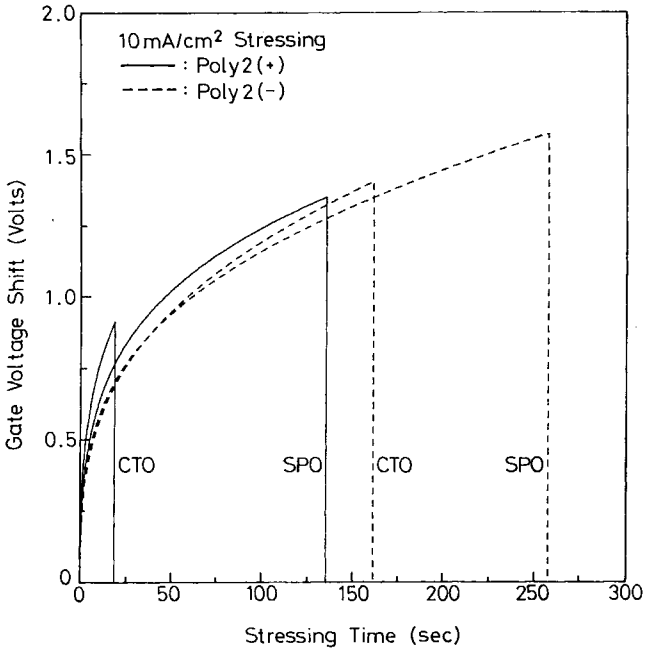
Fig. 1(a) and (b) show the TEM micrographs of the SPO and CTO polyoxides, respectively. It is seen that the SPO polyoxide has a smoother polyoxide/poly1 interface than the CTO polyoxide. The smoother surface morphology of the SPO polyoxide may be attributed to the reduction of the thermal stress, the native oxide growth, and the oxidation rate during the low-temperature wafer loading and N_2 pre-oxidation annealing process [13].

Fig. 2(a) shows the J_g–E_{ox} characteristics of the SPO polyoxide capacitor (heavy line) and the CTO polyoxide capacitor (thin line) grown on the heavily-doped poly1 ($\sim 30\,\Omega$/sq), respectively. The effective oxide thickness are 162 Å and 169 Å for the SPO and CTO polyoxides, respectively. The reduction in the oxide thickness of the SPO polyoxide is consistent with the thin oxide grown on the single-crystal silicon substrate with the same low-temperature wafer loading and N_2 pre-annealing process [13]. In the figure, the J_g–E_{ox} characteristics of the CTO polyoxide capacitor is nearly independent of the measurement polarity and consistent with the result of the previous paper [11]. However, the SPO polyoxide capacitor exhibits a strong polarity dependence on the J_g–E_{ox} characteristics, i.e., the SPO polyoxide capacitor conducts less tunneling current when poly2 is positively biased.

Fig. 2(b) shows the curves of gate voltage shift versus time of the SPO and CTO polyoxide capacitors under a constant current of ± 10 mA/cm^2 stressing. The area of the test capacitors is 1.26×10^{-3}cm^2. The increase in the gate voltage with the increasing time is due to electron trapping [14]. It is seen that the SPO polyoxide capacitor exhibits a lower electron trapping rate than does the CTO polyoxide capacitor in both injection polarities. Moreover, the value of charge-to-breakdown (Q_{bd}) of the SPO polyoxide capacitor is larger than that of the CTO polyoxide capacitor, especially for



(a)



(b)

Fig. 2. (a) The J_g–E_{ox} characteristics of the SPO polyoxide capacitor (heavy line) and the CTO polyoxide capacitor (thin line) grown on the heavily-doped poly1 ($\sim 30\ \Omega$/sq), respectively. The effective oxide thickness determined by the high-frequency C–V measurement are about 162 Å and 169 Å for the SPO and CTO polyoxide capacitors, respectively, and (b) the curves of gate voltage shift versus time of the SPO and CTO polyoxide capacitors under a constant current of ± 10 mA/cm^2 stressing. The area of the testing capacitors is 1.26×10^{-3} cm^2.

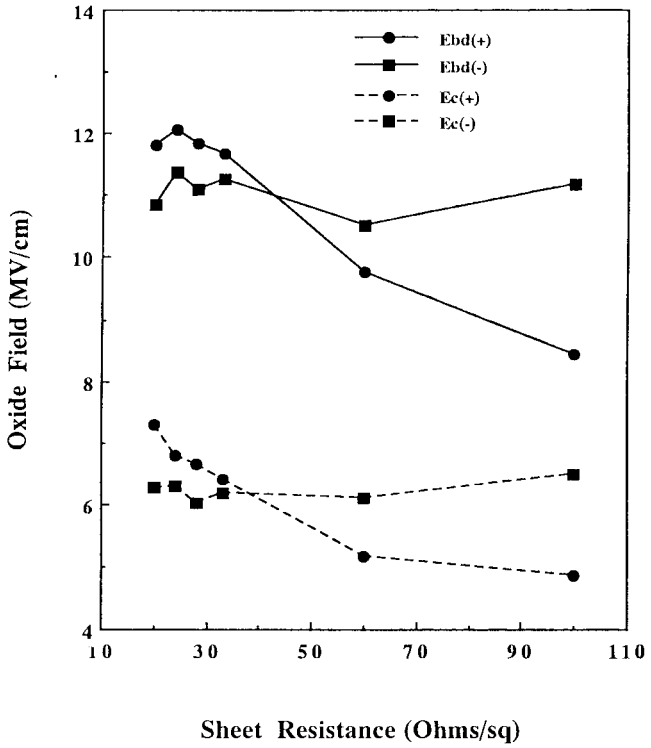


Fig. 3. The plots of the sheet resistance of poly1 and the critical electric field (E_c) and the breakdown field (E_{bd}).

the electron injection from the bottom polyoxide/polysilicon interface.

High electron trapping rate and low Q_{bd} value of polyoxides have been attributed to the outdiffusion of phosphorus from polysilicon into polyoxide [15]. During the high-temperature oxidation process, a large amount of phosphorus would pile up at or near the bottom polyoxide/polysilicon interface [15] and the phosphorus precipitates would remain in the grain boundaries of polysilicon and in the bulk of the polyoxide. These precipitates act as the electron trapping sites and result in an increase in the leakage current due to the trap-assisted direct tunneling [15]. From the lower electron trapping rate and the higher Q_{bd} value, it can be suggested that, for the SPO polyoxide, the amount of phosphorus outdiffusion from poly1 into polyoxide is less than that of the CTO polyoxide.

B. The Effect of Poly1 Doping Level on Polarity Asymmetry

It has been reported that the polyoxide/polysilicon interface of the oxides grown on the heavily-doped poly1 (heavily-doped polyoxide) is smoother than oxides grown on the median-doped poly1 (median-doped polyoxide) [12]. Also, the polarity asymmetry of the heavily-doped polyoxide is opposite to the median-doped polyoxide, i.e, the heavily-doped polyoxides conducts a less tunneling current and has a higher E_{bd} value when poly2 is positively biased while for the median-doped polyoxide, it conducts a higher tunneling current and has a lower dielectric breakdown field (E_{bd}) when poly2 is positively biased [12].

Fig. 3 shows the plots of the sheet resistance of poly1 versus the critical electric field (E_c), which is defined as the field for the leakage current of $1\,\mu$A/cm^2 through the polyoxide, and the destructive dielectric breakdown field (E_{bd}) for the

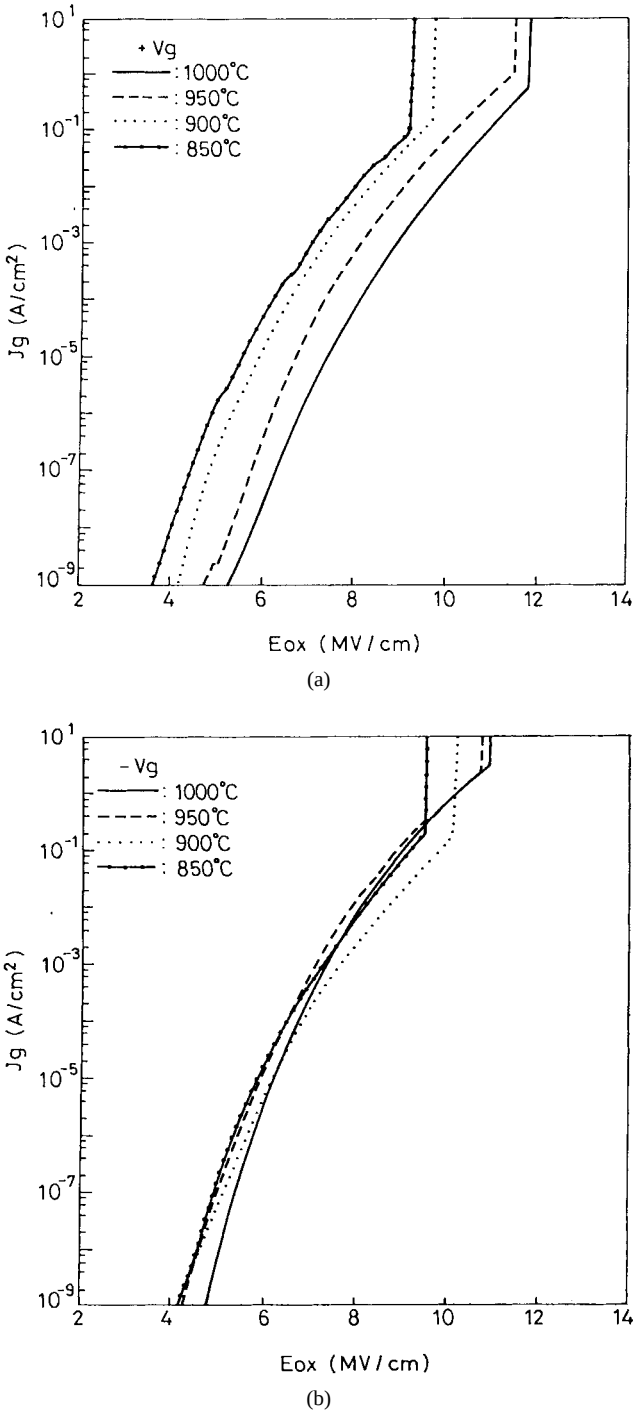


Fig. 4. The J_g–E_{ox} characteristics of the lower-temperature (850 °C and 900 °C) polyoxides and the higher temperature (950 °C and 1000 °C) polyoxides for poly2 under (a) a positive bias and (b) a negative bias, respectively.

polyoxides with the thickness ranging from 110–150 Å. It is seen that both the E_c and E_{bd} values of the heavily-doped polyoxide (20–33Ω/sq) are larger than those of the median-doped polyoxide (50–70Ω/sq) and the lightly-doped polyoxide (90–110Ω/sq) when poly2 is positively biased. The better quality of the heavily-doped polyoxide is believed to be due to the larger grain size of the heavy doping poly1, which results in a smoother polyoxide/polysilicon interface [8] and [12]. As the phosphorus concentration is increased, the stress-induced oxide thinning and the "horn" formation can be prevented by

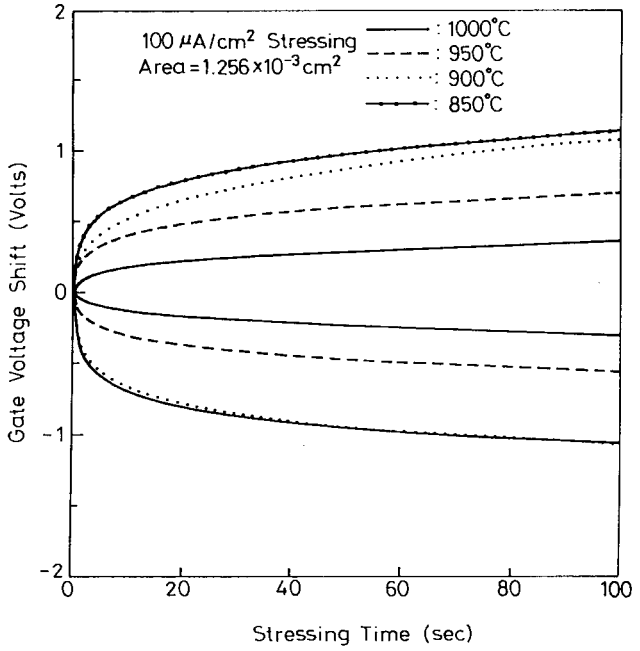


Fig. 5. The curves of gate voltage shift versus time of the lower-temperature and higher-temperature polyoxide capacitors under a constant current of $\pm 100\,\mu$A/cm^2 stressing.

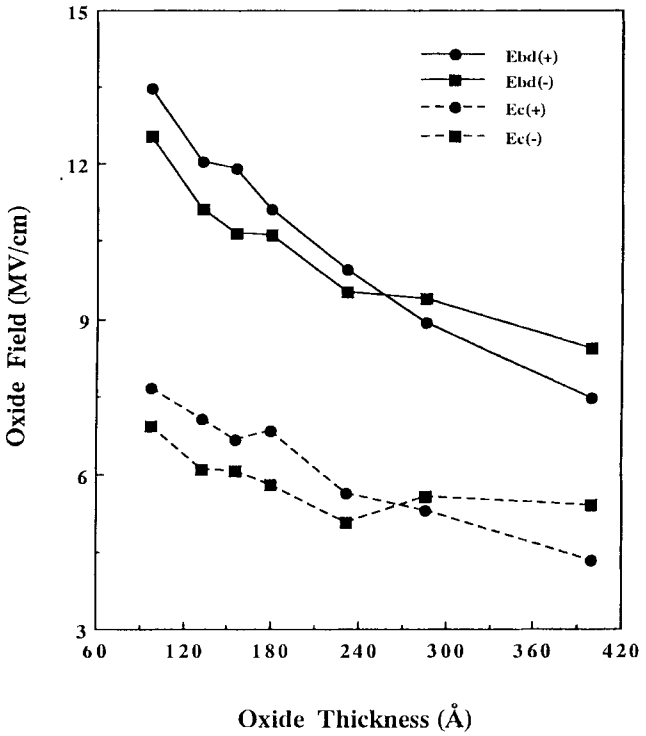


Fig. 6. The plots of the value of E_{bd} and E_c versus the oxide thickness ranging from 98 to 399 Å.

introducing vacancies into Si and by the enhancement of the SiO_2 viscous-flow [8]. However, as mentioned previously, due to the outdiffusion of phosphorus from poly1 into polyoxide during the oxidation process, a large amount of phosphorus would pile up at or near the polyoxide/polysilicon interface [15] and the phosphorus precipitates would remain in the polysilicon grain boundary and in the bulk of the polyoxide. These precipitates act as the electron trapping sites and result in an increase in the leakage current due to the trap-assisted direct tunneling [15]. Thus, a large amount of the phosphorus incorporated into the polyoxide will degrade the oxide quality, despite of the smoother polyoxide/polysilicon interface. The E_c values of the polyoxide grown on the more heavily-doped poly1 ($\sim$17Ω/sq) were reduced to 1.2 and 2.4 MV/cm for poly2 under a positive and negative bias, respectively.

C. The Effect of Oxidation Temperature on Polarity Asymmetry

Fig. 4(a) and (b) show the J_g–V_g characteristics of the lower-temperature (850 °C and 900 °C) polyoxides and the higher-temperature (950 °C and 1000 °C) polyoxides for poly2 under a positive and negative bias, respectively. The effective oxide thickness of these polyoxides are about 130–140 Å and the sheet resistance of poly1 is about 22 Ω/sq. It is seen that the lower-temperature polyoxides exhibit a larger oxide leakage current and a lower E_c value when poly2 is positively biased. This implies that for the lower-temperature polyoxides, the bottom polyoxide/polysilicon interface is rougher than the top one [11]. The polarity asymmetry is consistent to that reported by previous papers [7]–[11]. However, the higher-temperature polyoxides exhibit a much less oxide leakage current and a larger E_c value when poly2 is positively biased. This implies that the bottom polyoxide/polysilicon interface of the higher-temperature polyoxides is smoother than the top one. Thus, the polarity asymmetry on the electrical properties of the polyoxides is strongly dependent on the oxidation temperature. Moreover, the higher-temperature polyoxides have a much less electron trapping rate than the lower-temperature polyoxides in both injection polarities, as shown in Fig. 5. This suggests that the oxide quality of the higher-temperature polyoxides are much better than that of the lower-temperature polyoxides. This is consistent to the situation of oxides grown on the single-crystal silicon substrate [16] and could be explained as follows. It has been reported that the low-temperature oxidation process is pre-dominantly controlled by the surface reaction [17]. The enhanced oxidation rate at the grain boundaries would enhance the stress between the grains and cause a rougher polyoxide/polysilicon interface [8] and [17]. In contrast, the mechanism of the high temperature oxidation process is dominated by the oxidant diffusion [17], as a result, the oxidation-induced stress due to the higher oxidation rate at the grain boundaries could be reduced [8]. Besides, at a higher temperature the viscous flow of the oxide could occur [18]. Thus, a smoother polyoxide/polysilicon interface could be obtained for polyoxides prepared at a higher temperature. Hence, the polyoxides prepared by the higher-temperature oxidation process have better electrical properties than the lower-temperature polyoxides.

D. The Effect of Oxide Thickness on Polarity Asymmetry

In this section, we will discuss the effect of the oxide thickness on the polarity asymmetry of the value of E_c and E_{bd}, the electron trapping rate and the trapped-charge centroid of the heavily-doped polyoxides. The oxidation process was performed at 1000 °C in a $O_2 + N_2$ ambient. Fig. 6 shows the plots of the value of E_c and E_{bd} versus the oxide thickness

ranging from 98–399 Å. It is seen that the heavily-doped polyoxides have a larger E_c and E_{bd} value when poly2 is positively biased, until the oxide thickness is more than 240 Å, which has been reported to be independent of the measurement polarity [11]. The inversion of the polarity asymmetry on E_c and E_{bd} for the thicker polyoxides (>240 Å) may be due to the fact that the longer oxidation time resulted in more phosphorus outdiffusion from poly1 into the polyoxide to form phosphorus precipitates, which act as the electron trapping sites and cause a more oxide leakage current due to the trap-assisted direct tunneling [15]. Another reason was that the longer oxidation resulted in a rougher bottom polyoxide/polysilicon interface due to the enhanced oxidation rate at the grain boundaries [7]–[9].

The Fowler–Nordheim (F–N) injection technique [19] was used to identify the trapped oxide charges density (Q_{ot}) and the trapped-charge centroid (x) in the polyoxide. By comparing the deviations of the F–N I–V characteristics before and after stresses with both polarities, the values of Q_{ot} and x can be determined [19] and [20], where x is the location of the trapped oxide charges measured from the poly2. Fig. 7(a) and (b) shows the gate voltage shift, V_g, versus the injection fluence for the heavily-doped polyoxides of 131, 286, and 399 Å under a constant current of $\pm 10\,\mu$A/cm^2 injection stressings, respectively, where $V_g(+)$ is the voltage shift when the poly2 is positively biased and $V_g(-)$ is the voltage shift when the poly2 is negatively biased. It is seen that for the bottom injection, the values of $V_g(+)$ of all the polyoxides are much larger than those of the $V_g(-)$. Moreover, the value of $V_g(+)$ increases significantly with the increase of the oxide thickness, while the value of $V_g(-)$ increases only slightly. For the top injection, the value of $V_g(+)$ of all the heavily-doped polyoxides are somewhat smaller than that of the $V_g(-)$. Also, the increase in both the $V_g(+)$ and $V_g(-)$ values with the increase of the oxide thickness are similar. This implies that for the heavily-doped polyoxides, the increase in the electron trapping rate with the increase of the oxide thickness is predominated by the property of the bottom polyoxide/polysilicon interface. Due to the fact that a longer oxidation time results in rougher bottom polyoxide/polysilicon interface [7]–[9] and more phosphorus outdiffusion from poly1 into polyoxide to form phosphorus precipitates [15], which act as the electron trapping sites the thicker heavily-doped polyoxide has a much larger electron trapping rate than does the thinner heavily-doped polyoxide in both polarities, as shown in Fig. 7(a).

As mentioned previously, the thinner heavily-doped polyoxide has a lower oxide leakage current and a larger E_c and E_{bd} value when poly2 is positively biased. This can be expected because the thinner heavily-doped polyoxide has a lower electron trapping rate when electrons are injected from the bottom polyoxide/polysilicon interface. However, as shown in Fig. 8(a), the value of Q_{ot} of the bottom injection is larger than that of the top injection. Thus, it is believed that for the heavily-doped polyoxide, the larger electron trapping rate with poly2 under a positive bias is pre-dominantly by the outdiffusion of phosphorus from poly1 into the polyoxide to be the electron trapping sites near the bottom polyoxide/polysilicon interface [15].

For all the heavily-doped polyoxides, the location of the trapped-charge centroid, x, is strongly dependent on the injection polarity, as shown in Fig. 8(b). For the bottom injection,

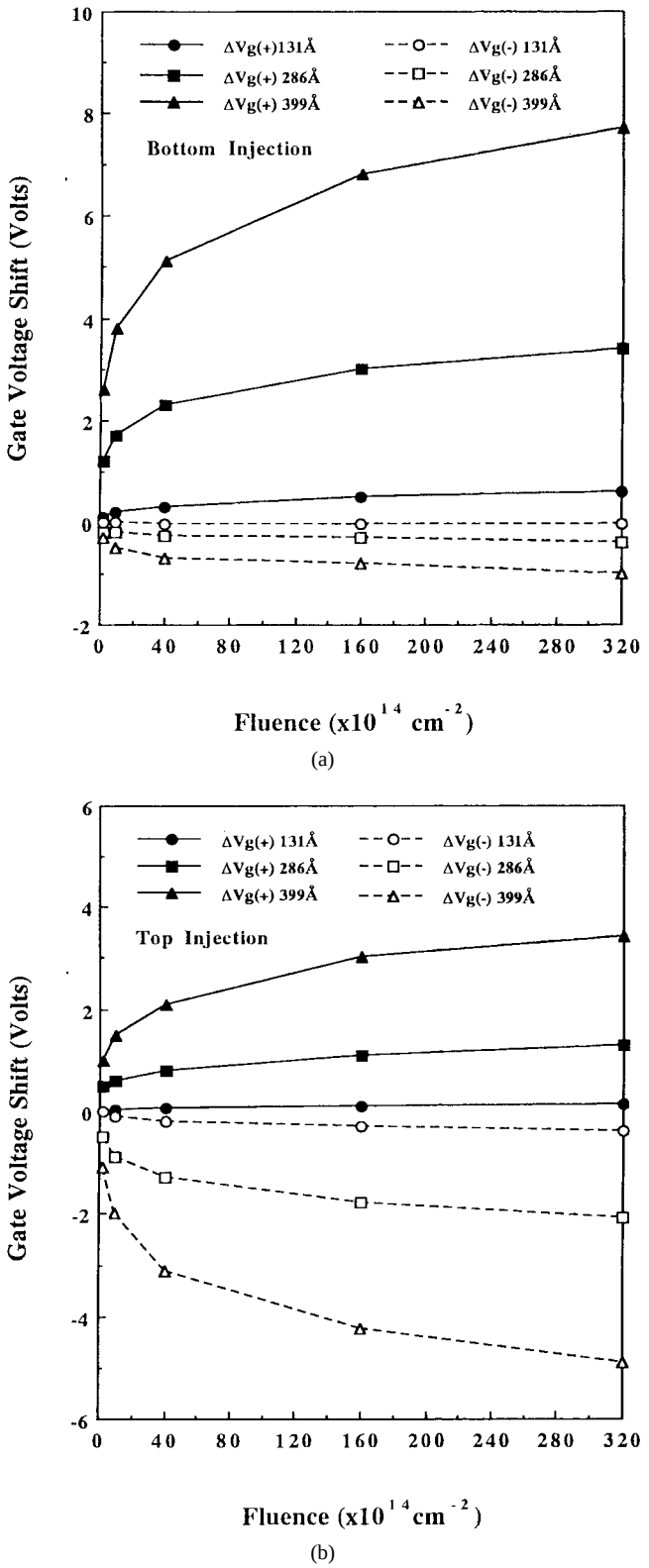
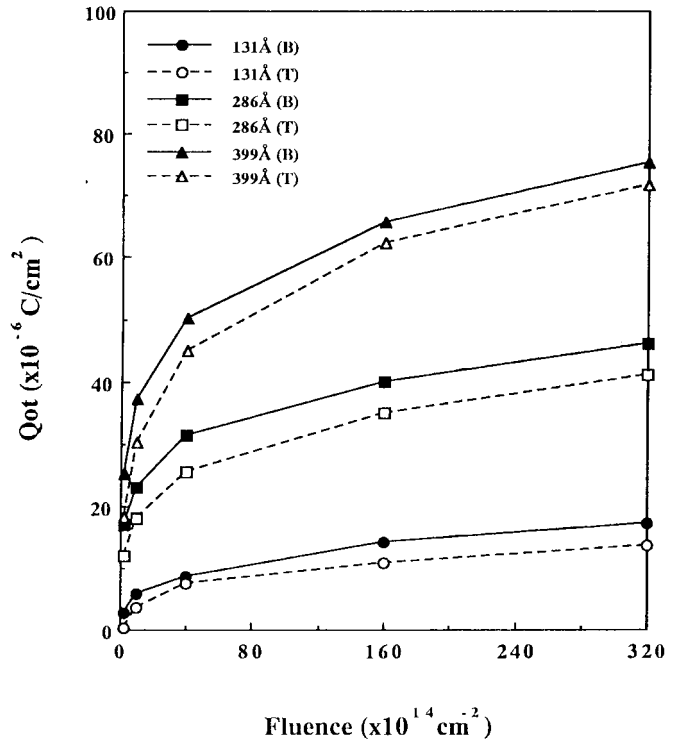
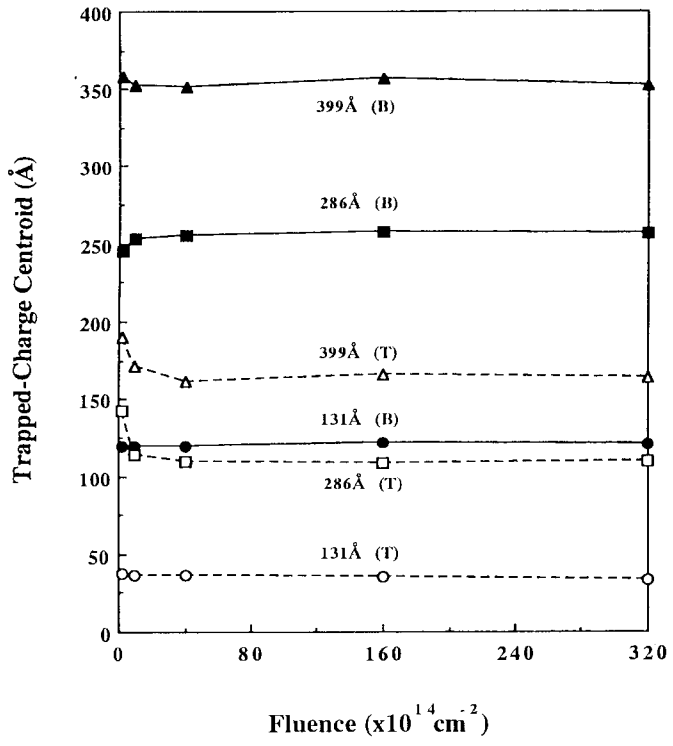


Fig. 7. The curves of the gate voltage shifts, $V_g(+)$ and $V_g(-)$, versus the injection fluence for the heavily doped polyoxides of 131, 286, and 399 Å under a constant current of (a) $10\,\mu$A/cm^2 (bottom injection) and (b) $-10\,\mu$A/cm^2 (top injection) stressings, respectively.

the trapped charges of all the heavily-doped polyoxides are located near the bottom polyoxide/polysilicon interface. For example, the value of x of the thicker (399 Å) and the thinner (131 Å) heavily-doped polyoxides are about 350



(a)



(b)

Fig. 8. The curves of (a) the trapped-charge density (Q_{ot}) and (b) the trapped-charge centroid (x) versus the injection fluence of the heavily-doped polyoxides of 131, 286, and 399 Å, respectively.

Å and 120 Å away from poly2, respectively. This can be explained by the outdiffusion of phosphorus from poly1 into polyoxide to generate the electron trapping sites near the bottom polyoxide/polysilicon interface [15]. However, for the top injection, the value of x of the thicker heavily-doped polyoxide is about 170 Å away from poly2, i.e., the trapped charges are located close to the middle of the polyoxide layer. This is consistent with the result of Avni *et al.* [20]. On the other hand, for the thinner heavily-doped polyoxide, the value of x is about 35 Å away from poly2, i.e., the trapped charges are located near the top polyoxide/polysilicon interface. This polarity dependence of the trapped-charge centroid of the thinner heavily-doped polyoxide was not reported before. This phenomenon may be explained by the fact that for the thinner heavily-doped polyoxide, the top polyoxide/polysilicon interface is rougher than the bottom one, while the amount of the phosphorus outdiffusion from poly1 into the polyoxide is larger than that from poly2 into the polyoxide.

IV. Conclusion

In this work, we have investigated the polarity asymmetry on the electrical characteristics of the polyoxides in terms of the oxidation process, the doping level of poly1, the oxidation temperature and the oxide thickness. It is found that high quality thin polyoxides could be obtained by using a low-temperature wafer loading and N_2 pre-annealing process. As compared to the normal polyoxides, the prepared polyoxides exhibit a lower oxide leakage current, a higher E_c and E_{bd} value, a smaller electron trapping rate and a larger Q_{bd} value. Moreover, the prepared polyoxides exhibit a lower oxide leakage current and a higher E_c and E_{bd} value when poly2 is positively biased, while for the normal polyoxide, the oxide leakage current and the dielectric breakdown field are nearly independent of the measurement polarity. This is due to that the bottom polysilicon/polyoxide interface of the prepared polyoxide is smoother than that of the normal polyoxide. The smaller electron trapping rate and a larger Q_{bd} value for the prepared polyoxides may also be due to the less electron trapping sites generated from the phosphorus outdiffusion from poly1 into the polyoxide [15].

The polarity asymmetry on the electrical characteristics of the polyoxides were found to be strongly dependent on the doping level of poly1, the oxidation temperature and the oxide thickness. Only the thinner polyoxide ($\leq$240 Å) grown on the heavily doped polysilicon film ($\leq$30 Ω/sq) by using the higher-temperature oxidation process ($\geq$950 °C) can exhibit lower oxide tunneling currents when the top electrode is positively biased. This is because the low-temperature oxidation process would enhance the oxidation-induced stress and cause more phosphorus atoms to segregate at grain boundaries [8]. Also, the longer oxidation time would cause more phosphorus outdiffusion from poly1 into the polyoxide to create the electron trapping sites and cause a rougher bottom polyoxide/polysilicon interface.

Acknowledgment

The authors would like to thank T. T. Sheng and J. F. Chen for TEM micrographs.

References

[1] S. K. Lai, V. K. Dham, and D. Guterman, "Comparison and trends in today's dominant E^2 technologies," in *IEDM Tech. Dig.*, 1986, pp. 580–583.

[2] R. Stewart, A. Ipri, L. Faraone, and J. Cartwright, "A low-voltage high-density EEPROM memory cell using symmetrical poly-to-poly

conduction," presented at the *IEEE Nonvolatile Semiconductor Memory Workshop*, Vail, CO, 1983.
[3] N. Mielke, A. Fazio, and H. C. Liou, "Reliability comparison of FLOTOX and textured-polysilicon E^2PROM's," in *Proc. 1987 IEEE/IRPS*, pp. 85–92.
[4] F. Massuoka, M. Asano, H. Iwahashi, T. Komuro, N. Tozawa, and S. Tanaka, "A 256-kbit flash E^2PROM using triple-polysilicon technology," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 548–552, 1987.
[5] *Nonvolatile Semiconductor Memories: Technologies, Design, and Applications*, C. Hu, Ed. New York: IEEE Press, 1991.
[6] R. M. Anderson and D. R. Kerr, "Evidence for surface asperity mechanism of conductivity in oxide grown on polycrystalline silicon," *J. Appl. Phys.*, vol. 48, pp. 4834–4836, 1977.
[7] P. A. Heimann, S. P. Murarka, and T. T. Sheng, "Electrical conduction and breakdown in oxides of polysilicon and their correlation with interface texture," *J. Appl. Phys.*, vol. 53, pp. 6240–6245, 1982.
[8] S. Mori, N. Arai, Y. Kaneko, and K. Yoshiawa, "Polyoxide thinning limitation and superior ONO interpoly dielectric for nonvolatile memory devices," *IEEE Trans. Electron Devices*, vol. 38, pp. 270–277, 1988.
[9] L. Faraone, R. D. Vibronek, and J. T. McGinn, "Characterization of thermally oxidized n^+polycrystalline silicon," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 577–583, 1985.
[10] J. C. Lee and C. Hu, "Polarity asymmetry of oxides grown on polycrystalline silicon," *IEEE Trans. Electron Devices*, vol. 35, pp. 1063–1070, 1988.
[11] L. Faraone, "Thermal SiO_2 films on n^+polycrystalline silicon: Electrical conduction and breakdown," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 1785–1794, 1986.
[12] S. L. Wu, T. Y. Lin, C. L. Lee, and T. F. Lei, "Electrical characteristics of textured polysilicon oxide prepared by a low-temperature wafer loading and N_2 preannealing process," *IEEE Electron Device Lett.*, vol. 14, pp. 113–114, Mar. 1993.
[13] S. L. Wu, C. L. Lee, and T. F. Lei, "Characterization of ultrathin oxide prepared by low-temperature wafer loading and nitrogen preannealing before oxidation," *J. Appl. Phys.*, vol. 72, pp. 1378–1385, 1992.
[14] M. S. Liang and C. Hu, "Electron trapping in very thin thermal silicon dioxides," in *IEDM Tech. Dig.*, 1981, p. 396.
[15] Y. Mikata, S. Mori, K. Shinada, and T. Usami, "Low leakage current poly-silicon oxide grown by two-step oxidation," in *Proc. 1985 IEEE/IRPS*, pp. 32–38.
[16] A. B. Joshi, G. Q. Lo, D. L. Kwong, and S. Lee, "Improved performance and reliability of MOSFET's with thin gate oxides grown at high temperatures," in *Proc. 1991 IEEE/IRPS*, pp. 316–322.
[17] E. A. Irene, E. Tierney, and D. W. Dong, "Silicon oxidation studies: Morphological aspects of the oxidation of polycrystalline silicon," *J. Electrochem. Soc.*, vol. 127, pp. 705–713, 1980.
[18] R. Mehta, A. B. Bhattacharyya, and D. N. Singh, "Post-growth process-induced degradation in thin gate oxides," *J. Appl. Phys.*, vol. 69, pp. 8247–8252, 1991.
[19] M.-S. Liang, N. Radjy, W. Cox, and S. Cagnina, "Charge trapping in dielectric grown on polycrystalline silicon," *J. Electrochem. Soc.*, vol. 136, pp. 3786–3790, 1989.
[20] E. Avni, O. Abramson, Y. Sonnenblick, and J. Shappir, "Charge trapping in oxide grown on polycrystalline silicon layers," *J. Electrochem. Soc.*, vol. 135, pp. 182–186, 1988.

Shye-Lin Wu (S'90–M'92) received the B.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, R.O.C., in 1987, and the M.S. and Ph.D. degrees from the National Chiao Tung University, Hsinchu, Taiwan, in 1989 and 1992, respectively.

From 1992 to 1993, he continued postdoctoral research at National Chiao Tung University. After serving two years in the military, he joined Vanguard International Semiconductor Corporation as a Senior Engineer. In 1996, he joined Powerchip Semiconductor Corporation, Hsinchu, Taiwan, as a member of the technical staff in the technology development department. His research interests include shallow junction formation, thin dielectric reliability, alternative gate dielectrics, isolation technology, dual poly gate structure, and polycide for advanced ULSI devices. He has published 20 papers and filed more than 40 patents (including four U.S. patents and seven R.O.C. patents granted) in the above areas.

Chun Yuan Chen, photograph and biography not available at the time of publication.

Ta Yow Lin, photograph and biography not available at the time of publication.

Chung Len Lee (S'70–M'75–SM'92) received the B.S. degree from National Taiwan University, Taipei, and the M.S. and Ph.D. degrees from Carnegie-Mellon University, Pittsburgh, PA, all in electrical engineering, in 1968, 1971, and 1975, respectively.

He joined the Department of Electronic Engineering, National Chiao Tung University, Hsinchu, Taiwan, as a faculty member in 1975, and is currently a Professor. His teaching and research have been in the areas of optoelectronics, integrated circuits, and computer-aided design. He was the director of the university's Semiconductor Research Center from 1980 to 1983, and has been the director of the Submicron Professionals Training Center since 1989. He has supervised more than 90 M.S. and Ph.D. students to completion of their theses and dissertations, and has published more than 120 papers in journals and conferences in the above areas.

Tan Fu Lei was born in Keelung, Taiwan, R.O.C., on September 17, 1944. He received the B.S. degree in electrical engineering from National Chung Keng University, Tainan, Taiwan, in 1967, and the M.S. and Ph.D. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1970 and 1979, respectively.

From 1970 to 1979, he was with the Fine Products Microelectronics Corporation, Taiwan, as an Engineer working on the fabrication of small-signal transistors. From 1980 to 1982, he was the Plant Manager, Photronic Corporation, Taiwan. In 1983, he joined the faculty of National Chiao Tung University as an Associate Professor, Department of Electronics Engineering and the Institute of Electronics. From 1984 to 1986, he was the Director of the Semiconductor Research Center. Presently, he is a Professor and the Associate Director of the National Nano Device Laboratory. His research interests are in semiconductor devices and optoelectronics.

Mong-Song Liang (M'83) received the B.S. and M.S. degrees in electrical engineering from Cheng-Kung University, Tainan, Taiwan, R.O.C., in 1975 and 1977, respectively, and the Ph.D. degree in electrical engineering from University of California, Berkeley, in 1984. His thesis research was in thin-gate dielectrics reliability.

From 1984 to 1988, he was with Advanced Micro Devices, Sunnyvale, CA, as a process development engineer, where he worked on the development of nonvolatile memories. From 1988 to 1992, he was with Mosel-Vetelic, San Jose, CA, where he worked on the development of SRAM and Mask ROM. In 1992, he joined Taiwan Semiconductor Manufacturing Company, Hsinchu, where he is engaged in the development of DRAM technology.