The Design of Low LO-Power 60-GHz CMOS Quadrature-Balanced Self-Switching Current-Mode Mixer

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***Abstract*—This letter describes the analysis and measurement of a complementary metal–oxide semiconductor (CMOS) quadrature-balanced current-mode mixer with a 90° branch-line hybrid coupler and self-switching current-mode devices. The proposed mixer, using 0.13 μm 1P8M CMOS technology, can downconvert a 60 GHz RF signal to a 2 GHz intermediate frequency (IF) signal, with a local-oscillator power of 0 dBm at 58 GHz. In the design, the mixer had a single-end conversion gain of 1 dB and an input-referred 1 dB compression point of 2 dBm. The LO–RF isolation of the mixer can achieve −37 dB while using 3 mA from a supply voltage of 1.2 V.**

***Index Terms*—Complementary metal–oxide semiconductor (CMOS), quadrature-balanced mixer, V-band.**

I. Introduction

DUE to the availability of a large unlicensed bandwidth of 7 GHz, there has been an increasing effort to exploit the 60 GHz band for wireless personal area network (WPAN) applications. With the continual scaling down of CMOS technology, a transit frequency (f_T) of up to 400 GHz has been reported in sub-10 nm technology nodes. As a result, CMOS technology has become a potential choice for the implementation of 60 GHz RF front-end circuits [1]–[3], all of which have voltage-mode mixer structures. While 60 GHz mixer structures use active single-ended topology [1] and have the low required input local-oscillator (LO) power, short-circuit drain nodes at the LO frequency are required to improve stability. Thus, an open quarter-wave stub at the drain node is used, which consequently consumes an extra chip area. And even though a 60 GHz single-ended resistive mixer [2] is designed to achieve high linearity, high input LO power is required, and the conversion loss is high. An active single-balanced 60 GHz mixer has been proposed [3], which has low linearity because of the required large voltage headroom.

Unlike voltage-mode circuits, where the commonly available voltage headroom is limited by the supply voltage, current-mode circuits have low impedance at internal nodes and signal information is carried by the time varying currents. Thus, the voltage at each node can be small, resulting in higher linearity performance. It is well known that in the design of mixers, linearity is a key performance parameter. Thus, a current-mode technique can be used to improve the linearity of a mixer operating with a low voltage supply.

Another proposed approach has been the implementation of a CMOS upconversion mixer at 2 GHz [4]. In the proposed upconversion mixer [4], a complimentary amplifier structure is used to combine the input LO and intermediate frequency (IF) signals. This letter proposes a 60 GHz quadrature-balanced downconversion mixer using a self-switching current-mode approach in 0.13 μm CMOS technology. In the proposed mixer, a self-switching current-mode circuit designed to include an area-efficient onchip 90° branch-line hybrid coupler is used to combine the LO and RF signals with an isolation of better than −37 dB. In downconversion mixers, both input LO and RF signals are high frequency. It is not efficient to combine them using the complimentary amplifier, with the low performance of a pMOS device at high frequencies. Thus, a passive combiner is proposed to overcome this problem.

The operational principle and circuit implementation are presented in Section II, while the experimental results themselves are described in Section III. Finally, the conclusion is given in Section IV.

II. Operational Principle and Circuit Implementation

The concept of the self-switching current-mode circuit is shown in Fig. 1(a) where Ma is an nMOS device. In Fig. 1(a), the RF signal current i_{rf} and the LO signal current i_{lo} are applied to the source together through a combiner, usually a filter or directional coupler. I_{TH} is the dc current added with i_{rf} to control the conversion gain. The resonator at the output port (capacitor C_T and inductor L_T) are used as the bandpass filter to reject all signals except IF. When $i_{lo} + I_{TH}$ is high enough in the direction of the source current i_s, Ma is switched on, and remains on only as long as this condition lasts, after which it is switched off. This property is adopted to form the downconversion mixer.

Assuming that the LO current i_{lo} is much larger than the input signal current i_{rf}, the ac current gain $A_i = i_d/i_{rf}$ of Ma can be considered to be a function of the sinusoidal LO current only, as shown in Fig. 1(b). In order to increase the speed of the switching device Ma, a proper $100\mu A\ I_{TH}$ bias current should be added to i_{rf} so that high operating speed with an acceptable conversion gain can be achieved.

The schematic diagram of the proposed 60 GHz CMOS downconversion quadrature-balanced mixer is shown in

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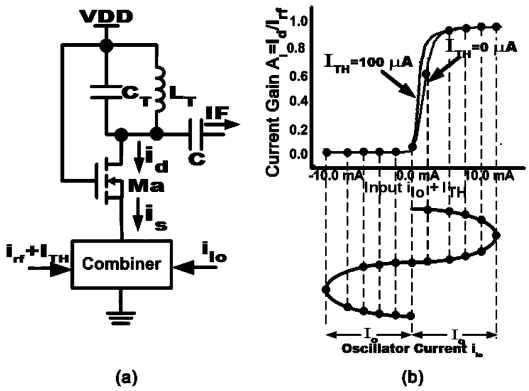

Fig. 1. (a) Circuit diagram of the self-switching current-mode mixer. (b) HSPICE simulated of ac current gain versus LO current with $I_{TH} = 0\ \mu$A and 100 μA.

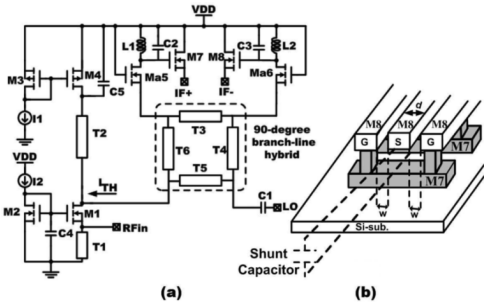

Fig. 2. (a) Circuit diagram of the CMOS quadrature-balanced current-mode mixer. (b) Coplanar waveguide transmission lines with the shunt capacitor.

Fig. 2(a). In Fig. 2(a), Ma5 and Ma6 are the self-switching devices, each biased by $1/2I_{TH}$. I_{TH} is controlled by I_1 and I_2 ($I_{TH} = I_2 - I_1$) through diode-connected transistors M3 and M2, respectively. The two parallel LC resonant tanks (L1, C2) and (L2, C3) at the output ports are used to select the IF frequency at 2 GHz. The 90° branch-line hybrid coupler, which consists of transmission lines T3-T6, each with the characteristic impedance of 60Ω at 60 GHz, is used to provide a 90° phase delay and achieve isolation between the LO and RF ports. The common-gate amplifier, consisting of M1, transmission lines T1 and T2 with a total length equal to 300 μm and bypass capacitors C4 and C5, is used to match the RF input port impedance of 50 Ω. C1 is the dc blocking capacitor to isolate the LO port from the dc source. Moreover, the two output source-follower buffers M7 and M8 are designed for measurement purposes to drive the 50-Ω input port of the network analyzer.

The proposed mixer offers two advantages. First, it has a self-switching device at its triode region with low operating power and high linearity. Second, the gate node is connected to VDD, an ac ground, and the drain node is short-circuited at the LO frequency, which reduces the required LO power [5] and improves the stability at the LO frequency [2]. And because the design of the proposed mixer must deal with the issue on the combination of LO and RF signals, a 90° branch-line hybrid coupler [5] and the quadrature-balanced mixer architecture are designed in.

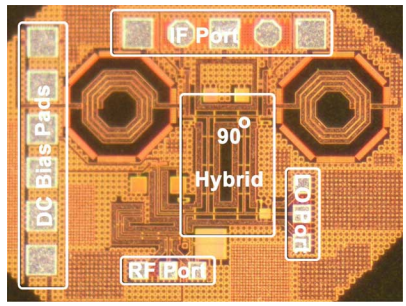

Fig. 3. Chip photograph of fabricated downconversion mixer.

At high operating frequencies, the hybrid can be easily integrated onto a chip, but it suffers from a large insertion loss due to the high substrate loss of the standard CMOS. In order to reduce the effect of the substrate loss, the branch-line and through-line lengths of the hybrid are reduced from $\lambda/4$ to $\lambda/6.4$ and $\lambda/10$, respectively, based on the methodology [6] of a short high-impedance transmission line with shunt lumped capacitors. In the methodology proposed in [6], the maximum transmission line length reduction depends on the maximum characteristic impedance of the transmission line. Conventionally, both microstrip line (MSL) and coplanar waveguide (CPW) are used to implement the transmission line. However, the maximum characteristic impedance of MSL depends on the distance between the top-layer and bottom-layer metals, which is fixed for a given CMOS technology. In the CPW transmission line shown in Fig. 2(b), the signal-to-ground spacing W can be used to increase the impedance of CPW, while the signal width d controls the conductor loss. Additionally, the underpass metal, which connects the two planar grounds to suppress unwanted odd CPW mode, is used with intrinsic device capacitances to implement the required shunt capacitors. Moreover, CPW is more area efficient than MSL. In MSL the isolation between the adjacent lines must be considered because the coupling between two adjacent lines changes the characteristic impedance. Consequently, an extra separation distance between the adjacent elements should be considered to eliminate the unwanted coupling effects. This drawback can be avoided in CPW by surrounding the signal line with two adjacent well-grounded lines. For these reasons, the CPW is used to design the 90° branch-line hybrid.

III. Experimental Results

The proposed mixer operating at 60 GHz was designed and fabricated in 0.13 μm 1P8M CMOS technology. The chip photograph is shown in Fig. 3, and the total die area is 1400 μm×1040 μm including all test pads and dummy metals. The performance of the fabricated mixer circuit was tested through an onwafer probing technique.

The test setup is shown in Fig. 4, where a signal generator with an external source module is used as 58 GHz LO source followed by a 10 dB directional coupler. A power sensor followed by a power meter is connected to the coupler's coupled port to monitor the LO power levels of the through port. The coupler's through port is connected through the waveguide connector of the 100 μm V-band microwave probe to the DUT.

The 60 GHz RF signal is generated by the signal generator and followed by a source module. However, because this source

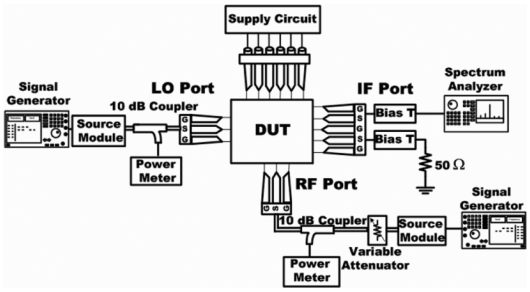

Fig. 4. Measurement setup of 60 GHz downconversion mixer.

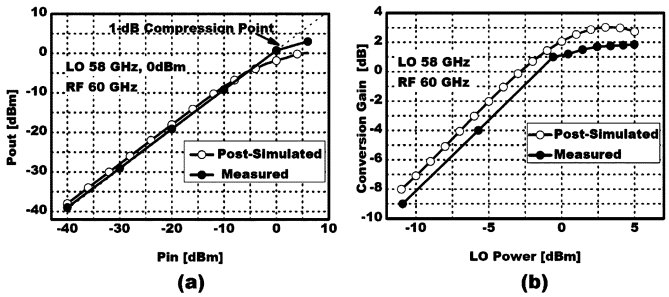

Fig. 5. (a) Measured and simulated IF output power versus RF input power. (b) The measured and simulated conversion gain versus LO power.

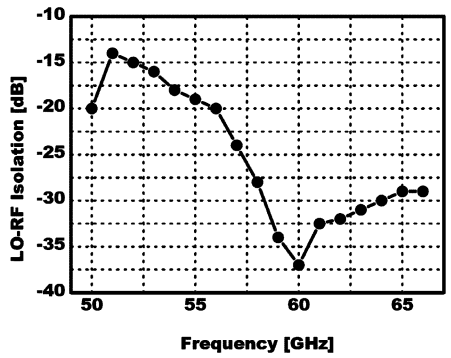

Fig. 6. Measured LO-RF isolation characteristics.

module output power level is fixed and not adjustable, a variable attenuator is added to the RF port while the rest of the test setup is identical to the LO port. The output IF signal is measured using differential 150 μm probes through the bias-tee, where one IF port is connected to 50 Ω for termination, while the other IF port is connected to a spectrum analyzer. The loss of probes, bias-tees, coaxial cables, and the waveguide connecters were measured separately and used to correct the measured results. The measured results are accurate to within ± 1 dB. The measured and simulated output IF power versus the input RF power at 0 dBm LO power is shown in Fig. 5(a), where the input referred to as 1 dB compression again is up to 2 dBm. The measured and simulated conversion gain values versus the LO power at 58 GHz with RF signal at 60 GHz are shown in Fig. 5(b), which shows that the single-ended conversion gain is 1 dB at 0 dBm LO power. The discrepancy of 2 dB between measurement and simulation is likely due to the accuracies of the measurement system (± 1 dB), and the modeling of MOS transistor at high frequencies. The measured LO-RF isolation is better than -37 dB, as shown in Fig. 6. Besides, the measured 3 dB RF and IF bandwidth of the mixer are 6.3 GHz and 400 MHz, respectively. The simulated SSB noise figure of 10 dB is expected, and the fabricated mixer drains 3 mA from a power supply of 1.2 V.

TABLE I
PERFORMANCE SUMMARIES OF THE PROPOSED MIXER AND COMPARISONS WITH OTHER PUBLISHED MIXERS

Ref.	*This work*	[1]	*[2]*	*[3]*
Tech.	$0.13\mu m$ $CMOS$	$0.13\mu m$ $CMOS$	$90\ nm$ $CMOS$	$0.13\mu m$ $CMOS$
Topology	Current-mode; active single ended	Voltage-mode; active single ended	Voltage-mode; resistive single ended	Voltage-mode; active balanced
RF Freq.	60 GHz	60 GHz	60 GHz	60 GHz
IF Freq.	2 GHz	2 GHz	2 GHz	0
Conv. gain	$1\ dB$	$-2\ dB$	$-11.6\ dB$	$28^{*}\ dB$
LO Power	$0\ dBm$	$0\ dBm$	$4\ dBm$	$--$
P_{1dB}	$2\ dBm$	$-3.5\ dBm$	$6\ dBm$	$-22.5\ dBm$
Power diss.	3 mW	2.4 mW	$--$	9 mW
Area (mm^2)	1.4×1.0	1.6×1.7	2.0×2.0	$0.3 \times 0.4^{**}$

* Voltage gain ** Active area only (not include balun and DC & RF pads)

Finally, the measured performance of the fabricated mixer is summarized in Table I, where comparisons with other published 60 GHz mixers are also provided. From Table I, the proposed current-mode mixer can achieve high linearity and a higher conversion gain with low LO power while, at the same time, achieving a smaller chip area by reducing the transmission lines used in the proposed mixer.

IV. CONCLUSION

This letter has proposed the fabrication and analysis of a CMOS quadrature-balanced current-mode mixer based on a self-switching device. An area-efficient onchip 90° branch-line hybrid coupler is designed to combine the LO and RF signals with an isolation better than -37 dB. The measurement results have shown that the proposed current-mode mixer is suitable for the applications of low-voltage and lower-power RF communication systems. Future research will be conducted to design a complete 60 GHz CMOS front-end receiver using the proposed mixer and followup 2 GHz IF amplifier to efficiently combine the IF branches.

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