Investigation of Coulomb Mobility in Nanoscale Strained PMOSFETs

William Po-Nien Chen, Pin Su, *Member, IEEE*, and Ken-Ichi Goto, *Member, IEEE*

***Abstract*—This paper provides an experimental assessment of Coulomb scattering mobility for advanced strained devices. By accurate short-channel mobility extraction, we examine the impact of process-induced uniaxial strain on Coulomb mobility in short-channel pMOSFETs. Our extracted Coulomb mobility shows very weak stress dependency at room temperature. This finding has also been verified in both long- and short-channel devices by the four-point wafer bending measurement. Therefore, in order to maximize the process-induced strain efficiency on nanoscale pMOSFETs, lower surface impurity concentration is suggested to avoid the Coulomb mobility domination in carrier transport.**

***Index Terms*—Coulomb mobility, MOSFET, strained silicon.**

I. Introduction

UNIAXIAL strained-Si technology is critical to transistor performance in state-of-the-art CMOS technology [1], [2], [8]. The improvement of current drive shows strong correlation with low-field mobility enhancement by uniaxial strain [2]. However, in order to suppress the short-channel effect for device scaling, halo implantation is widely used. With shrinking gate length, halo profiles begin to merge and result in higher effective bulk concentration. Recently, several studies [3]–[8] have reported degraded carrier mobility for short-channel devices and pointed out the increasing importance of Coulomb scattering. Whether Coulomb mobility can be enhanced by process-induced strain is crucial to device design and merits investigation.

Weber and Takagi [3] have demonstrated that the mobility limited by substrate impurity scattering is still enhanced by a strain process in long-channel strained nFETs ($L_G = 10\ \mu$m). However, similar studies have not been performed in PMOSFET, especially for short-channel devices. Therefore, further examination on Coulomb mobility is needed for PMOSFET.

In this paper, we investigate the Coulomb mobility for short-channel PMOS devices with process-induced uniaxial strain at room temperature. The Coulomb mobility in the short-channel region under compressive and neutral uniaxial local stress conditions is carefully characterized by split capacitance–voltage (C–V) method and Matthiessen's rule. In order to further verify our experimental results, we have also utilized the four-point mechanical bending technique on both short- and long-channel devices.

Manuscript received June 26, 2007; revised June 4, 2008. Current version published September 26, 2008. This work was supported in part by the National Science Council of Taiwan under Contract NSC 95-2221-E-009-327-MY2, in part by the Ministry of Education under the ATU program, and in part by the Taiwan Semiconductor Manufacturing Company. The review of this paper was arranged by Editor Dr. Daniel Herr.

W.P.-N. Chen is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 30013, Taiwan, R.O.C., and also with the Taiwan Semiconductor Manufacturing Company, Science-Based Industrial Park, Hsinchu 300, Taiwan, R.O.C. (e-mail: williamchen.ee93g@nctu.edu.tw).

P. Su is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 30013, Taiwan, R.O.C.

K.-I. Goto is with the Taiwan Semiconductor Manufacturing Company, Science-Based Industrial Park, Hsinchu 300, Taiwan, R.O.C.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNANO.2008.2004771

II. Device Fabrication

P-channel MOSFETs with channel direction $\langle 110 \rangle$ with neutral and compressive uniaxial *c*ontact *e*tch *s*top *l*ayer (CESL) were manufactured based on state-of-the-art CMOS technology on 300-mm p-type (1 0 0) silicon substrate. Shallow trench isolation (STI) was patterned to define the active region. Then, an ultrathin oxide was grown on the surface of the wafer. The polygate was implanted with heavily doped P-type species after polydeposition and postannealed to increase gate activation rates. Then, ultrashallow *h*eavily *d*oped *d*rain (HDD) implant, spacer formation, source and drain implant, postimplantation annealing, and back-end process were implemented sequentially.

For comparison purpose, films with neutral and compressive stress were deposited on PMOS to stop the etching of contact, respectively, at CESL deposition stage, as shown in Fig. 1. The compressive film may transfer significant compressive stress to the channel region, modulating silicon subbands and carrier populations, and altering carrier mobility [2]. The device ON–OFF performance is boosted $\sim$35% by compressive uniaxial stressors in the short-channel region.

Effective gate length ranges from 950 to 45 nm with gate width equal to 1 μm. Special transistor arrays were designed to provide sufficient area for split C–V measurement. In addition, it is known that parasitic capacitance components play an important role in short-channel devices and affect the accuracy of the extraction result. Therefore, calibration test keys were also designed to exclude the parasitic effects.

In order to reproduce the stress environment by local compressive stressors, a four-point mechanical bending tool was used to apply external stress on both long- and short-channel devices. The compressive stress level is around -230 MPa based on the meter reading.

III. Stress Simulation

In order to explain how CESL stressor transfers stress to the channel region, 2-D stress profiles induced by strained CESL were determined by technology computer-aided design (TCAD) stress simulation. In order to accurately reconstruct the device scheme, all major front-end processes from the shallow trench

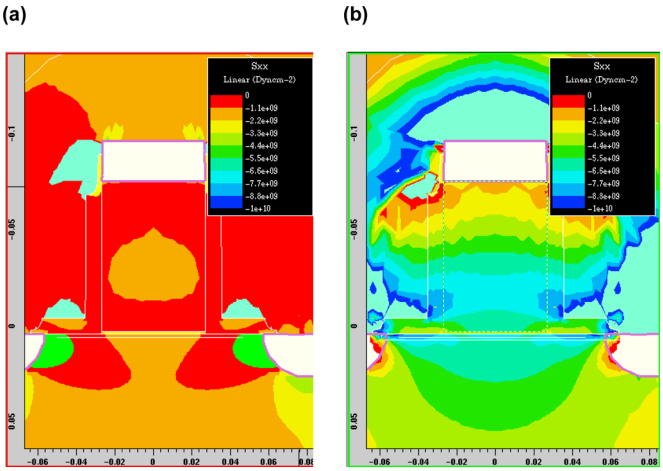


Fig. 1. Stress contours by TCAD simulation. (a) Neutral CESL. (b) Compressive CESL. The gate length equals 54 nm. Average stress levels along the channel direction are –0.153 GPa and –0.662 GPa for (a) and (b), respectively.

isolation to the rapid thermal annealing were included. The thermal budget and temperature profiles during processing have been well calibrated. The corresponding simulation geometries were also calibrated from TEM cross-section images.

PMOS devices with neutral and compressive CESL stressors are under investigation. The layout effects (e.g., polyspacing effect) have been considered in this simulation. In order to investigate the stress dependence on device geometry, MOSFET schemes at different gate lengths have been constructed.

Fig. 1(a) and (b) shows the simulated stress contours with intrinsic and compressive CESL films, respectively. The gate length for both devices is 54 nm. Note that the stress level, which is shown in Fig. 1, represents the average stress over the volume of the silicon channel (depth = 10 A and length = gate length). The average stress levels along the channel direction (S_{xx}) are -0.153 GPa and -0.662 GPa for neutral and compressive CESL nitride films, respectively. The S_{xx} of neutral CESL is mainly contributed by the STI effect instead of the CESL effect. For compressive CESL, the corner effect and the direct CESL effect are responsible for S_{xx} in the short-channel device [17].

Fig. 2(a) and (b) shows the stress level [S_{xx} and S_{yy}, as shown in the inset of Fig. 2(a)] between long- and short-channel devices. In Fig. 2(a), the compressive CESL induces stronger compressive stress (S_{xx}) in the Si channel as gate length becomes shorter. It is mainly attributed to the corner and the direct CESL effect [17]. The corner effect is due to the interaction of the lateral-CESL and the bottom-CESL, resulting in compressive stress along the channel direction. The direct CESL effect is dominated by the bottom-CESL effect. In Fig. 2(b), the compressive CESL induces stronger tensile stress (S_{yy}) vertical to the Si surface as gate length becomes shorter. It is mainly due to the indirect CESL effect [17]. For long-channel devices, the indirect effect arises from the top-CESL; for short-channel devices, 49% of the total stress amount comes from the lateral-CESL, 29% from the top-CESL, and 21% from the bottom-CESL [17].

S. Thompson *et al.* [2] have shown that the mobility of PMOSFET with $\langle 110 \rangle$ channel direction on (0 0 1) wafer prefers compressive S_{xx} (longitudinal) and tensile S_{yy} (out-of-plane) stress based on piezoresistance. The simulation results of Fig. 1 and 2 can explain how the compressive CESL affects the hole mobility.

IV. Characterizations and Extraction

To accurately extract the carrier mobility, the split C–V method [10], [11], [16] is used to characterize the inversion charge density ($Q_{\rm inv}$) and bulk charge density (Q_b) for long- and short-channel devices.

The characterized gate-to-channel capacitance with floating bulk terminal ($C_{\rm gc}$) is calibrated by considering the parasitic components such as overlap capacitance and fringing capacitance [12], and then, $Q_{\rm inv}$ is obtained by integrating the whole $C_{\rm gc}$ curve from flat-band voltage. The gate-to-channel capacitance with source/drain/bulk tied together ($C_{\rm gg}$) is also calibrated using the same calibration procedure with $C_{\rm gc}$. Then, Q_b can be obtained. The characterized $C_{\rm gc}$ data at different gate lengths with neutral CESL are carefully calibrated by considering parasitic components, such as overlap capacitance and fringing capacitance [9], [11], [12]. It is worth noting that the inner fringing capacitance ($C_{\rm inov}$) shows no dependency on $L_{\rm EFF}$ at V_g larger than 0 V, which is consistent with [12].

The effective bulk doping concentration (N_a) from long to short channel is extracted by the North Carolina State University (NCSU) fitting program [13]. The information of N_a is important for the following extraction of Coulomb mobility. In order to exclude the parasitic source/drain series resistance ($R_{\rm sd}$) effect, the BSIM $R_{\rm sd}$ extraction method is adopted [14]. After $R_{\rm sd}$ is obtained, the ideal drain current can be derived from (1)

$$I_d({\rm int}) = \frac{I_d({\rm ext})}{1 - I_d({\rm ext}) \times \frac{R_{\rm sd}}{V_{\rm d}}} \tag{1}$$

where $I_d({\rm int})$ represents the intrinsic drain current, $I_d({\rm ext})$ represents the extrinsic drain current that includes the $R_{\rm sd}$ effect, and $R_{\rm sd}$ is the parasitic source/drain series resistance.

The physical polygate length ($L_{\rm phy}$) can be obtained from the in-line *s*canning *e*lectron *m*icroscopy (SEM) measurement (with accuracy within ± 2 nm) at polypatterned stage and the etching-induced length bias (ΔL), as shown in (2)

$$L_{\rm phy} = L_{\rm SEM} - \Delta L. \tag{2}$$

The overlap distance between poly and HDD region ($L_{\rm ov}$) is extracted by the split C–V method [10], [11]. Then, the effective channel length ($L_{\rm EFF}$) can be derived by subtracting $L_{\rm ov}$ from $L_{\rm phy}$. Finally, the total mobility can be extracted by (3)

$$\mu = \frac{I_{\rm d}({\rm int}) \cdot L_{\rm EFF}}{W \cdot Q_{\rm inv} \cdot V_{\rm d}} \tag{3}$$

where W represents the device width. Equation (3) represents the total mobility, from which the Coulomb mobility is extracted using Matthiessens's rule. It is worth noting that the total mobility is inversely proportional to $Q_{\rm inv}$ at high vertical field region, where the surface roughness scattering mechanism dominates.

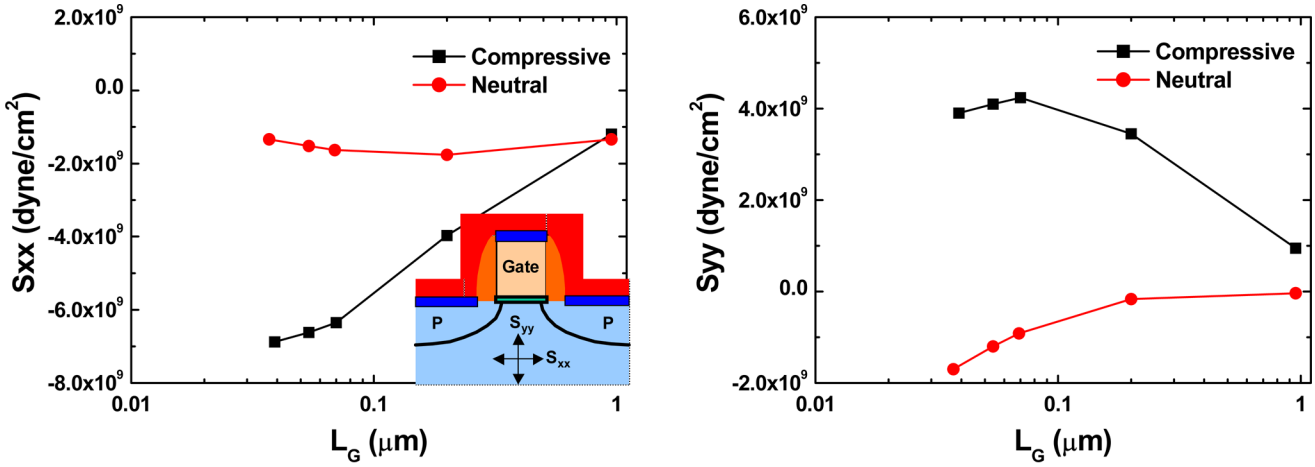


Fig. 2. Gate length dependence of (a) S_{xx} and (b) S_{yy} show that compressive CESL contributes stronger compressive S_{xx} and stronger tensile S_{yy} as L_G becomes shorter. (Inset: S_{xx} represents the stress along the Si channel direction, S_{yy} represents the stress vertical to the Si channel direction).

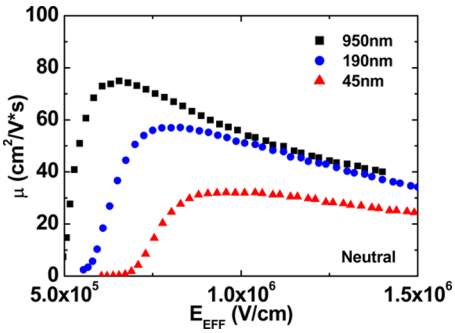


Fig. 3. PFET low field mobility versus the vertical electric field at different L_{EFF} with a neutral stressor.

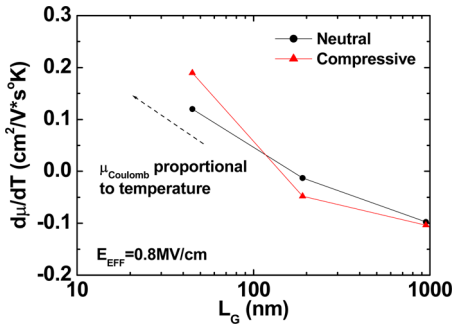


Fig. 4. Vertical field mobility sensitivity to temperature ($E_{\mathrm{EFF}} = 0.8\ \mathrm{MV/cm}$) versus L_{EFF} in PMOS. It shows that Coulomb mobility plays an important role in the short-channel region. When temperature is increased, the thermal velocity of carriers becomes faster. It means Coulomb scattering probability becomes lower and causes higher Coulomb mobility.

V. Results and Discussion

Fig. 3 shows the characterized mobility with neutral stressors at room temperature, where L_{EFF} equals 950 nm, 190 nm, and 45 nm, respectively. It can be seen that the high vertical field mobility is degraded as L_{EFF} shrinks. The abnormal behavior can be explained by halo pile-up, interface states, oxide charges, neutral defects, and remote Coulomb scattering [4], [6], [8], [10], [11], [14], [15].

Fig. 4 shows the temperature dependence of the total mobility when the effective vertical field is equal to 0.8 MV/cm. When temperature is decreased, the thermal velocity of carriers becomes reduced. Therefore, the interaction time between moving carriers and ionized impurity charges becomes longer. This means higher Coulomb scattering probability and lower Coulomb mobility. As gate length shrinks, the temperature sensitivity of the mobility increases, indicating that the Coulomb mobility plays a critical role in the short-channel region.

In order to extract the Coulomb mobility, we assume that the universal mobility curve follows the measurement data in the high-field region [4] from long- to short-channel lengths. Matthiessen's rule can then be used to extract the Coulomb mobility [4]. The extracted PMOS Coulomb mobility versus Q_{inv} is shown in Fig. 5. It can be seen that the Coulomb mobility decreases with channel length. The length dependence of Coulomb mobility comes from the nonuniform halo profiles. As channel length becomes shorter, the effective bulk charge increases and the Coulomb mobility decreases because of halo merge effect. To verify our mobility data, we fit it using the equation $\mu_{\mathrm{coulomb}} = AQ_{\mathrm{inv}}^{\alpha} N_a^{-\beta}$ [4], where A is a constant, α

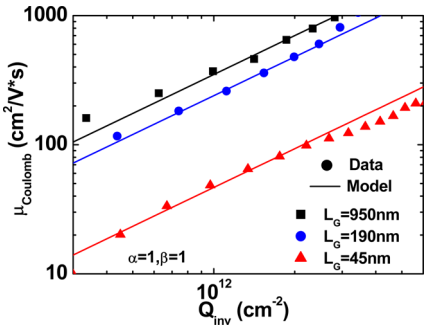
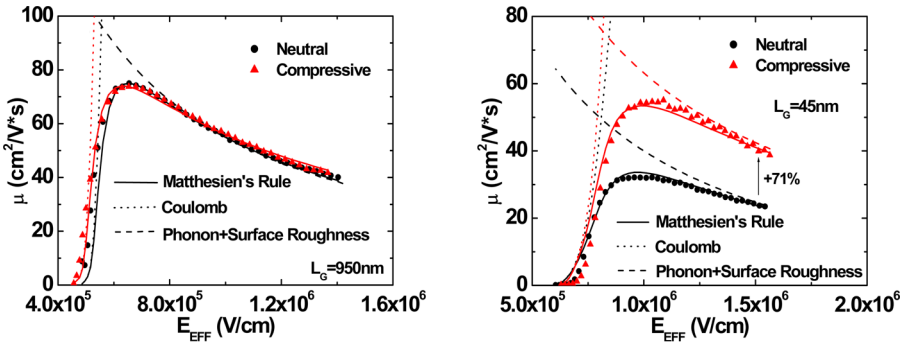


Fig. 5. Coulomb mobility data versus model in PMOS for long- and short-channel regions. Coulomb mobility becomes smaller as L_{EFF} shrinks because of higher N_a. A is a constant, α and β are both equal to 1, and N_a is extracted from NCSU fitting programs.



(a) (b)

Fig. 6. (a) PFET long-channel mobility ($L_{\rm EFF} = 950$ nm) with neutral and compressive CESL stressors. The mobility model matches with silicon data very well. Since the uniaxial stressor is only effective for short-channel devices, the long-channel mobility is almost the same under different neutral and compressive stressors. (b) PFET short-channel mobility ($L_{\rm EFF} = 45$ nm) with neutral and compressive CESL stressors. The extracted total mobility agrees with the model quite well. The 71% mobility enhancement for compressive stressor in the high vertical field region is mainly due to the uniaxial local compressive stress.

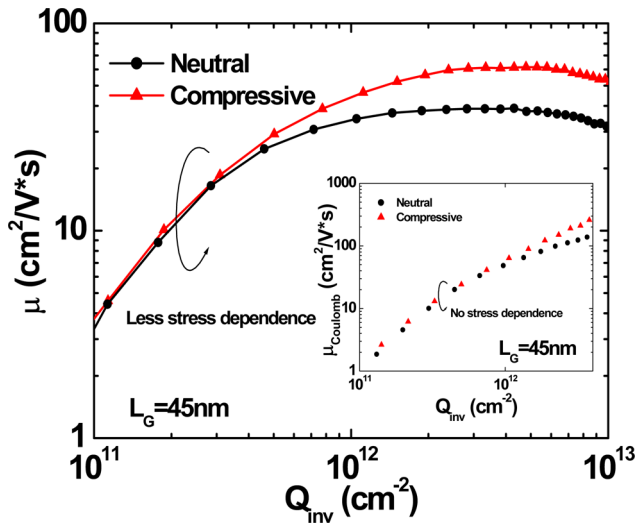


Fig. 7. PFET total mobility at low vertical field versus $Q_{\rm inv}$ under various stressors. Very little stress dependence is observed in the low field region, where Coulomb scattering mechanism dominates. (Inset: PFET Coulomb mobility extracted by Matthiessen's rule between neutral and compressive stressors. No stress dependence is observed in the short-channel region at room temperature.).

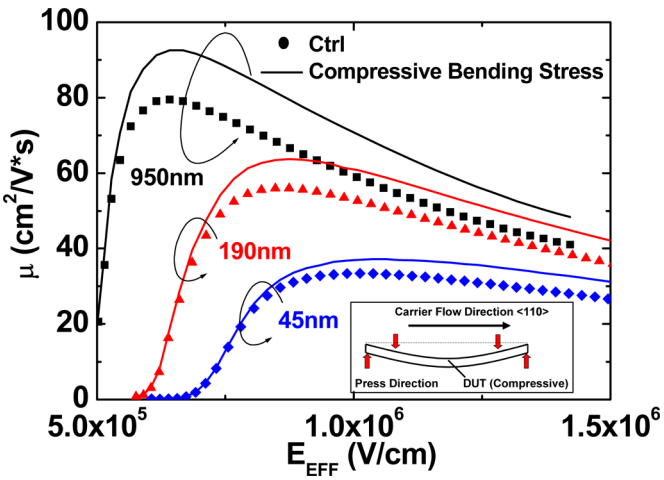


Fig. 8. PFET total mobility versus $E_{\rm EFF}$ after applying 230 MPa compressive bending stress on devices with different $L_{\rm EFF}$. Unlike the behavior of local stressors, significant mobility improvement can be observed from long- to short-channel devices in the high vertical field region because of global stress effect. (Inset: The schematic of the mechanical bending tool).

and β are both equal to 1, and N_a is extracted from NCSU fitting programs. The result shows a fairly good fit between the data and the Coulomb mobility model.

Fig. 6(a) shows that the long-channel total mobility with $L_{\rm EFF} = 950$ nm agrees with the model equation. Since the uniaxial stressor is only effective for short-channel devices, the long-channel mobility is almost the same between neutral and compressive stressors. Weber and Takagi used SiGe strained material under the silicon substrate with the stress being effective from long- to short-channel devices because of global stress effect [3]. Fig. 6(b) shows that for the short-channel device with $L_{\rm EFF} = 45$ nm, our extracted total mobility agrees with the model. The 71% mobility enhancement for the compressive stressor in the high vertical field region is mainly due to the uniaxial stress effect [2].

Fig. 7 shows the total mobility versus $Q_{\rm inv}$. It is observed that the PMOS mobility in the high vertical field region shows strong stress dependence. However, very little stress dependence is observed in the low vertical field region. The inset of Fig. 7 shows the extracted Coulomb mobility for neutral and compressive stressors using Matthiessen's rule. It indicates that the Coulomb mobility has almost no stress dependence at room temperature.

To further verify our observation, we have also utilized the four-point wafer bending measurement. The advantage of this method is that it can provide the same global stress level to devices with various dimensions. Based on the extracted mobility data under varying mechanical stress, we can determine whether the Coulomb mobility shows stress dependency and verify the result obtained from the local stressors. The inset of Fig. 8 shows the schematic of the mechanical bending tool. In this case, 230 MPa compressive stress is applied to the test device based on instrument reading. Fig. 8 shows the mobility versus effective vertical field for devices under global compressive bending stress. Unlike the behavior of local stressors, significant mobility improvement can be observed in long- and short-channel devices in the high vertical field region because

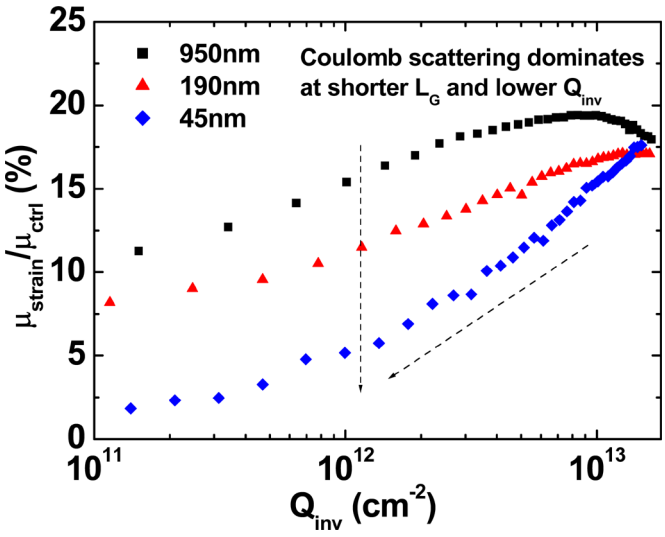


Fig. 9. PFET total mobility enhancement versus $Q_{\rm inv}$ by applying compressive mechanical stress on the devices with different $L_{\rm EFF}$.

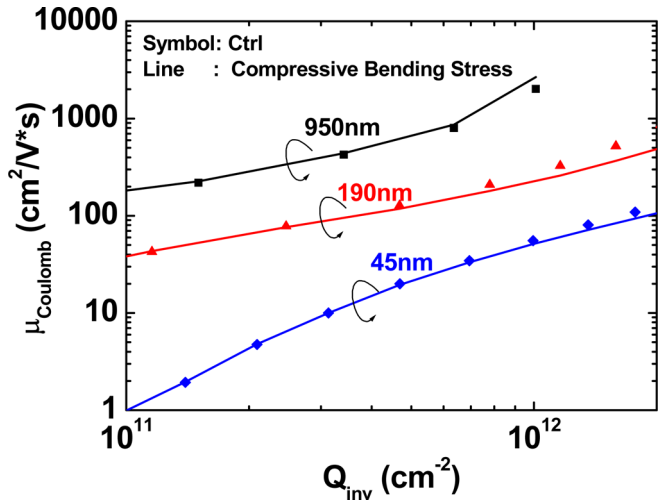


Fig. 10. PFET Coulomb mobility versus $Q_{\rm inv}$ by applying compressive mechanical stress on the devices with different $L_{\rm EFF}$. No stress dependence is observed for both long- and short-channel Coulomb mobility, which is consistent with the findings from local stressors.

of the global stress effect. It should be noted that $R_{\rm sd}$ has been well calibrated during mobility extraction.

Fig. 9 shows the total mobility enhancement percentage from long-channel to short-channel devices in the wafer bending experiment. In the high vertical field region, the mobility enhancement is around 15% and is independent of the channel length. It indicates that devices with various dimensions have a similar stress level under the global stress and that the phonon scattering mechanism still dominates in this higher vertical field region. However, the total mobility enhancement decreases with $Q_{\rm inv}$. Moreover, the total mobility enhancement decreases with the channel length for a fixed $Q_{\rm inv}$. It indicates that the Coulomb mobility has less stress dependence. In Fig. 10, the extracted Coulomb mobility, indeed, shows negligible stress dependency for either long-channel or short-channel devices, verifying our previous observation in Fig. 7. According to [3], it is plausible that the stress sensitivity of the bulk charge scattering is counterbalanced by the interface charge scattering. However, the actual root cause is still unknown and merits further investigation in the future.

VI. Conclusion

By using the split C–V method and careful calibration of parasitic components on the short-channel devices with local stressors, we have observed that the Coulomb mobility in PMOS shows almost no stress dependency at room temperature. This observation has also been verified by the four-point wafer bending measurement. Therefore, in order to maximize the process-induced strain efficiency on nanoscale pMOSFETs, lower surface impurity concentration is suggested to avoid the Coulomb mobility domination in carrier transport.

References

[1] Z. Luo, N. Rovedo, S. Ong, B. Phoong, M. Eller, H. Utomo, C. Ryou, H. Wang, R. Stierstorfer, L. Clevenger, S. Kim, J. Toomey, D. Sciacca, J. Li, W. Wille, L. Zhao, L. Teo, T. Dyer, S. Fang, J. Yan, O. Kwon, D. Park, J. Holt, J. Han, V. Chan, J. Yuan, T. Kebede, H. Lee, S. Kim, S. Lee, A. Vayshenker, Z. Yang, C. Tian, H. Ng, H. Shang, M. Hierlemann, J. Ku, J. Sudijono, and M. Ieong, "High performance transistors featured in an aggressively scaled 45 nm bulk CMOS technology," in *Proc. Symp. VLSI Technol.*, 2007, pp. 16–17.

[2] S. E. Thompson, M. Armstrong, C. Auth, M. Alavi, M. Buehler, R. Chau, S. Cea, T. Ghani, G. Glass, T. Hoffman, C. H. Jan, C. Kenyon, J. Klaus, K. Kuhn, Z. Ma, B. Mcintyre, K. Mistry, A. Murthy, B. Obradovic, R. Nagisetty, P. Nguyen, S. Sivakumar, R. Shaheed, L. Shifren, B. Tufts, S. Tyagi, M. Bohr, and Y. E. Mansy, "A 90-nm logic technology featuring strained-silicon," *IEEE Trans. Electron Devices*, vol. 51, no. 11, pp. 1790–1797, Nov. 2004.

[3] O. Weber and S. Takagi, "New findings on Coulomb scattering mobility in strained-Si nFETs and its physical understanding," in *Proc. Symp. VLSI Technol.*, 2007, pp. 130–131.

[4] H. M. Nayfeh, C. W. Leitz, A. J. Pitera, E. A. Fitzgerald, J. L. Hoyt, and D. A. Antoniadis, "Influence of high channel doping on the inversion layer electron mobility in strained silicon n-MOSFETs," *IEEE Electron Device Lett.*, vol. 24, no. 4, pp. 248–250, Apr. 2003.

[5] F. Gamiz, J. B. Roldan, J. A. Lopez-Villanueva, and P. Cartujo, "Coulomb scattering in strained-silicon inversion layers on $Si_{1-x}Ge_x$ substrates," *Appl. Phys. Lett*, vol. 69, pp. 797–799, 1996.

[6] A. Cros, K. Romanjek, D. Fleury, S. Harrison, R. Cerutti, P. Coronel, B. Dumont, A. Pouydebasque, R. Wacquez, B. Duriez, R. Gwoziecki, F. Boeuf, H. Brut, G. Ghibaudo, and T. Skotnicki, "Unexpected mobility degradation for very short devices: A new challenge for CMOS scaling," in *IEDM Tech. Dig.*, San Francisco, CA, 2006, pp. 1–4.

[7] K. Rim, S. Narasimha, M. Longstreet, A. Mocuta, and J. Cai, "Low field mobility characteristics of sub-100nm unstrained and strained Si MOSFETs," in *IEDM Tech. Dig.*, 2002, pp. 43–46.

[8] F. Andrieu, T. Ernst, F. Lime, F. Rochette, K. Romanjek, S. Barraud, C. Ravit, F. Boeuf, M. Jurczak, M. Casse, O. Weber, L. Brevard, G. Reimbold, G. Ghibaudo, and S. Delenibus, "Experimental and comparative investigation of low and high field transport in substrate- and process-induced strained nanoscaled MOSFETs," in *Proc. Symp. VLSI Technol.*, 2005, pp. 176–177.

[9] H. Ohta, H. Fukutome, T. Sakuma, A. Hatada, K. Ohkoshi, K. Ikeda, T. Miyashita, T. Mori, and T. Sugii, "Novel thin sidewall structure for high performance bulk CMOS with charge-assisted source-drain-extension," in *Proc. Symp. VLSI Technol.*, 2007, pp. 120–121.

[10] K. Romanjek, F. Andrieu, T. Ernst, and G. Ghibaudo, "Improved split C–V method for effective mobility extraction in sub-0.1-μm Si MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 583–585, Aug. 2004.

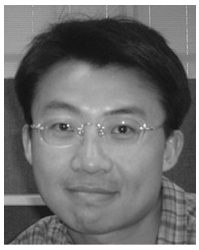
[11] K. Romanjek, F. Andrieu, T. Ernst, and G. Ghibaudo, "Characterization of the effective mobility by split $C(V)$ technique in sub 0.1 mm Si and SiGe PMOSFETs," *Solid State Electron.*, vol. 49, pp. 721–726, 2005.

[12] F. Pregaldiny, C. Lallement, and D. Mathiot, "A simple efficient model of parasitic capacitances of deep-submicron LDD MOSFETs," *Solid State Electron.*, vol. 46, pp. 2191–2198, 2002.

[13] J. R. Hauser *et al.*, in *Proc. Charact. Metrol. ULSI Technol.: 1998 Int. Conf.*, 1998, p. 235.
[14] W. P. N. Chen, P. Su, J. S. Wang, C. H. Lien, C. H. Chang, K. Goto, and C. H. Diaz, "A new series resistance and mobility extraction method by BSIM model for nano-scale MOSFETs," in *Proc. VLSI-TSA-Technol.*, 2006, pp. 143–144.
[15] F. Aandrieu, T. Ernst, C. Ravit, M. Jurczak, G. Ghibaudo, and S. Deleonibus, "In-depth characterization of the hole mobility in 50-nm process-induced strained MOSFETs," *IEEE Electron Device Lett.*, vol. 26, no. 10, pp. 755–757, Oct. 2004.
[16] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. New York: Wiley, 2006.
[17] S. Orain, V. Fiori, D. Villanueva, A. Dray, and C. Ortolland, "Method for managing the stress due to the strained nitride capping layer in MOS transistors," *IEEE Trans. Electron Devices*, vol. 54, no. 4, pp. 814–821, Apr. 2007.

William Po-Nien Chen received the B.S. and M.S. degrees in electrical engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1999 and 2003, respectively.

In 2004, he joined Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu. His current research interests include physics of semiconductor devices, nanodevice characterizing/modeling, and the carrier transport mechanism.



Pin Su (S'98–M'02) received the B.S. and M.S. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, R.O.C., and the Ph.D. degree from the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, in 2002.

From 1997 to 2003, he was engaged in doctoral and postdoctoral research in physics and modeling of silicon-on-insulator devices in the Device Group of UC, Berkeley. Since August 2003, he has been with the Department of Electronics Engineering, National Chiao Tung University, where he is currently an Associate Professor. He is the author or coauthor of more than 60 technical papers. His current research interests include silicon-based nanoelectronics, advanced CMOS devices, and device modeling.

Ken-Ichi Goto (M'97) received the B.S., M.S., and Ph.D. degrees from Tohoku University, Sendai, Japan, in 1989, 1991, and 1998, respectively, all in electronics engineering.

In 1991, he joined Fujitsu Laboratories, Ltd., Atsugi, Japan, where he was engaged in research on silicide process for deep submicron CMOS ULSI devices. In 2004, he joined Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, Taiwan, R.O.C. His current research interests include high-performance deca-nano scaling CMOS devices, and shallow junction technology and processes.

Dr. Goto is a member of the Japan Society of Applied Physics and the IEEE Electron Devices Society.