A Symbol-Rate Timing Synchronization Method for Low Power Wireless OFDM Systems

Jui-Yuan Yu, Ching-Che Chung, and Chen-Yi Lee

***Abstract*—This work addresses power reduction and performance improvement for wireless orthogonal frequency-division multiplexing (OFDM) systems using a dynamic sample-timing controller (DSTC) and phase-tunable clock generator (PTCG). The receiver, applying the proposed DSTC algorithm, searches for the optimal sampling phase at the symbol rate, instead of the Nyquist rate (or higher), to reduce the extra power consumed in high-rate operations. The proposed PTCG circuits provide the desired clock phase for optimum sampling to improve system performance. Both the DSTC and the PTCG are evaluated in a multibandt OFDM (MB-OFDM) ultra-wide-band system. Simulation results indicate that the overall system performance is improved by 1.7-dB signal-to-noise ratio at a packet error rate of 8% and the total baseband power is reduced by 40%.**

***Index Terms*—Dynamic sample-timing controller (DSTC), orthogonal frequency-division multiplexing (OFDM), phase-tunable clock generator (PTCG), synchronization, ultra-wide-band.**

I. Introduction

TRADEOFF between system performance and power dissipation is one of the most critical issues in the design of a wireless portable device. Timing synchronization plays an important role in ensuring good signal decoding performance, since it determines the sampling timing and frequency of the analog-to-digital converter (ADC) on incoming signals or packets. Existing design approaches apply multirate sampling (at Nyquist rate or higher than $4\times$ symbol rate [1]–[3]) to the incoming waveform with a fixed high-rate clock source that drives an ADC circuit. Those high-rate sampled signals are then calculated by an interpolation algorithm [4] to yield a symbol-rate signal stream for data decoding. This design methodology to designing power-thirsty portable devices is facing increasing difficulty, because both the ADC circuits and the interpolation circuits are operated at a higher processing rate, resulting in higher power consumption.

To enable power reduction with symbol-rate sampling, both Mueller–Muller detection (MMD) [5] and MMD-based timing recovery methods [6] have been proposed under a pulse amplitude modulation (PAM) scheme for best sampling timing search within a sample period. The literature explores the timing synchronization issue in orthogonal frequency-division multiplexing (OFDM) systems based on the best block-boundary search for each fast Fourier transform (FFT) window [7], [8]. However, those studies [7], [8] do not guarantee that the signals in each block are sampled at the best sampling timing. Accordingly, multirate sampling schemes [1], [2] have been developed to maintain system performance; hence the high-rate operations significantly increase power dissipation.

To maintain system performance and, in the meantime, to reduce power dissipation, this work presents a dynamic sample-timing control (DSTC) scheme for symbol-rate synchronization in OFDM systems, where the optimal sampling timing within a symbol-period interval can be calculated. Unlike multirate sampling methods [1]–[3], this DSTC requires aided circuits in a clock source design to generate a phase-tunable clock waveform that corresponds to the best sampling instance as calculated by the DSTC. A digitally-controlled oscillator (DCO) design concept [9] is applied to the phase-tunable clock generator (PTCG) design to enable this symbol-rate DSTC [10] for low-power wireless applications.

The rest of this paper is organized as follows. Section II presents an overview of the proposed system. Section III then derives the proposed DSTC algorithm. Section IV shows the design of the proposed PTCG. Section V analyzes the system performance and the hardware design complexity of our proposal.

II. System Overview

OFDM signals transformed by an N-point discrete inverse Fourier transformation (IDFT) after digital-to-analog conversion (DAC) are expressed as

$$x_T(t) = \sum_{n=-\infty}^{\infty} \left(X[k] e^{j\frac{2\pi kn}{N}} \right) \cdot \mathrm{sinc}(t - nT_s) \qquad (1)$$

where $X[k]$ is an information symbol stream with phase-shift keying (PSK) or quadrature amplitude modulation (QAM) encoded, and T_s is the sample period. In up/down and analog/digital data conversions, the signal suffers from any nonideal hardware distortion, including every filter response (f_T and f_R) from both the transmitter (TX) and the receiver (RX) sides. Therefore, down-converted signals in a receiver are given by

$$x_R(t) = [x_T(t) * f_T(t) * f_R(t)] \cdot e^{j2\pi \cdot f_{\mathrm{CFO}} \cdot t} + w(t) * f_R(t) \qquad (2)$$

where $f(t) = f_T(t) * f_R(t)$, f_{CFO} is the carrier frequency offset (CFO) between the TX and RX, and $w(t)$ is additive white Gaussian noise (AWGN). After the ADC circuits, signals in digital time domain are given by

$$x_{R;\varepsilon}[n] = \sum_n x_R(t) \cdot \delta\left[t - (n - \varepsilon)T_s\right], \qquad \varepsilon \in R,\ |\varepsilon| < \frac{1}{2} \qquad (3)$$

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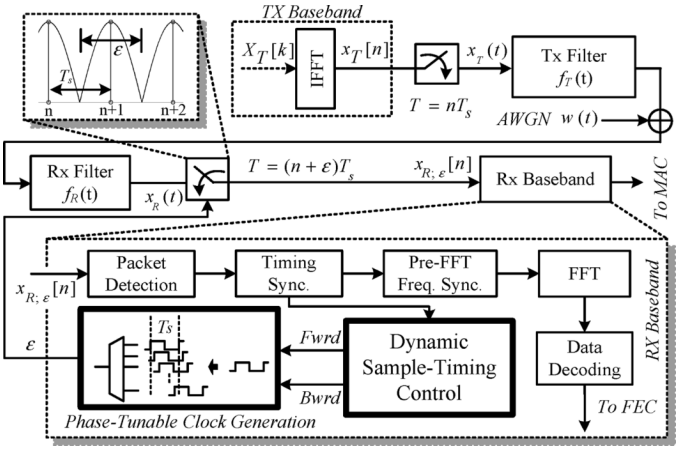

Fig. 1. Block diagram of the proposed baseband receiver with the aid of the proposed DSTC and PTCG.

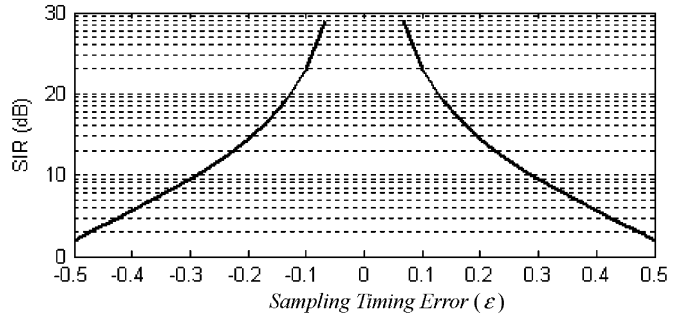

Fig. 2. SIR power ratio versus sampling timing error ε with $f(t) = \text{raised} - \text{cosine filter}$ (roll-off factor 0.5).

where ε is a sampling phase offset fraction of the sample period, and $\delta(t)$ is an impulse function. Once a packet has been detected, the DSTC is activated to provide commands to the PTCG to generate the optimal clock phase for signal sampling in the ADCs. Then, the signals follow the conventional decoding flows. Fig. 1 depicts the system diagrams and their operations.

III. DSTC

The goal of this algorithm is to determine a signal sampling instance with the sampling rate equal to the symbol rate, $T = T_s$, where the intersymbol interference (ISI) associated with filter pulse responses is minimized. Hence, the optimum sampling instance ε_{opt} is defined as

$$\varepsilon_{\text{opt}} = \arg\max_{\tau} \left(\frac{|f_\varepsilon[0]|^2}{\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} |f_\varepsilon[n]|^2} \right) = \arg\max_{\tau}(\text{SIR}_\varepsilon) \quad (4)$$

where $f[(n-\varepsilon)T_s]$ is written in a simplified notation as $f_\varepsilon[n]$ and the ratio is the signal-to-ISI power ratio (SIR). Thus, the ε_{opt} is determined when the minimum ISI power sum appears in the denominator of (4). In other words, the SIR of the sampled signals becomes maximized when the optimum sampling instance is chosen. Here, $f(t)$ is replaced by a raised-cosine filter impulse response with a roll-off factor of 0.5 as shown in Fig. 2. A noncalibrated sampling timing error may yield low signal-integrity data even in the absence of noise, implying there is system performance degradation when sampling time is not well-calculated.

To find the optimum sampling time ε_{opt}, the ratio given by (4) cannot be calculated directly because both the $f_T(t)$ and the $f(t) = f_T(t) * f_R(t)$ are unknown to any receivers. Therefore, an alternative approach, the maximum absolute-squared sum equivalent to (4) and also hardware realizable, is examined. Accordingly, the absolute-squared-sum of the received signals is

$$|x_{R;\varepsilon}[n]|^2 = \left| \sum_m x_{T;\varepsilon}[n-m] f_\varepsilon[m] e^{j(2\pi f_{\text{CFO}})(n+\varepsilon)T_s} \right|^2 + |w_{B;\varepsilon}[n]|^2 + 2\text{Re}\left\{ w_{B;\varepsilon}[n] \sum_m x_{T;\varepsilon}[n-m] f_\varepsilon[m] e^{j(2\pi f_{\text{CFO}})(n+\varepsilon)T_s} \right\} \quad (5)$$

where $w_{B;\varepsilon}$ is the band-limited zero-mean additive noise sampled at timing offset ε with $w_B = w(t) * f_R(t)$. Notably, $w_{B;\varepsilon}$ is assumed to be independent of transmitted signals, and the expected value of the received signals $x_{R;\varepsilon}$ is

$$E\left\{ |x_{R;\varepsilon}[n]|^2 \right\} = E\left\{ \left| \sum_m x_{T;\varepsilon}[n-m] f_\varepsilon[m] \right|^2 \right\} + \sigma^2_{B;w} \quad (6)$$

where $\sigma^2_{B;w}$ represents the power of the color noise $w_{B;\varepsilon}$. The absolute-function operation suppresses the CFO factor. Therefore, the expected received signal power is composed of the transmitted signals filtered by the $f(t)$ and the band-limited noise power. The effects of $f(t)$ on the transmitted signals are expressed as main signal taps $f[n]|_{n=0}$ and their filter interference $f[n]|_{n\neq 0}$. Moreover, the expected power $E\{|x_{T;\varepsilon}[n]|^2|\}$ may be assumed to be a constant, say unit power, because every received signal power is adjusted by applying an automatic gain control (AGC) mechanism, thus normalizing the signal power to the dynamic range of the ADC. For simplicity $E\{|x_{T;\varepsilon}[n]|^2|\} = E\{|X_{T;\varepsilon}[n]|^2|\} = 1$ is defined. Equation (6) becomes

$$E\left\{ |x_{R;\varepsilon}[n]|^2 \right\} = |f_\varepsilon[0]|^2 + \sum_{m\neq 0} |f_\varepsilon[m]|^2 + \sum_p \sum_{p\neq q} E\left\{ x_{T;\varepsilon}[n-p] x^*_{T;\varepsilon}[n-q] \right\} f_\varepsilon[p] f^*_\varepsilon[q] + \sigma^2_{B;w}. \quad (7)$$

These information symbols are assumed to be independent, and then $E\{x_{T,\varepsilon}[n-p]x^*_{T,\varepsilon}[n-q]\} = E\{X_{T,\varepsilon}[k_1]X^*_{T,\varepsilon}[k_2]\}|_{k_1\neq k_2} = 0$. Therefore, (7) reduces to

$$E\left\{ |x_{R;\varepsilon}[n]|^2 \right\} = |f_\varepsilon[0]|^2 + \sum_{m\neq 0} |f_\varepsilon[m]|^2 + \sigma^2_{B;w}. \quad (8)$$

Consequently, the expected absolute-squared value of the received signals is determined by the power of both the filter response and AWGN. Based on the SIR definition, (8) is rewritten as

$$E\left\{ |x_{R;\varepsilon}[n]|^2 \right\} = (\text{SIR}_\varepsilon + 1) \cdot I_\varepsilon + \sigma^2_{B;w} \quad (9)$$

where $I_\varepsilon = \sum_{m\neq 0} |f_\varepsilon[m]|^2$ is the interference power of the filter tail. $(\text{SIR}_\varepsilon + 1) \cdot I_\varepsilon$ is defined as a characteristic function (CF) of the $E\{|x_{R;\varepsilon}[n]|^2\}$. A sharper CF curve is more easily recognized to calibrate the sampling timing errors. Fig. 3 plots a CF curve that corresponds to the raised-cosine filter of Fig. 2 in a noiseless channel. This finding reveals that the maximum $E\{|x_{R;\varepsilon}[n]|^2\}$ implies the optimum sampling instance

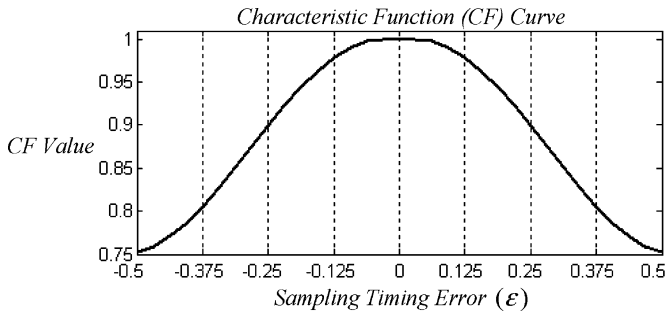

Fig. 3. CF for timing error search.

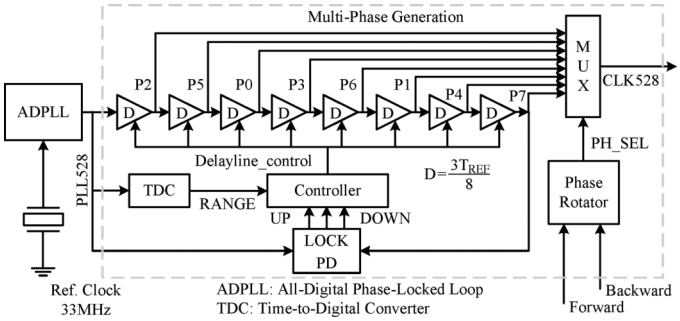

Fig. 4. Proposed PTCG.

$\varepsilon_{\rm opt}$. Therefore, the $\varepsilon_{\rm opt}$ search based on the SIR curve in (4) is transferred to the search of the maximum $E\{|x_{R;\varepsilon}[n]|^2\}$, i.e.,

$$\varepsilon_{\rm opt} = \arg\left(\max E\left\{|x_{R;\varepsilon}[n]|^2\right\}\right). \tag{10}$$

Each sample period is planned to be divided into eight phases, as shown in Fig. 3, for the finite hardware resolution and limited CF value degradation. Therefore, the optimal sampling timing from these eight positions always corresponds to a CF value that approaches the maximum value. The next section describes the design of an 8-phase clock generator.

IV. PTCG

An all-digital PTCG provides eight clock sampling candidates for phase selection, and outputs a specific one according to the $\varepsilon_{\rm opt}$ calculated in (10). This PTCG phase-tuning is achieved within a few cycles, and a clock output during this tuning period is glitch-free. Fig. 4 presents the proposed PTCG, which primarily consists of an all-digital pahse-locked loop (ADPLL), a TDC, and a cell-based delay line. Initially, the ADPLL is locked to the target frequency with the period $T_{\rm REF}$. This generated clock is used as a reference source for multiphase clock generation.

In the earlier delay-locked loop (DLL)-based multiphase clock generation approach [11], the TDC enables a delay line locked to a single clock period $(T_{\rm REF})$, giving a $T_{\rm REF}/8$ in each delay stage. In a high-speed cell-based DLL design, however, maintaining such a short delay and a high resolution simultaneously is difficult. Thus, in this design, the TDC measures three periods and makes the DLL lock to $3 \times T_{\rm REF}$. After the DLL is locked, each delay stage presents a $3 \times T_{\rm REF}/8$ delay. Hence, the minimum delay constraint for each delay stage (D) is extended to three times its original value. Moreover, the numbers in the numerator and denominator of the delay fraction 3/8 are not divisible by each other. As a result, the generated phase $\mathrm{P}_{n|n=0\sim7}$ after each delay cell presents a unique fraction of the period.

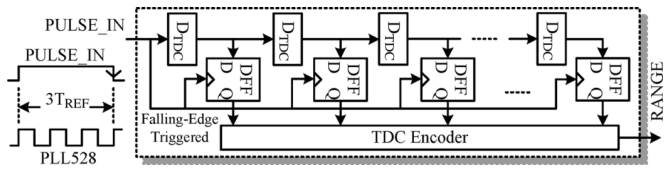

Fig. 5. Proposed TDC in the PTCG.

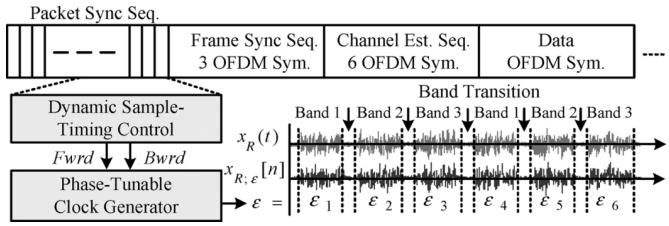

Fig. 6. Packet frame used for the DSTC computation.

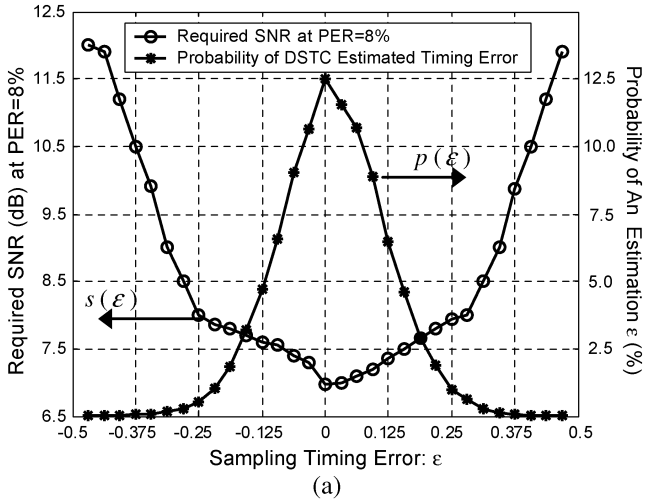

Fig. 7. (a) SNR required at $\mathrm{PER} = 8\%$ and the probability in estimating a timing error ε. (b) Overall system PER in our proposed DSTC and $2\times$-interpolation design schemes.

Fig. 5 shows the proposed TDC design architecture. The TDC takes the input PLL528 from the ADPLL. From this PLL528,

a PULSE_IN signal is internally generated with a pulsewidth of $3T_{\mathrm{REF}}$ as the TDC delay line input. A flip-flop is inserted between each pair of delay elements (D_{TDC}) in the delay line to latch data. The trigger event of all the flip-flops occurs at a PULSE_IN falling edge, and a latched data vector is encoded in a variable RANGE to the PTCG controller. According to the RANGE, the controller determines whether the periods of both PLL528 and PULSE_IN are correctly generated to avoid a false lock in this loop. Then, the phase detector (PD) of the PTCG continues fine tuning the delay of the delay elements to improve the accuracy of the output phase position.

An example is shown here. The delay between the PLL528 and P0 is $3 \times (3\ T_{\mathrm{REF}}/8) = 9 \times T_{\mathrm{REF}}/8$. Therefore, the P0 phase shift to the PLL528 is $T_{\mathrm{REF}}/8 = \{(9 \times T_{\mathrm{REF}}/8) \bmod T_{\mathrm{REF}}\}$. The clocks $\mathrm{P0} \sim \mathrm{P7}$ are generated accordingly. This PTCG takes the estimated timing error ε, represented by Forward or Backward, from the DSTC to select a proper clock phase for ADC sampling. To avoid glitches in CLK528, a Forward command is converted cyclically to several Backward commands by a glitch-free controller, say a phase rotator block.

V. Simulation and Measurement Results

The proposed DSTC and PTCG [10] are evaluated in a multiband OFDM (MB-OFDM)-based ultra-wide-band (UWB) system [12] with a low-density-parity-check (LDPC) code for error correction [13]. The signal bandwidth is 528 MHz with quadrature phase-shift keying (QPSK) and OFDM modulations, and the maximum data rate 480 Mbps is selected in the following simulations.

The dynamic timing recovery starts the $\varepsilon_{\mathrm{opt}}$ search right after a packet is detected. Each packet is composed of 21 OFDM symbols at the beginning of each preamble frame (Packet Sync Seq), which is applied to the DSTC as shown in Fig. 6. With those 21 identical OFDM symbols in the packet sync sequence, each of which gives an absolute-squared sum, and the sampling time ε is changed in the time slots between OFDM symbols. In other words, the PTCG changes its output clock phase only during the time slots associated with band transitions such that signals in each OFDM symbol are sampled with the same clock phase within an OFDM block period.

Fig. 7 plots the overall system performance. The curve denoted $s(\varepsilon)$ in Fig. 7(a) represents the signal-to-noise ratio (SNR) required to reach a packet error rate (PER) of 8%, where whole packets are sampled at a fixed and identical sampling offset ε. When the DSTC algorithm is applied, the optimal sampling instance is sought during the preamble. Before the end of the preamble, the DSTC decides which timing instance is the best for sampling in terms of system performance. Since the DSTC is operated in a noisy environment, it does not always choose the best sampling instance. Consequently, the curve $p(\varepsilon)$ represents the probability of the final decision made by the DSTC. Therefore, the SNR of our proposed system required to reach $\mathrm{PER} = 8\%$ is given by

$$\mathrm{SNR}_{\mathrm{PER}=8\%} = \int_{-0.5}^{0.5} s(\varepsilon) \cdot p(\varepsilon) \cdot d\varepsilon. \tag{11}$$

TABLE I
Summary of System Improvement and Power Reduction

	2× Oversampling Timing Sync.	This Work (DSTC+PTCG)
Required SNR @ PER=8%	9dB	7.3dB
ADC Sampling Rate	1056MHz	528MHz
ADC Power (I+Q paths) [14]	160mW × 2	70mW × 2
Timing Sync. Circuits	High-rate interpolation computation	DSTC (1.9mW) PTCG (10.9mW)

On the other hand, the system with the $2\times$ interpolation scheme takes two samples (pair sample) within each symbol period for timing synchronization. Although the signals from the interpolated pair-samples are noise-averaged, one of the pair samples always suffers from stronger ICI effects, leading to degrade the signal quality. Therefore, this interpolation-based approach does not outperform our proposal with signals sampled at the optimal instance. Moreover, the interpolation approaches in the existing literature does not support phase-tunable capability such that the probability function $p(\varepsilon)$ in this case can be regarded as a uniform distribution. Fig. 7(b) plots the system performances of the proposed DSTC-PTCG and the interpolation schemes. Fig. 8 shows both the simulated and measured waveforms from the PTCG design. This PTCG provides eight clock phases operating at 528 MHz, and each consecutive phase is separated by about 237 ps. As shown in Fig. 8(a), the output CLK528 is initially aligned to P5. When a command Forward is asserted, the selected output clock phase from the multiplexer (PH_SEL) counts down to zero and cyclically rotates back to P7 and P6. As the targeted clock phase is reached, a phase ready signal (PH_RDY) is activated to denote that the clock is updated from a new phase. To further explain the conversion of the Forward into several Backwards commands, P5 is again assumed to be initially selected as the system clock (CLK528), and the value of PH_SEL changes at the rising edge of the system clock, say P5. If $\mathrm{CLK528} = \mathrm{P5}$ is directly updated to $\mathrm{CLK528} = \mathrm{P6}$ before the rise of P6, a glitch may occur. Conversely, a change in CLK528 from $\mathrm{P_n}$ to $\mathrm{P_{n-1}}$ can avoid this glitch problem, except for the duty cycle change of CLK528 in the phase change intervals. The waveform in Fig. 8(b) plots the phase $\mathrm{P_n}$ and $\mathrm{P_{n+1}}$. The measured RMS and $\mathrm{P_k} - \mathrm{P_k}$ jitters are 30 s and 101 ps, respectively.

The resulting PTCG power is 10.9 mW [10] in the 0.13-μm standard CMOS process. Table I presents both the performance and the power reduction in this work. The scheme herein offers an improvement of approximately 1.7-dB SNR over that of the $2\times$ interpolation method. In this MB-OFDM UWB system, the symbol rate is 528 MHz, and the $2\times$ interpolation scheme requires a sampling rate of 1056 MHz in the ADC circuits. The estimated power reduction is from 160 mW × 2 to 70 mW × 2 (for both *I* and *Q* paths) if the ADC circuits in [14] are taken into account. When the baseband processor power 31.2 mW [10] is included, this reduced sampling rate results in a baseband power saving of $(160\times2-70\times2+31.2)\mathrm{mW}/(160\times2+31.2)\mathrm{mW} \fallingdotseq 40\%$ if the ADC [14] is calculated together. Note that the proposed symbol-rate synchronization method requires both the DSTC and PTCG circuits with power consumption of 1.9 and 10.9 mW, respectively. Fig. 9 presents a microphoto of this baseband test chip.

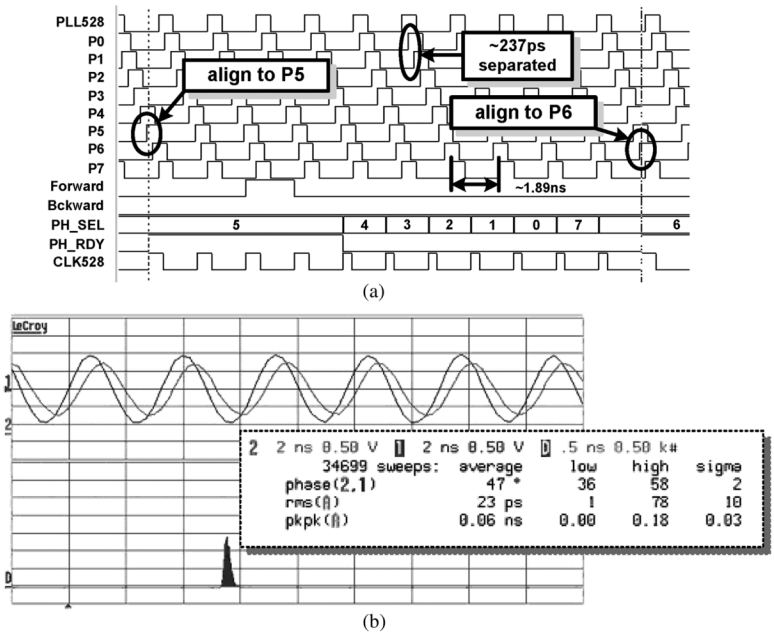

Fig. 8. Generated PTCG waveforms. (a) Simulated waveforms. (b) Measured waveforms.

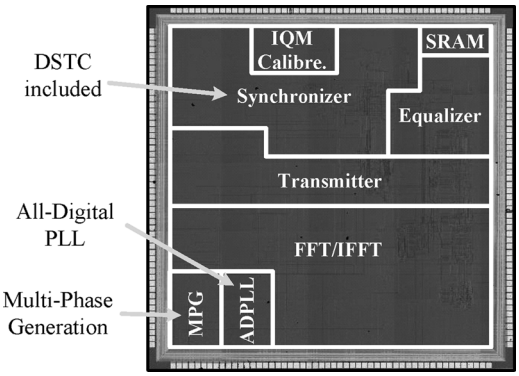

Fig. 9. Microphoto of the test chip in 0.13-μm standard CMOS technology.

VI. Conclusion

In this work, both the DSTC and the PTCG schemes are proposed to enable symbol-rate synchronization to reduce power consumption by preventing high-rate circuit operations. This proposal offers better signal sampling quality and enhances overall system performance compared to those interpolation-based solutions. In addition, this proposal has low design complexity with the low power feature, making it very suitable for realizing cost-effective OFDM-based wireless communications solutions.

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