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# InAs High Electron Mobility Transistors with Buried Gate for Ultralow-Power-Consumption Low-Noise Amplifier Application

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An InAs/$In_{0.7}Ga_{0.3}As$ composite channel high-electron-mobility transistor (HEMT) fabricated using the gate sinking technique was realized for ultralow-power-consumption low-noise application. The device has a very high transconductance of 1900 mS/mm at a drain voltage of 0.5 V. The saturated drain–source current of the device is 1066 mA/mm. A current gain cutoff frequency ($f_T$) of 113 GHz and a maximum oscillation frequency ($f_{max}$) of 110 GHz were achieved at only drain bias voltage $V_{ds} = 0.1$ V. The $0.08 \times 40\,\mu m^2$ device demonstrated a minimum noise figure of 0.82 dB and a 14 dB associated gain at 17 GHz with 1.14 mW DC power consumption. [DOI: 10.1143/JJAP.47.7119]

KEYWORDS: InAs/InGaAs, gate sinking, current gain cutoff frequency ($f_T$), ultralow power

Low-noise amplifiers (LNAs) with extremely low DC power consumption have always been considered as critical components for various emerging wireless communication applications including mobile radio systems and handheld imagers. Among all the possible technologies that meet the stringent system requirements, high-indium-content InP-based InAlAs/$In_{1-x}Ga_xAs$ high electron mobility transistors (HEMTs) are particularly promising because they provide higher electron mobility, higher saturation velocity, and higher sheet electron densities which lead to incomparable speed-power device performance with competing technologies such as GaAs HEMTs.[1–3)]

In general, high electron mobility and conductivity are essential for devices to have high drive currents at both low drain ($I_{DLIN}$) and high drain ($I_{DSAT}$) biases, which are very critical to maintain excellent RF performance with extremely low DC power consumption.[4,5)] In the effort of minimizing noise figure of devices, several approaches have been adopted, as described in the references. Since noise figure is directly related to the gate length ($L_g$) and gate resistance ($R_g$), reduction of these two parameters has been the principle in achieving extremely low noise figure of devices. While reduction of gate length seems to be a good approach, the limitation of such an approach lies mainly in the degradation of performance caused by the short channel effect. Thus, care must be taken in obtaining the optimum physical parameters of devices for such applications.[2)]

Pt-based gate sinking technology has been widely applied in the fabrication of HEMTs since it provides a promising solution that enables vertical scaling of gate-to-channel distance without increasing access resistance. On the other hand, the short-channel effect can also be minimized.[6,7)] Another advantage of using a Pt-based structure is the relatively larger Schottky barrier height, which in turn suppresses gate leakage current.[8)] In this study, we developed 80 nm gate InAs/$In_{0.7}Ga_{0.3}As$ composite channel HEMTs using the Pt-buried gate technique with excellent DC and RF performances for ultralow-power low-noise applications.

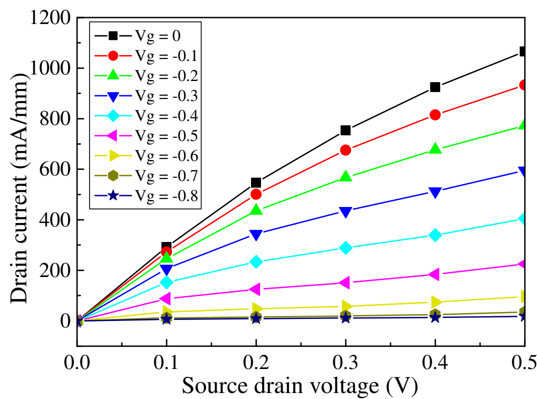
In the HEMT structure, $In_xAl_{1-x}As$ was used as the buffer layer, which was grown by the molecular beam epitaxy (MBE) method on a 2-in. InP substrate. The epitaxial structure of the device is shown in Fig. 1. The following process flow describes the sequence of device fabrication. The active area of the device was isolated by wet chemical mesa etching. After that, the 3 µm source–drain (S–D) spacing ohmic contacts were formed by evaporating Au/Ge/Ni/Au on a heavily doped n-InGaAs cap layer and then alloyed at 250 °C using rapid thermal annealing (RTA) system. The contact resistance and sheet resistance measured using the transmission line model (TLM) were 0.021 Ω·mm and 37.4 Ω/□, respectively. To process the T-shaped gate, the 50 kV JEOL electron beam lithography system (JBX 6000 FS) of 100 pA beam current was used with a conventional trilayer e-beam resist consisting of ZEP-520/PMGI/ZEP-520. After gate recess, the Pt (12 nm)/Ti (60 nm)/Pt (80 nm)/Au (180 nm) were deposited as Schottky gate metal and lifted off using a ZDMAC remover (ZEON) to form a 80 nm T-shaped gate. Devices were passivated with 1000 Å silicon nitride film by plasma-enhanced chemical vapor deposition (PECVD). Finally, thermal annealing at 250 °C for 3 min in forming gas ambient was performed for gate sinking to further recess the channel. The access resistance increased from 0.021 Ω·mm to 0.032 Ω·mm during gate sinking, the change was negligible and the characteristics of the device did not degrade.

The drain–source current $I_{ds}$ versus drain–source voltage $V_{ds}$ curves and the dc transconductance ($g_m$) versus gate voltage at different $V_{ds}$ values of the 80 nm gate, $2 \times 20\,\mu m^2$ width InAs/$In_{0.7}Ga_{0.3}As$ composite channel HEMT with gate sinking are shown in Figs. 2(a) and 2(b), respectively. The device exhibits a very high drain current density (1066 mA/mm), which is mainly attributed to a very low contact resistance and the superior electron mobility in the InAs channel.

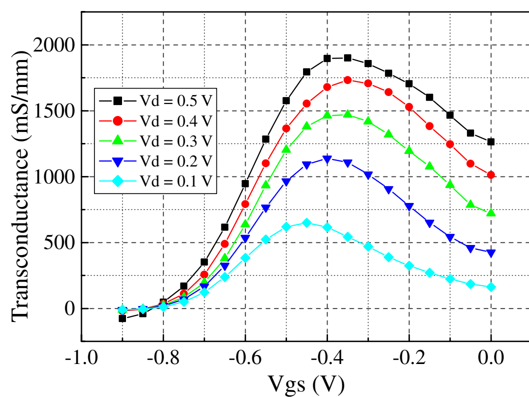
Additionally, very high $g_m$ values at low drain voltages were achieved due to the reduction of distance between the gate and the channel resulting from the gate sinking process. A peak of $g_m$ 1900 mS/mm at $V_{ds} = 0.5$ V was observed. Care must be taken in the biasing of such devices with a very small energy bandgap since the impact ionization phenomenon would occur at a high drain bias level, which in turn causes serious performance degradation. *S*-parameter measurement was performed from 5 to 80 GHz using a Cascade Microtech on-wafer probing system with a vector network analyzer, and a standard load-reflection-reflection-match

| n+ Cap | InGaAs, x = 0.53 | 35 nm, $2x10^{18}$ |
|---|---|---|
| Etch stop | InP | 4 nm |
| Barrier | InAlAs, x = 0.52 | 10 nm |
| δ-doping | Si | $5x10^{12}$ |
| Spacer | InAlAs, x = 0.52 | 4 nm |
| subchannel | InGaAs, x = 0.7 | 2 nm |
| Channel | InAs | 5 nm |
| subchannel | InGaAs, x = 0.7 | 3 nm |
| Buffer | InAlAs, x = 0.52 | 500 nm |
| **2-in. S.I. InP Substrate** | | |

Fig. 1. (Color online) Epitaxial structure of the InAs HEMT device.



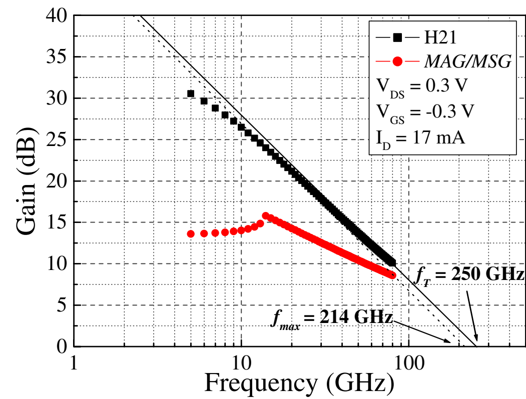

(a)



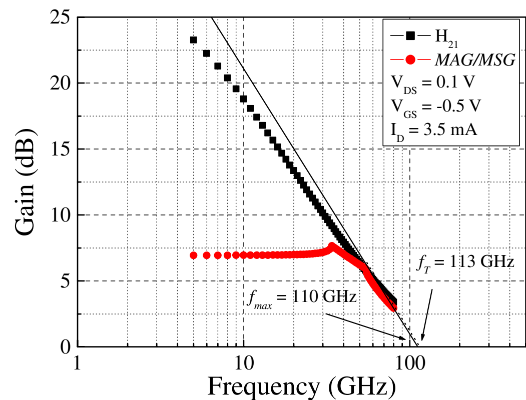

(b)

Fig. 2. (Color online) (a) The drain–source current $I_{ds}$ vs drain–source voltage $V_{ds}$ curves and (b) the dc transconductance ($g_m$) versus gate voltage curves at different $V_{ds}$, the device size is 80 nm × 40 μm with gate sinking.

(LRRM) calibration method was used to calibrate the measurement system. The reference plane of calibration was set at the tips of the probes. To accurately evaluate the performance of the intrinsic device, the parasitic effects due to the probing pads were carefully de-embedded from the measured *S*-parameters using the same method as that described in ref. 9 and the equivalent circuit model described in ref. 10. The maximum frequency of oscillation $f_{max}$ of a $2 \times 20\,\mu m^2$ device peaked at 214 GHz, at gate and drain bias of −0.3 and 0.3 V, respectively [see Fig. 3(a)]. The corresponding cutoff frequency $f_T$ at this bias point was 250 GHz.




(a)




(b)

Fig. 3. (Color online) Maximum frequency of oscillation ($f_{max}$) and corresponding cutoff frequency $f_T$ of 80 nm × 40 μm device at different drain biases.

In evaluating the devices for ultralow-DC-power-consumption applications, the devices were biased at 0.1 V and the RF performance of the devices was characterized. As shown in Fig. 3(b), a reasonable $f_T/f_{max}$ of 113/110 GHz was achieved at low bias levels. The total DC power consumptions were 5.10 and 0.35 mW when biased at peak $f_T$ and $f_{max}$, respectively. These excellent RF performances resulted from reduced gate-to-channel distance by the gate sinking process. This reduction of gate-to-channel distance through gate sinking tends to suppress the short-channel effect and enhances the overshooting in electron velocity. The noise performances at different drain voltage biases are shown in Figs. 4(a) and 4(b) with the frequency range from 1 to 17 GHz under optimum bias conditions. The measured minimum noise figures ($NF_{min}$) at 17 GHz were 0.82 and 1.05 dB for $V_{ds} = 0.3$ and 0.1 V, respectively; in addition, the corresponding associated gains ($G_a$) were 14 and 8.6 dB, respectively.

In summary, the 80 nm T-gate $InAs/In_{0.7}Ga_{0.3}As$ HEMTs fabricated by Pt gate sinking were characterized for ultra-low-power low-noise applications. With the epitaxial structure of the device optimized, the reduction of gate-to-

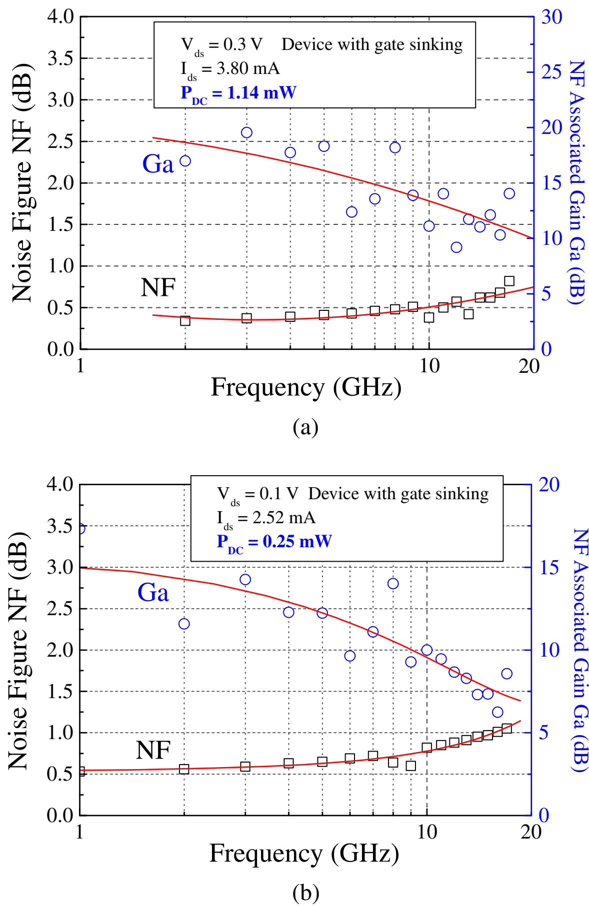



Fig. 4. (Color online) Measured noise performance of device under various bias conditions (a) with $V_{ds} = 0.3$ V, $I_{ds} = 3.80$ mA/mm and (b) with $V_{ds} = 0.1$ V, $I_{ds} = 2.52$ mA/mm.

channel distance was achieved by the gate sinking process. The device exhibited a very high drain current density of 1066 mA/mm at $V_{ds} = 0.5$ V, with a maximum $g_m$ of 1900 mS/mm. It also exhibited an $f_T$ of 113 GHz and an $f_{max}$ up to 110 GHz at $V_{ds} = 0.1$ V. Measured noise performance revealed that the devices had a very low noise figure of 1.05 dB with an 8.6 dB associated gain at 17 GHz with only 0.25 mW DC power consumption. These state-of-the-art results demonstrate the potential of InAs HEMT for ultra-low-power and low-noise applications.

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