The Channel Length Extension in Poly-Si TFTs With LDD Structure

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***Abstract*—In this letter, the resistance of the lightly doped drain (LDD) region in n-channel polycrystalline-silicon thin-film transistors (poly-Si TFTs) was analyzed. It was found that the LDD resistance was composed of an LDD-length-dependent part and a gate-bias-dominant part. The latter was located next to the gate edge and was governed by the channel extension phenomenon with an extended length of around 0.55 μm under a 10-V gate bias. The current density distribution simulated by Silvaco ATLAS supported this severe fringing field effect. The influences of the gate bias, LDD doping level, gate oxide thickness, and LDD length on the channel extension are also investigated with Silvaco ATLAS simulation. This letter is the first report of long channel extensions in the LDD region of poly-Si TFTs. The result may significantly influence the device model in the short channel regime.**

***Index Terms*—Effective channel length, lightly doped drain (LDD), parasitic resistance, polycrystalline-silicon thin-film transistor (poly-Si TFT).**

I. Introduction

POLYCRYSTALLINE-SILICON thin-film transistors (poly-Si TFTs) have high carrier mobility, which enables the design of small devices to offer large current and fast switching speed. However, the grain boundary defects in the poly-Si film make the devices exhibit large leakage current and pronounced kink effect [1], [2]. To suppress the leakage and to alleviate the kink behavior, lightly doped drain (LDD) structures with a total (source side and drain side) LDD length of around 2 μm are usually used [3]. As a result, the LDD region may significantly influence the devices when the channel length is scaled down. Although there have been many studies on poly-Si TFTs with LDD structures, these studies either proposed novel structures or analyzed device reliability [3]–[5]. In this letter, poly-Si TFTs with different LDD lengths fabricated in the same run were investigated. It was found that the parasitic resistance in the LDD region was modulated by the gate bias. By using Silvaco ATLAS simulation, the channel extension around the gate electrode was observed in devices with LDD structures. A similar phenomenon had been observed in the numerical simulation of LDD MOSFETs [6], [7]. However, little experimental evidence can be found since MOSFETs seldom have the LDD length greater than 0.3 μm. In this letter, a 0.55-μm-long channel extension under a 10-V gate bias was first reported. The influences of the gate bias, LDD doping level, gate oxide thickness, and LDD length on the channel extension are also investigated by using Silvaco ATLAS simulation.

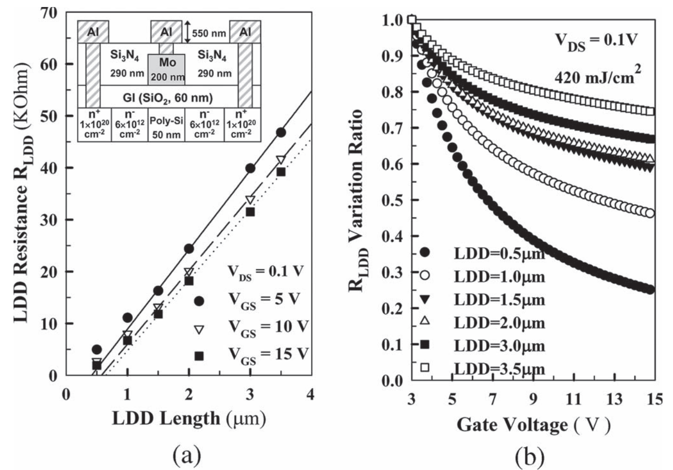

Fig. 1. (a) Relationship between LDD resistance (R_{LDD}) and LDD length. The straight lines are the linear fitting of the R_{LDD} extracted from the poly-Si TFTs with LDD lengths greater than 1.5 μm. The device structure is shown in the inset. (b) Variation ratios of R_{LDD} as a function of gate bias for devices with different LDD lengths are depicted. The variation ratio is the R_{LDD} at different gate biases ($V_{\mathrm{GS}} = 3$ to 15 V) divided by the R_{LDD} at $V_{\mathrm{GS}} = 3$ V.

II. Experimental

A 50-nm-thick a-Si layer was first deposited on a glass substrate and then crystallized by excimer laser annealing with the laser energy density of 420 mJ/cm^2. After the active island formation, a 60-nm-thick oxide layer was deposited as the gate insulator. Next, a 200-nm-thick Molybdenum was deposited and patterned as the gate electrode. The n$^-$ doping was performed self-aligned to the gate electrode by phosphorous implantation with a dosage of 6×10^{12} cm^{-2}. The n$^+$ source and drain regions were defined by an additional mask and doped by phosphorous with a dosage of 1×10^{20} cm^{-2}. Dopants were activated by thermal process. After the deposition of nitride passivation and the formation of contact holes, a 550-nm-thick aluminum layer was deposited and patterned as the metal pads. All the devices exhibit threshold voltage = 0.55 V and subthreshold swing = 0.31 V/dec. The standard devices without LDD structures have a mobility of 94 cm^2/Vs. All the

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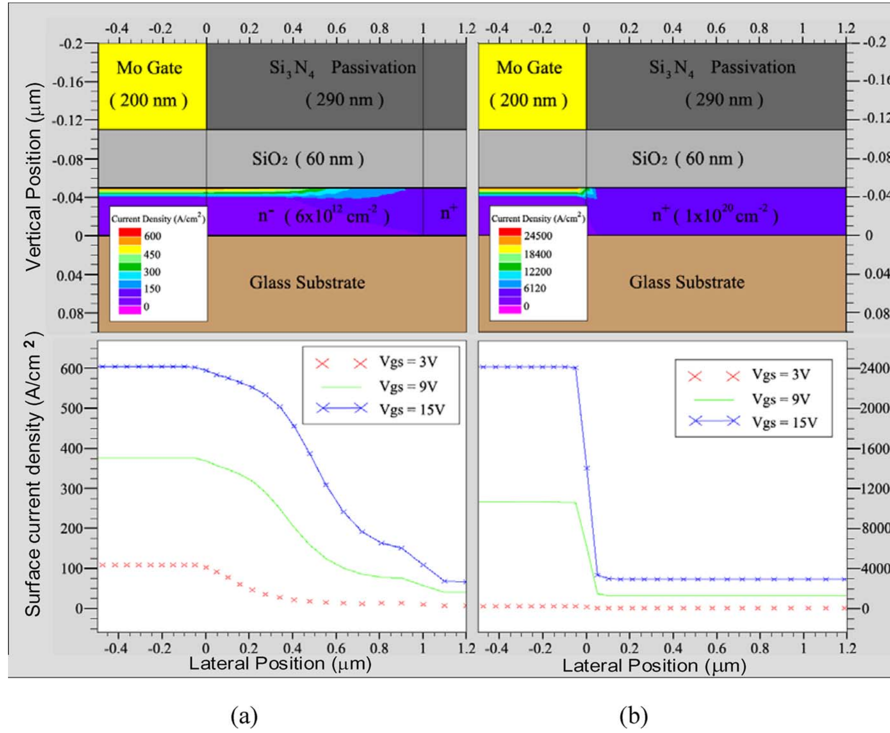

(a) (b)

Fig. 2. Current density distribution ($V_{\mathrm{GS}} = 15$ V) and surface current density distribution ($V_{\mathrm{GS}} = 3$, 9, and 15 V) for (a) devices with a 1-μm-long LDD and (b) devices without LDD structures. The channel width is 6 μm, and the channel length is 6 μm. The simulation was performed by Silvaco ATLAS with device structures shown in the inset of Fig. 1(a) and with density-of-states distribution.[1]

devices exhibit a channel length of 6 μm, a channel width of 6 μm, and an identical distance between the edge of the contact holes and the boundary of the n^+/n^- regions.

III. Results and Discussion

First, the turn-on resistance as a function of gate bias is extracted from the transfer characteristics measured when the drain bias (V_{DS}) is 0.1 V. The resistance is considered to include an intrinsic channel resistance located under the gate electrode as well as a parasitic resistance caused by the LDD resistance, the n^+ sheet resistance, and the contact resistance. When V_{DS} is small, the intrinsic channel resistance of all the devices should be the same under an identical gate bias. With the aforementioned process control and structure design, the n^+ sheet resistance and the contact resistance for all the devices should be the same. As a result, the LDD resistance (R_{LDD}) can be obtained by subtracting the turn-on resistance of devices without LDD from that of devices with LDD. As shown in Fig. 1(a), R_{LDD} is plotted as a function of LDD lengths under three gate biases ($V_{\mathrm{GS}} = 5$, 10, and 15 V). When the LDD length is greater than 1.5 μm, the relationship between R_{LDD} and the LDD length can linearly be fitted. When the LDD length is 1 or 0.5 μm, however, R_{LDD} deviates from the fitting lines. This implies that R_{LDD} has a different resistivity in short and long LDD lengths. To study the underlying mechanism, the influence of gate bias on R_{LDD} was analyzed. By taking R_{LDD} under $V_{\mathrm{GS}} = 3$ V as the reference, the R_{LDD}'s under different gate biases ($V_{\mathrm{GS}} = 3$ V to 15 V) were normalized and shown in Fig. 1(b). Obviously, R_{LDD}'s in the short LDD regions suffer from severe gate modulation effect.

By using the Silvaco ATLAS device simulator with the device structure and the doping dosage shown in the inset of Fig. 1(a), the current density distributions ($V_{\mathrm{GS}} = 15$ V) of devices with LDD (1 μm) and without LDD structures are shown at the top of Fig. 2(a) and (b). Obviously, the high current density region (channel region) of devices with LDD structures extends into the LDD region, whereas the channel region of devices without LDD structures is well confined by the gate electrode. The surface current density (J_{sf}) distributions of the two devices under various gate biases ($V_{\mathrm{GS}} = 3$, 9, and 15 V) are shown at the bottom of Fig. 2(a) and (b). Devices with LDD structures exhibit an extended channel as a strong function of gate bias.

Then, the extended channel length (ΔL) is defined as the distance between the gate edge and the position at which the surface current density (J_{sf}) is $e^{-1} \times J_{\mathrm{sf}}^{\max}$, where $J_{\mathrm{sf}}^{\max}$ is the maximum value of J_{sf} under the given gate bias. Fig. 3(a) depicts ΔL as a function of gate bias under various LDD doping dosages. ΔL increases with increasing gate bias and saturates under high gate bias. When the LDD doping dosage is below 6×10^{12} cm^{-2}, it has no influence on ΔL. When the LDD doping dosage increases from 6×10^{12} to 6×10^{13} cm^{-2}, ΔL gradually reduces to be almost zero. It is noted that the simulation uses the bandgap defect model with the parameters

[1]Bandgap defect model parameters for acceptor-like states. 1) Exponentially distributed tail states: density at the conduction band $(N_{\mathrm{TA}}) = 1.12 \times 10^{21}$ cm^{-3}/eV, and characteristic decay energy $(W_{\mathrm{TA}}) = 0.02$ eV. 2) Gaussian-distributed deep states: total density $(N_{\mathrm{GA}}) = 6 \times 10^{17}$ cm^{-3}, central energy $(E_{\mathrm{GA}}) = 0.3$ eV below the conduction band, and characteristic decay energy $(W_{\mathrm{GA}}) = 0.1$ eV. The donor-like states are not addressed because they have no influence on n-channel devices.

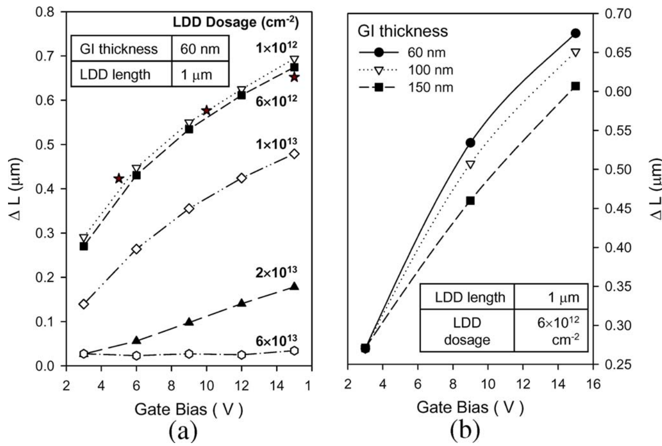

Fig. 3. ΔL extracted from the simulated surface current density distribution as a function of gate bias under (a) various LDD doping dosage and (b) various oxide thickness. ΔL is defined as the distance between the gate edge and the position at which the surface current density $(J_{\rm sf})$ is $e^{-1} \times J_{\rm sf}^{\rm max}$, where $J_{\rm sf}^{\rm max}$ is the maximum value of $J_{\rm sf}$ under the given gate bias.

given in footnote 1. The acceptor-like deep-state total density $(N_{\rm GA})$ is 6×10^{17} cm^{-3}. With a dopant activation rate of 33% given in the simulation, the dosage of 6×10^{12} cm^{-2} corresponds to the doping concentration of 4×10^{17} cm^{-3}, which is close to $N_{\rm GA}$. For a doping concentration higher than $N_{\rm GA}$, the channel extension is significantly suppressed. Three star symbols representing the x-axis intersections of the three fitting lines in Fig. 1(a) are also shown in Fig. 3(a). Their values and relationship with the gate bias are in good agreement with the simulated ΔL. The influence of the gate oxide thickness can be studied by extracting ΔL from the same simulation of $J_{\rm sf}$ distribution with different oxide thicknesses (60, 100, and 150 nm). As shown in Fig. 3(b), the thinner the oxide thickness, the more pronounced the fringing field and the channel extension.

Finally, ΔL as a function of LDD length under $V_{\rm GS} = 3$, 9, and 15 V is shown in Fig. 4. When the LDD length is small, ΔL is very close to the LDD length. When the LDD length is large, ΔL tends to saturate and has no dependence on the LDD length. A hump is found in the transition region, and the mechanism needs further investigation. However, it can be noted that when the LDD length is 0.5 μm, the whole LDD region is almost fully occupied by the extended channel.

IV. Conclusion

According to the LDD resistance analysis and the device simulation results performed by Silvaco ATLAS, a pronounced channel extension phenomenon has been proposed in poly-Si TFTs with LDD structures. The fringing field from the gate induces the channel in the LDD region, whereas no such effect can be observed for devices without LDD structures. The extended channel length is strongly influenced by the gate bias, oxide thickness, and LDD doping concentration when the doping concentration is around the total deep state density $(N_{\rm GA})$.

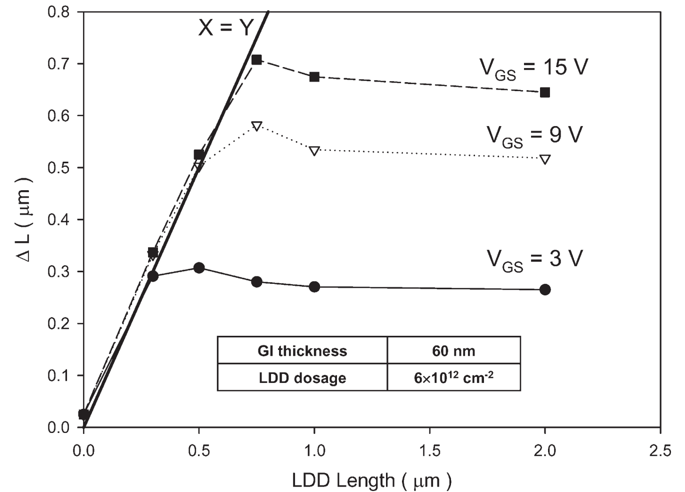

Fig. 4. ΔL extracted from the simulated surface current density distribution as a function of LDD length under $V_{\rm GS} = 3$, 9, and 15 V.

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