Short Papers

A Compact RF CMOS Modeling for Accurate High-Frequency Noise Simulation in Sub-100-nm MOSFETs

Jyh-Chyurn Guo and Yi-Min Lin

***Abstract*—A compact RF CMOS model incorporating an improved thermal noise model is developed. Short-channel effects (SCEs), substrate potential fluctuation effect, and parasitic-resistance-induced excess noises were implemented in analytical formulas to accurately simulate RF noises in sub-100-nm MOSFETs. The intrinsic noise extracted through a previously developed lossy substrate de-embedding method and calculated by the improved noise model can consistently predict gate length scaling effects. For 65- and 80-nm n-channel MOS with f_T above 160 and 100 GHz, $\mathrm{NF}_{\min}$ at 10 GHz can be suppressed to 0.5 and 0.7 dB, respectively. Drain current noise S_{id} reveals an apparently larger value for 65-nm devices than that for 80-nm devices due to SCE. On the other hand, the shorter channel helps reduce the gate current noise S_{ig} attributed to smaller gate capacitances. Gate resistance R_g-induced excess noise dominates in S_{ig} near one order higher than the intrinsic gate noise that is free from R_g for 65-nm devices. The compact RF CMOS modeling can facilitate high-frequency noise simulation accuracy in nanoscale RF CMOS circuits for low-noise design.**

***Index Terms*—Lossy substrate de-embedding, radio frequency (RF) complementary metal–oxide–semiconductor (CMOS) model, short-channel effect (SCE), thermal noise model.**

I. Introduction

The advancement of CMOS device technology to the sub-100-nm regime has driven a remarkable increase in cutoff frequency (f_T) and maximum oscillation frequency $(f_{\max})$ to well above 100 GHz and has made RF CMOS a vital technology enabling communication SoC [1]–[3]. The decrease in noise with device scaling is desirable for low-noise RF circuit design. However, an accurate noise extraction and modeling emerges as a challenging subject for miniaturized devices. For the first time, a lossy substrate de-embedding method was developed to successfully extract the intrinsic noise parameters in 80- and 65-nm devices for exploring the aggressive gate length scaling effect on RF noise [4], [5].

Regarding short-channel effect (SCE) on channel thermal noise, there has been much controversy in the last two decades [6]–[11]. It was reported that the channel thermal noise model implemented in the Berkeley Short-channel IGFET Model 3 (BSIM3, an industry standard model) generally underestimates drain current noise (S_{id}) and cannot accurately simulate the noise parameters [12]. Our study suggests that hot carrier effect plays a minor role, and the classical noise model remains valid, provided that SCEs such as mobility degradation, velocity saturation, carrier heating, drain-induced barrier lowering (DIBL), and channel length modulation (CLM) are accurately implemented in the I–V and channel thermal noise models [8]–[11].

In this paper, an improved thermal noise model is presented. SCE, substrate potential fluctuation effect, and parasitic-resistance-induced excess noises are important features implemented in the form of analytical formulas and seamlessly integrated as a complete RF noise model. The power spectral density of current noises at drain and gate (S_{id} and S_{ig}) is calculated, and four noise parameters ($\mathrm{NF}_{\min}$, R_n, Y_{opt}) can be derived from the noise power corresponding to the simulated current noises and source impedance [13]. This enhanced noise model in the explicit form can easily be deployed in high-frequency circuit simulators such as Agilent ADS and can realize a compact RF CMOS model for dc, ac, and RF noise simulation over tens of gigahertz. The comparison between the improved noise model, BSIM3 noise model, and measurement reveals that BSIM3 underestimates $\mathrm{NF}_{\min}$ and S_{id} in magnitude and frequency dependence for miniaturized MOSFETs down to 65 nm. The improved noise model can fix the problem and demonstrate promising accuracy in sub-100-nm devices over wide frequencies and bias conditions.

II. RF Device Test Structure and Lossy Substrate Model

MOSFETs measuring 65 and 80 nm were fabricated to investigate gate length (L_{gate}) scaling effect on speed and noise. Multifinger structures with the finger width fixed at 4 μm and various finger numbers $N_F = 6, 18, 36,$ and 72 were employed to reduce R_g and the induced excess noises. The noise parameters were measured by an ATN-NP5B system to 18 GHz for fixed V_{gs} at maximum g_m or minimum $\mathrm{NF}_{\min}$. Based on the noise correlation matrix method [14] and equivalent circuit analysis for a two-port noisy network, the measured $\mathrm{NF}_{\min}$, R_n, and Y_{opt} can be used to derive S_{id} and S_{ig}. The details of device characterization and modeling flow involving measurement, parameter extraction, optimization, and model calibration can be found in our original work [4], [15].

Fig. 1 illustrates an RF device test structure composed of a device under test (DUT), ground–signal–ground (GSG) pad, and transmission line (TML) in 3-D topology, and the equivalent circuits representing lossy substrate networks underneath the pad and TML. Open and through-pad S-parameters were measured for lossy substrate model parameter extraction. The physical properties of substrate RLC parameters have been defined in [15]. Then, the lossy substrate model was integrated with intrinsic MOSFET as a full equivalent circuit in Fig. 2 for extrinsic noise simulation and intrinsic noise extraction. Note that TML in a standard open pad is composed of M8 through M7–M4 and terminated at M3. The parasitic capacitances contributed from M3–M1 cannot be removed by the conventional open de-embedding. This kind of extrinsic gate capacitance is nonscalable with device dimension and may impose a significant influence on miniaturized devices in high-frequency performance.

III. Intrinsic MOSFET Modeling

A. BSIM3 I–V Model Calibration

An extensive calibration was done on the BSIM3 I–V model for sub-100-nm MOSFETs. The important corrections involve SCE in threshold voltage (V_T), velocity saturation, CLM, and DIBL effects

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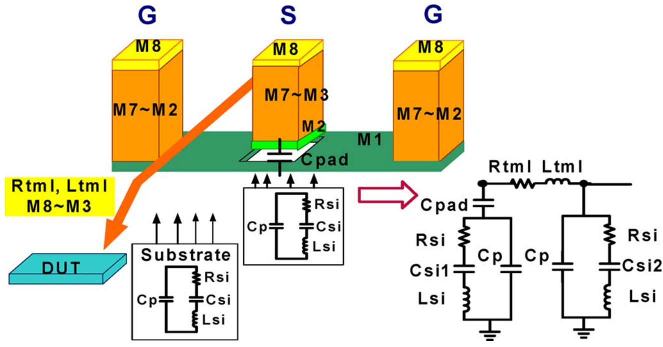

Fig. 1. RF device test structure composed of DUT, GSG pad, and TML in 3-D topology and the equivalent circuits representing lossy substrate networks underneath the pad and TML.

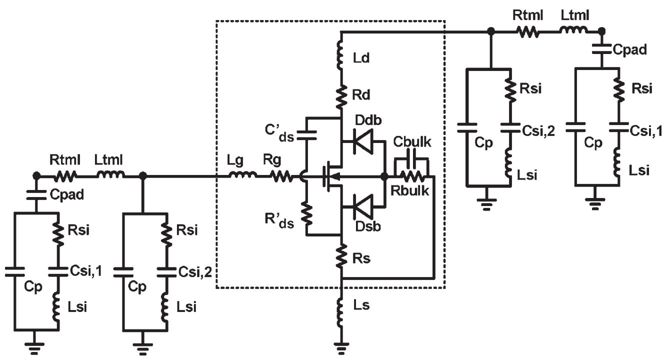

Fig. 2. Full circuit schematics with substrate *RLC* network integrated with intrinsic MOSFET.

in saturation I–V, as well as DIBL and drain-to-source coupling capacitance effects in subthreshold I–V [16]. As a result, the I–V model with SCE parameters properly specified can accurately simulate I_d–$V_{\rm gs}$, I_d–$V_{\rm ds}$, and transconductance (g_m), as well as output conductance ($g_{\rm ds}$) for 80- and 65-nm n-channel MOS (nMOS) with various N_F's [5]. The refined I–V model can predict g_m enhancement by about 20%–30% for 65-nm devices compared to that for the 80-nm devices, which is attributed to the $L_{\rm gate}$ reduction by 20%. The accurate simulation of g_m is essential to predict ${\rm Re}(Y_{21})$ and f_T.

B. BSIM3 C–V Model Calibration

C–V model calibration was done by incorporating extrinsic gate capacitances and appropriate threshold voltage tuning $V_{\rm off,CV}$. The impact from the nonscalable extrinsic capacitances increases in miniaturized devices with shorter $L_{\rm gate}$ and smaller N_F. For the smallest device with $L_{\rm gate} = 65$ nm and $N_F = 6$, the extrinsic capacitances contribute about 30% of the total capacitance. The calibrated C–V model can accurately simulate C–V characteristics for various N_F's, as well as $L_{\rm gate}$, and over a wide range of $V_{\rm gs}$ from weak-to-strong inversion [5]. For $L_{\rm gate}$ scaling from 80 to 65 nm, $C_{\rm gg}$ is reduced by about 16%–20%, corresponding to $N_F = 6{-}72$, whereas $C_{\rm gd}$ is reduced by only 7%–14%. The weaker dependence on $L_{\rm gate}$ revealed by $C_{\rm gd}$ suggests drain depletion effect under saturation [5].

I–V and C–V models with the proven accuracy for sub-100-nm devices can validate high-frequency simulation for the prediction of key performance parameters such as f_T and $f_{\rm max}$, and ${\rm NF}_{\rm min}$. Fig. 3 presents f_T over a wide range of I_d, in which f_T is extracted corresponding to $|H_{21}| = 1$. A good match between simulation and measurement is demonstrated for all N_F's. The maximum f_T realized

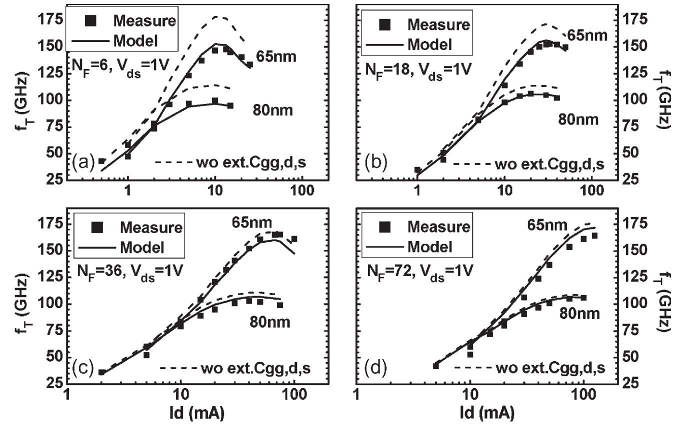

Fig. 3. Comparison of measured and simulated f_T versus $I_d(V_{\rm ds} = 1$ V) for 80- and 65-nm RF n-channel MOSFETs (nMOSFETs). (a) $N_F = 6$. (b) $N_F = 18$. (c) $N_F = 36$. (d) $N_F = 72$. (Solid line) Calibrated model. (Dashed line) CV model without $C_{\rm gg,ext}$, $C_{\rm gd,ext}$, and $C_{\rm gs,ext}$.

by 65-nm nMOS is about 160 GHz. It exhibits 50%–60% improvement over its 80-nm counterpart with maximum f_T at 100–110 GHz. The f_T enhancement factor matches well with the prediction calculated by an analytical expression of $f_T = g_m/2\pi\sqrt{(C_{\rm gg}^2 - C_{\rm gd}^2)}$, in which the increase in g_m by 20%–30% and reduction in $C_{\rm gg}$ by 16%–20% can improve f_T by nearly 60% due to $L_{\rm gate}$ scaling from 80 to 65 nm. Note that neglecting extrinsic gate capacitances will overestimate f_T, as denoted by dashed lines in Fig. 3. The overestimation becomes significant in miniaturized devices with smaller N_F and shorter $L_{\rm gate}$.

IV. Improved Thermal Noise Model for Sub-100-nm RF CMOS

The advantage provided by $L_{\rm gate}$ scaling on RF performance, such as $f_T(g_m, C_{\rm gg})$, calls for an interest to investigate its effect on high-frequency noises. We reported interesting but abnormal features in ${\rm NF}_{\rm min}$ measured from sub-100-nm devices, such as weak dependence on $L_{\rm gate}$, strong dependence on N_F, and nonlinear frequency dependence [5]. All three observations cannot be explained by thermal noise theory and intrinsic device performance. We proposed that substantial excess noises were generated from the lossy substrate and led to a dramatic impact on miniaturized devices in RF noises. In this paper, an improved thermal noise model is proposed to work with the proven lossy substrate model for accurate RF noise simulation in sub-100-nm devices.

In the following, an improved thermal noise model is implemented to replace the default noise model in BSIM3. The major features incorporated in this improved noise model are SCE (velocity saturation, CLM, and carrier heating) and substrate-resistance-induced potential fluctuation effect in drain current noise, and gate-resistance-induced excess noises in both drain and gate current noises.

The model equations are formulated in (1)–(7) for drain current noise $S_{\rm id}$ and (8)–(11) for gate current noise $S_{\rm ig}$. To calculate drain current noise $S_{\rm id}$, SCEs such as the velocity saturation that originated from lateral field-induced mobility degradation, carrier heating, CLM effect [10], [11], and nonuniform channel effect on V_T, as well as body coefficient (α), have been implemented in (2)–(4). The frequency dependence generally revealed in the measured $S_{\rm id}$ and R_n with higher value at lower frequency is modeled by an excess noise $S_{\rm id,sub}$ in (6), which is caused by the substrate potential variation associated with substrate resistance and capacitances ($R_{\rm bulk}$, $C_{\rm bulk}$) [17]. As for gate current noise $S_{\rm ig}$, the intrinsic gate noise is calculated by

(9), in which noise factor β is about 1.3–1.6 for 80-nm devices and 1.5–2.0 for 65-nm devices. The excess noise that originated from gate resistance R_g has been taken into account and implemented for both S_{id} and S_{ig} through (7) and (10), respectively [9]. The simulation results based on the proposed model indicate that the intrinsic gate noise is much smaller than gate-resistance-induced excess noise by nearly one order of magnitude in sub-100-nm devices.

Drain current noise spectral density S_{id} is calculated as [9]–[11], [14]

$$S_{\iota d} = \frac{\overline{|\iota_{\mathrm{nd}}|^2}}{\Delta f} = S_{\iota d0} + \Delta S_{\iota d} \tag{1}$$

where

$$S_{\iota d0} = 4k_B T \cdot g_{\mathrm{do}} \cdot \frac{1 - u + u^2/3}{1 - u/2} \tag{2}$$

$$g_{\mathrm{do}} = \frac{\mu_{\mathrm{eff}} W C_{\mathrm{ox}} V_{\mathrm{GT}}}{L_{\mathrm{eff}}} \tag{3}$$

$$u = \alpha \frac{V_{\mathrm{ds}}}{V_{\mathrm{GT}}}, V_{\mathrm{GT}} = V_{\mathrm{gs}} - V_T \tag{4}$$

$$\Delta S_{\iota d} = S_{\iota d,\mathrm{sub}} + S_{\iota d, R_g} \tag{5}$$

$$S_{\iota d,\mathrm{sub}} = \frac{4k_B T \cdot R_{\mathrm{bulk}} g_{\mathrm{mb}}}{1 + (\omega R_{\mathrm{bulk}} C_{\mathrm{bulk}})^2} \tag{6}$$

$$S_{\iota d, R_g} = 4k_B T \cdot R_g |Y_{21}|^2 \tag{7}$$

where

- α body effect coefficient;
- ι_{nd} noise current at drain;
- $S_{\iota d}$ power spectral density of drain current noise;
- $S_{\iota d,\mathrm{sub}}$ excess drain current noise caused by substrate-resistance-induced potential fluctuation;
- $S_{\iota d, R_g}$ excess drain current noise caused by the gate resistance.

Gate current noise spectral density S_{ig} is calculated by [9]

$$S_{\iota g} = \frac{\overline{|\iota_{\mathrm{ng}}|^2}}{\Delta f} = S_{\iota g0} + \Delta S_{\iota g} \tag{8}$$

where

$$S_{\iota g0} = \frac{4k_B T \cdot \beta |\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{12})|^2}{5 g_{\mathrm{do}}} \tag{9}$$

$$\Delta S_{\iota g} = S_{\iota g, R_g} = 4k_B T \cdot R_g |\mathrm{Im}(Y_{11})|^2 \tag{10}$$

and $S_{\iota g, R_g}$ is the excess gate current noise caused by the gate resistance.

For short-channel devices with sub-100-nm gate lengths

$$S_{\iota g0} \ll S_{\iota g, R_g} \cong S_{\iota g} \tag{11}$$

where

- ι_{ng} noise current at the gate;
- $S_{\iota g}$ power spectral density of the gate current noise.

V. Noise Simulation Result and Discussion

A. Extrinsic Noise Simulation—Current Noises and Noise Parameters

The improved thermal noise model was implemented in intrinsic MOSFETs and integrated with the proven lossy substrate model for extrinsic noise simulation. Fig. 4 compare the measured and simulated S'_{id} and S'_{ig} over frequencies of up to 18 GHz. As shown in Fig. 4(a) and (b), the improved noise model can consistently predict S'_{id} for 65- and 80-nm nMOS, in which the SCE was presented with higher S'_{id} in 65-nm devices. The frequency dependence of S'_{id} with an increase at sufficiently low frequencies can be simulated by the introduced excess noise $S_{\mathrm{id,sub}}$ in (6) due to substrate potential variation. Note that conventional models commonly assume that S_{id} is a pure white noise independent of frequency. However, the measured S'_{id} generally reveals apparent frequency dependence. For comparison, the BSIM3 noise model appears to underestimate S'_{id} for 65-nm devices and fails to predict the frequency dependence. This result suggests that the SCE was not appropriately implemented in the BSIM3 noise model with a simple equation given by $S_{\mathrm{id}} = 4k_B T \mu_{\mathrm{eff}} Q_{\mathrm{inv}}/L^2$ [10]–[12]. As for extrinsic S'_{ig} in Fig. 4(c) and (d), the frequency dependence deviates much from the theory of being proportional to ω^2, and the N_F dependence is abnormally weak, both due to the lossy-substrate-introduced excess noises.

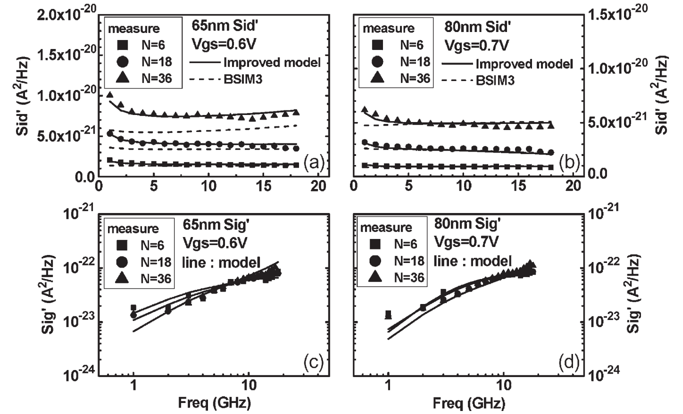

Fig. 4. Measured and simulated S'_{id} and S'_{ig} for 65- and 80-nm nMOSFETs of various N_F's. $V_{\mathrm{ds}} = 1.0$ V. The gate bias is fixed at maximum g_m, and the frequency is swept from 1 to 18 GHz. (a) 65-nm S_{id}. (b) 80-nm S'_{id}. (c) 65-nm S'_{ig}. (d) 80-nm S'_{ig}. (Solid line) Improved noise model. (Dashed line) BSIM3 noise model.

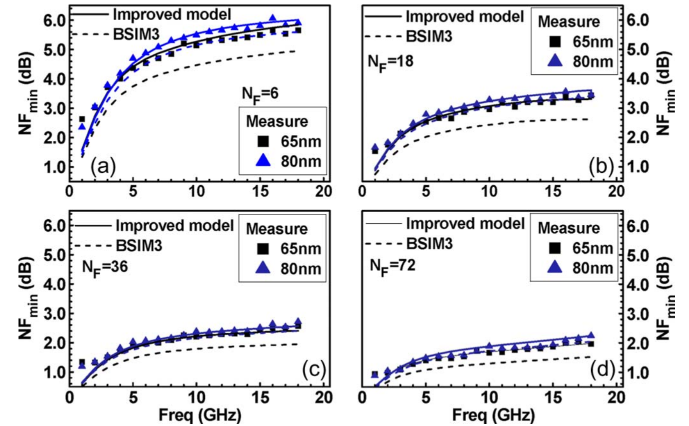

Fig. 5. Measured and simulated $\mathrm{NF_{min}}$ versus frequency (1–18 GHz) for 65- and 80-nm nMOSFETs. (a) $N_F = 6$. (b) $N_F = 18$. (c) $N_F = 36$. (d) $N_F = 72$. The bias conditions are at $V_{\mathrm{ds}} = 1.0$ V and V_{gs} at maximum g_m. (Solid line) Improved noise model. (Dashed line) BSIM3 noise model. BSIM3 simulation reveals an underestimation in $\mathrm{NF_{min}}$, with an apparently worse deviation for 65-nm devices.

Fig. 5 presents the simulated $\mathrm{NF_{min}}$ over frequencies to 18 GHz and the comparison with the measurement. The improved noise model can predict the extrinsic $\mathrm{NF_{min}}$ for 65- and 80-nm devices with various N_F's, whereas the BSIM3 noise model underestimated $\mathrm{NF_{min}}$ in

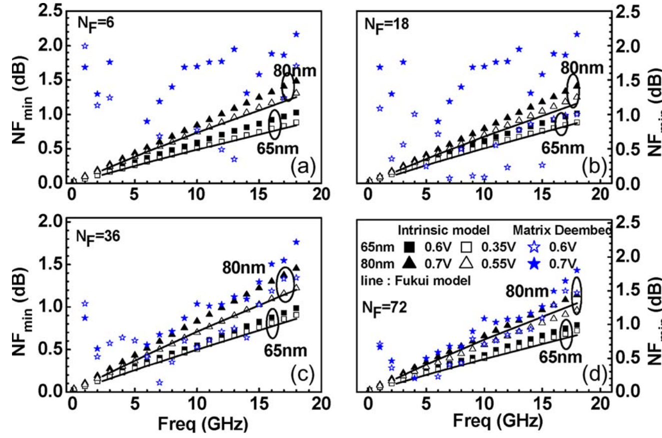

Fig. 6. Extracted intrinsic $\mathrm{NF}_{\min}$ for 80- and 65-nm nMOSFETs under varying frequencies (1–18 GHz). $V_{\mathrm{ds}} = 1.0$ V, and V_{gs} is at maximum g_m (0.7/0.6 V for 80/65-nm devices) and minimum $\mathrm{NF}_{\min}$ (0.55/0.35 V for 80/65-nm devices). (a) $N_F = 6$. (b) $N_F = 18$. (c) $N_F = 36$. (d) $N_F = 72$. (Line) Fukui's formulas. (Star) Noise de-embedding by the noise correlation matrix method.

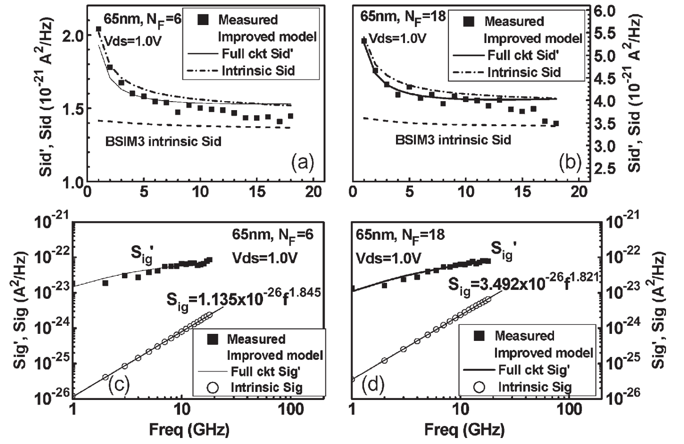

Fig. 7. Comparison between the extrinsic (S'_{id} and S'_{ig}) and intrinsic (S_{id} and S_{ig}) current noises, which were simulated by full circuit and intrinsic models for 65-nm nMOSFETs. (a) S'_{id} and S_{id} for $N_F = 6$. (b) S'_{id} and S_{id} for $N_F = 18$. (c) S'_{ig} and S_{ig} for $N_F = 6$. (d) S'_{ig} and S_{ig} for $N_F = 18$. A good match between the full circuit simulation (lines) and measurement (symbols) was demonstrated.

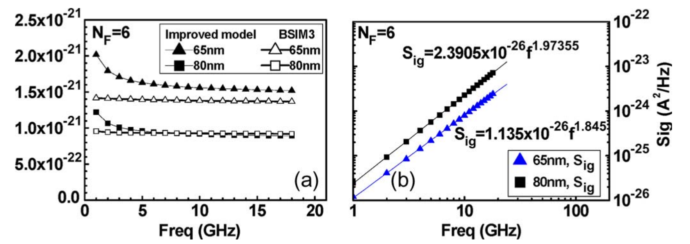

Fig. 8. Comparison of intrinsic S_{id} and S_{ig} between 65- and 80-nm nMOSFETs to show SCE. $N_F = 6$. (a) S_{id}. (b) S_{ig}. $V_{\mathrm{ds}} = 1.0$ V. V_{gs} is at maximum g_m and frequency in the range of 1–18 GHz.

65-nm devices. The excellent match with measured noises in dependence of L_{gate}, N_F, and frequency proves the solution realized by the improved thermal noise mode working with the lossy substrate model for extrinsic noise simulation.

B. Intrinsic Noise Parameters—Frequency Dependence and Comparison With Noise Correlation Matrix De-Embedding

The lossy substrate model and intrinsic MOSFET model proven over varying frequencies and device dimensions enable an accurate lossy substrate de-embedding for intrinsic noise extraction. The lossy substrate de-embedding can precisely be done by removing all elements of the pad and substrate RLC networks from the full equivalent circuit in [15]. The parasitic resistances (R_g, R_s, R_d, and R_{bulk}) that remained with the intrinsic MOSFET act as important elements that are responsible for the excess noises even after de-embedding. Fig. 6 shows the intrinsic $\mathrm{NF}_{\min}$ extracted for 65- and 80-nm nMOS under V_{gs} at maximum g_m and minimum $\mathrm{NF}_{\min}$, respectively. The accuracy of the extracted intrinsic noise is justified by a good match with the Fukui formula $F_{\min} = 1 + k^* f/f_T[g_m(R_g + R_s)]^{1/2}$ [18] for those under V_{gs} at minimum $\mathrm{NF}_{\min}$. Apparently, the 65-nm devices demonstrate lower $\mathrm{NF}_{\min}$ than their 80-nm counterparts with the same N_F. The suppression of $\mathrm{NF}_{\min}$ by about 0.2 dB at 10 GHz suggests the contribution from f_T enhancement by nearly 60% due to L_{gate} scaling and the advantage offered by continuous scaling to the deep sub-100-nm regime. Note that the noise de-embedding by using the noise correlation matrix method [14] was simultaneously performed for a comparison. The results shown by the star sign in Fig. 6 reveal a dramatic fluctuation over frequency. It is a common problem presented in many publications, and a smoothing was reported to get a reasonable frequency dependence [19].

C. Extrinsic and Intrinsic Current Noise—Lossy Substrate De-Embedding and Noise Model Comparison

Fig. 7 presents intrinsic current noises S_{id} and S_{ig} extracted through lossy substrate de-embedding and the comparison with extrinsic ones such as S'_{id} and S'_{ig}. For S_{id} compared to S'_{id} shown in Fig. 7(a) and (b), the increase in lower frequency while suppression to near constant at higher frequency can be explained by the de-embedding effect on $|Y_{21}|^2$, which is a major parameter determining S_{id}. At lower frequency, $|Y_{21}|^2$ is dominated by $|\mathrm{Re}(Y_{21})|^2$, which may increase after de-embedding. As for higher frequency, $|\mathrm{Im}(Y_{21})|^2$ may take over the influence on S_{id} for larger N_F before de-embedding, whereas the substantial decrease in $|\mathrm{Im}(Y_{21})|^2$ after de-embedding will suppress S_{id} to near constant. Note that the intrinsic S_{id} simulated by the BSIM3 noise model was put together for comparison. The results indicate much lower noises and diminishing frequency dependence. It supports previous comments that the BSIM3 noise model is not valid for noise simulation in miniaturized devices with significant SCE. As for S_{ig} and S'_{ig} shown in Fig. 7(c) and (d), the lossy substrate de-embedding can reduce the gate current noise by orders of magnitude and recover the frequency dependence to follow the ideal theory of being proportional to ω^2. The results prove an effective de-embedding of parasitic capacitances at the input represented by $\mathrm{Im}(Y_{11})$ and $\mathrm{Im}(Y_{12})$ in (9).

D. Intrinsic Current Noises S_{id} and S_{ig}—SCE

Fig. 8(a) and (b) presents intrinsic S_{id} for 65- and 80-nm devices to investigate SCE. The obviously larger S_{id} for 65-nm devices, compared to that for 80-nm devices, accounts for the major effect from larger g_{do} due to shorter effective length L_{eff}. The excess noise that originated from R_g given by $S_{\mathrm{id,Rg}}$ in (7) also increases with L_{eff} scaling due to the larger $|Y_{21}|^2$. The frequency-dependent excess noise $S_{\mathrm{id,sub}}$ given by (6) can consistently simulate the interesting behavior, which is different from the general assumption of white noise. Again, the BSIM3 noise model underestimates S_{id} and its frequency dependence. Regarding the L_{gate} scaling effect on the intrinsic S_{ig}

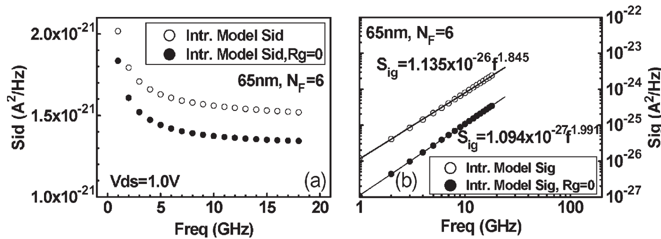

Fig. 9. Simulated intrinsic S_{id} and S_{ig} for 65-nm nMOSFETs with and without R_g. $N_F = 6$. (a) S_{id}. (b) S_{ig}. $V_{\mathrm{ds}} = 1.0$ V. V_{gs} is at maximum g_m and frequency in the range of 1–18 GHz.

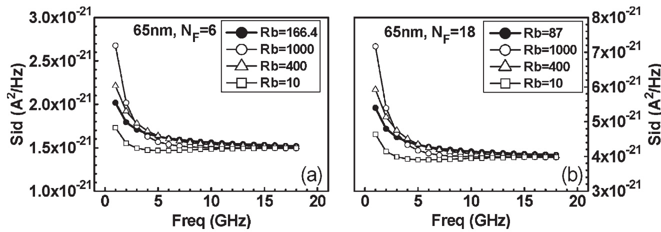

Fig. 10. Simulated intrinsic S_{id} for 65-nm nMOSFETs with various bulk resistance R_{bulk}, with optimized values of 1000, 400, and 10 Ω. (a) $N_F = 6$. (b) $N_F = 18$. $V_{\mathrm{ds}} = 1.0$ V. V_{gs} is fixed at maximum g_m and frequency in the range of 1–18 GHz.

shown in Fig. 8(c) and (d), the obviously smaller S_{ig} for 65-nm devices than that for 80-nm devices accounts for the smaller gate capacitances C_{gg} and C_{gs} represented by $\mathrm{Im}(Y_{11})$ and $\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{12})$, respectively, for intrinsic devices after de-embedding. The decrease in S_{ig} while S_{id} is increasing with L_{gate} scaling results in the absolute dominance of S_{id} over S_{ig} in nanoscale devices. For 80-nm devices, S_{id} remains higher than S_{ig} by more than one order. As for 65-nm devices, the ratio keeps going up to more than two orders.

E. Excess Noises in S_{id} and $S_{\mathrm{ig}} - R_g$ and R_{bulk} Effect

Gate-resistance-induced excess noise was simulated by (7) and (10) for S_{id} and S_{ig}, respectively. Fig. 9 presents the simulation for 65-nm devices with and without R_g for comparison. In practical devices, R_g cannot be eliminated to zero. Assuming an ideal condition in simulation without R_g, the intrinsic S_{id} can be reduced by about 13%–17% over 18 GHz. The suppression of S_{ig} due to the removal of R_g is even larger to near one order. Note that variation in R_g causes a near-parallel shift in S_{id} and S_{ig} over frequency, i.e., no influence on frequency dependence. Regarding one more excess noise in S_{id} that originated from the substrate potential fluctuation calculated by (6), noise simulation was done to investigate the R_{bulk} effect. Fig. 10 indicates an interesting result in that the larger R_{bulk} leads to a significant increase in S_{id} in lower frequency but has nearly no influence in higher frequency (> 10 GHz). Sufficiently low R_{bulk} can suppress the frequency dependence and may approach a white noise, which is independent of frequency.

VI. Conclusion

A compact RF CMOS model has been developed for accurate RF noise simulation in sub-100-nm MOSFETs. An improved thermal noise model was implemented in explicit form, incorporating SCE, substrate potential variation, and resistance-induced excess noises. The accuracy has been proven by a good match with measurement in $f_T(g_m, C_{\mathrm{gg}}, C_{\mathrm{gd}})$, noise parameters, and current noises over frequencies. The improved thermal noise model can solve problems in BSIM3 and accurately simulate the L_{gate} scaling effect on RF noises. The shorter L_{gate} can help reduce $\mathrm{NF}_{\min}$, R_n, and S_{ig} due to larger g_m, smaller C_{gg}, and higher f_T. The major penalty from the L_{gate} scaling is the increase in S_{id}. R_g-induced excess noises contribute almost all of S_{ig} and about 15% of S_{id} in 65-nm devices. On the other hand, R_{bulk}-induced excess noises have a major impact on S_{id} at lower frequency but have no influence on S_{ig}. The developed compact RF CMOS model is useful in facilitating accurate noise simulation in nanoscale RF CMOS circuits for low-noise design.

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