Smooth Pole Tracking Technique by Power MOSFET Array in Low-Dropout Regulators

Yung-Hsin Lin, Kuo-Lin Zheng, and Ke-Horng Chen

***Abstract*—This paper proposes an advanced Q-reduction technique of pole-splitting compensations for low dropout (LDO) regulator. The output pole is load dependent and may cause the scenario of complex poles when load current changes. LDO regulators may oscillate because high-Q incurs the less gain and phase margins. The reasons of causing complex poles depend on the design methodology. For the design of capacitor-free LDO regulator, high-Q issue happens when load current changes from heavy to light. Recent literature provides a method to alleviate the high-Q problem. However, large dropout voltage in case of suddenly large loads forces designers to include a small load capacitor as an indispensable component for supplying system-on-chip (SoC) systems. Different to the case of capacitor-free LDO regulators, high-Q issue happens when load current changes from light to heavy. According to our proposed power MOSFET array, the high-Q problem can be alleviated and prevent LDO regulators from oscillating when load changes. Experimental results promise the stability and show the improvement of load and line regulations.**

***Index Terms*—Capacitor-free, complex pole, low-dropout regulator (LDO), power MOSFET array, Q-reduction.**

I. Introduction

THE low-dropout regulator (LDO) architecture compensated by the pole-splitting technique is shown in Fig. 1. For pole-splitting compensation techniques, we need to implement multistage operational amplifier to have an equivalent large Miller capacitance at the first stage output for generating a dominant pole. The outputs of the cascading stages contribute the non-dominant poles in sequence. In other words, the characteristics of LDO regulators with pole-splitting compensation are larger low-frequency gain and higher crossover frequency. Recently, the design of a capacitor-free LDO regulator [2], [3] is increasingly requisite for every battery-operated device because it has the advantages of lower usage of printed circuit board (PCB) space and fewer off-chip components. Owing to the non-dominant complex poles locate near unit gain frequency (UGF), a large Q value causes a sharper phase change at the angular corner frequency [1]. The LDO will become unstable because frequency peaking near UGF makes less gain and phase margin [4]. An advanced Q-reduction technique [1] is proposed to solve the oscillation problem when load current changes from heavy to light.

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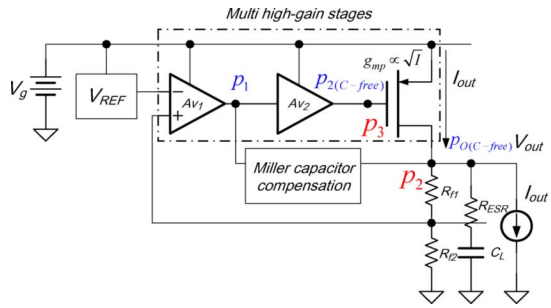

Fig. 1. Location of poles in a capacitor-free LDO regulator with pole-splitting compensation and in a LDO regulator with a small output capacitor. The first non-dominant pole (p_2) is changed from the output of the output of second stage ($p_{2(\mathrm{C\text{-}free})}$) to the output of the last stage. The second non-dominant pole (p_3) is located at the gate of power MOSFET.

Furthermore, the critical problem of a capacitor-free LDO regulator is low driving capability when load current changes within a short time. For sudden load variations within a short time, the output voltage is drastically pulled down or up to an unacceptable voltage for system-on-chip (SoC) systems. Direct current feedback [5] is proposed to dynamically basing the LDO regulator for alleviating the slewing problem of operational amplifier. As we know, the current sensor [5] suffers from low accuracy when load current is too low to make the current sensor work correctly. Thus, for a stable supplying source for SoC systems, an output capacitor is sometimes needed at the output node of a LDO regulator for prevent the output voltage from pulling too high or low [6].

Owing to the small output capacitor, the output pole substitutes the pole at the second stage output as the first non-dominant pole. Thus, the frequency response of this architecture is different from that of capacitor-free LDO regulators. It means that the advanced Q-reduction proposed by literature [1] is not useful for this design. On the contrary, we have to find out another Q-reduction to improve the stability of LDO regulators in case of load variations.

Most importantly, the Miller-compensated LDO regulator with an output capacitor not only have the capability to react to sudden load variations but also not is limited to a minimum load current because of equivalent series resistance (ESR) zero provided by output capacitor. As just alluded, the two separate non-dominant poles may become complex poles with a high Q value or small damping factor when the output current changes from low to high. It is similar to the case when the output current changes from high to low in the capacitor-free LDO regulator. In other words, large variation of the load current may cause the output voltage to have a drastic voltage drop owing to the lack of a large output capacitor. It causes malfunction in SoC

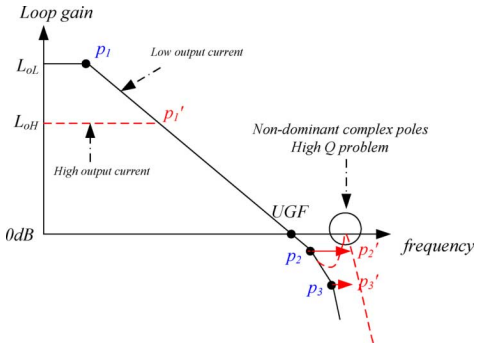

Fig. 2. High-Q problem happened in the LDO regulator with small output capacitor.

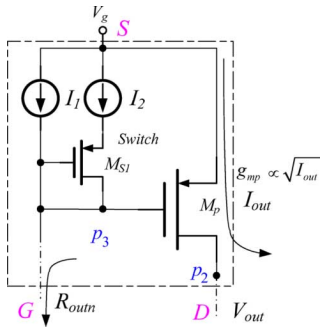

Fig. 3. Simple pole-tracking technique proposed by [6].

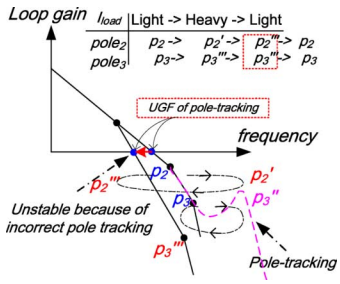

Fig. 4. Loci of the first and second non-dominant poles reveal the unstable condition caused by incorrect pole tracking technique.

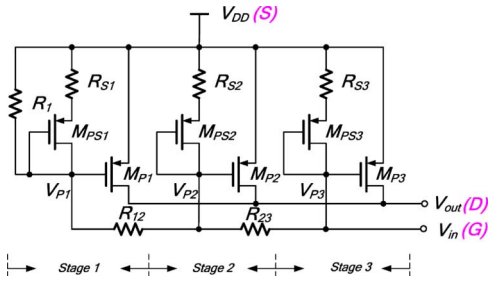

Fig. 5. Equivalent power MOSFET array with smooth pole tracking technique.

systems. Thus, an output capacitor is requested to ensure minimized transient voltage variation for supplying SoC systems. To make a summary, a suitable LDO regulator for supplying SoC systems has to use a high-gain multistage operational amplifier for improving load and line regulations and an output capacitor for alleviating the drastic transient voltage variation. Certainly, high-Q problem is different to that of capacitor-free LDO regulator design due to the first non-dominant contributed by the low-frequency pole at the output node in Fig. 1.

The first non-dominant pole, which is located at output of the last stage, moves to high frequency at heavy load. Thus, the occurrence of complex poles, which is shown in Fig. 2, may happen when load current changes from light to heavy. Thus, the only way for us to avoid high Q problem is to make the second non-dominant pole adapt to the first non-dominant pole moving to higher frequency [6]. The smooth tracking of the second non-dominant pole is important because it may cause the phase margin less than that of LDO regulator without pole tracking technique. In other words, a worse pole tracking technique may cause the LDO regulator unstable when load changes. Therefore, we propose a smooth pole tracking technique [7], [8] to reduce the high Q problems in an LDO regulator with a small output capacitor.

In this paper, an LDO with smooth pole tracking targeted for SoC will be proposed. The key feature is to alleviate the transient dropout voltage and the possibility of oscillation with a smooth pole tracking technique. Advanced circuit implementation of the pole tracking circuit will then be introduced and discussed. Finally, experimental results will be given to verify the theory.

II. Circuit Implementation of Power MOSFET Array

In order to maintain a stable LDO regulator over a wide load current range, a pole tracking technique is utilized to force the first non-dominant pole (p_2) to track the load variations. Besides, the pole tracking technique also moves the second non-dominant pole (p_3) to a high frequency associated with the loading variations in order not to affect the stability of the system. Even that the complex poles occurred at high frequency, the stability of the LDO regulator is still promised.

A. Implementation of the Simple Pole Tracking Technique

A simple scheme of pole tracking technique is shown in Fig. 3 [6]. The purpose of transistor M_{S1} is used to generate a large biasing current for reducing the equivalent resistance seen at the gate of power MOSFET when load current changes from light to heavy. In other words, it makes the second non-dominant pole (p_3) at the gate of power MOSFET moves to higher frequency (p_3'') at heavy load current. This pole tracking can alleviate the complex pole problem, which is shown in Fig. 4. The reason is that the location of high Q is located at a higher frequency than that of a LDO regulator without pole tracking technique. The loci of the first and second non-dominant poles are shown in Fig. 4. The less phase margin may happen when load current changes from heavy to light because the location of the first non-dominant pole (p_2''') is below the unit-gain frequency. It may cause the LDO regulator unstable. The locations of the first and second non-dominant poles are also listed in Fig. 4 to illustrate the scenario of less phase margin owing to the load current variations.

B. Implementation of the Equivalent Power MOSFET Array

In order to solve this problem, an equivalent power MOSFET array with smooth pole tracking technique is proposed in Fig. 5. An equivalent power MOSFET array is composed of three

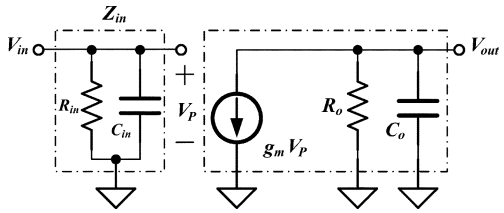

Fig. 6. Small signal circuit of a single power MOSFET stage.

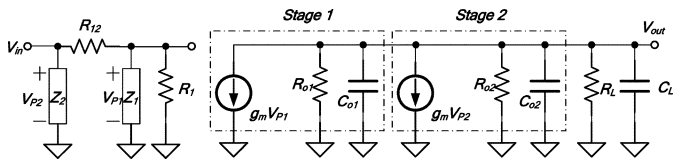

Fig. 7. Small signal circuit of power MOSFET array that contains two power MOSFET stages.

power MOS transistors with different aspects to each other for smoothly providing current to load. Resistor R_1 decides the biasing current of the power MOSFET stage. Besides, the turn-on/off sequence of the three power MOS transistors is controlled by three switches, which are transistors $M_{\rm PS1} \sim M_{\rm PS3}$. The resistors $R_{S1} \sim R_{S3}$ are designed to have the same size because we determine the on/off sequence of power MOSFET only by scaling the sizes of switches $M_{\rm PS1} \sim M_{\rm PS3}$.

The power MOSFET array makes the power stage be turned on/off in a proper sequence to achieve smooth pole tracking. Basically, the turn-on sequence is from the large power MOS transistor to the small power MOS transistor and the turn-off sequence is from the small size power MOS transistor to the large size power MOS transistor. The relationship between power MOS transistors and switches are based on a rule that a large power MOSFET is driven by a small switch and a small power MOSFET is driven by a large switch. In other words, the smaller switch can slow down the driving speed of large power MOS transistor for alleviating the large inrush current. It can prevent the operating point at the gate of power MOSFET is over-estimated. Contrarily, a large switch can speed up the turn-on/off of smaller power MOS transistors. Besides, resistors R_{12} and R_{23} are used to pull low the gate voltages at M_{P1} and M_{P2} to enhance the driving capability of the two power MOSFETs. The selection of the values of resistors R_1, R_{12}, and R_{23} depend on the location of the second non-dominant pole p_3 to avoid oscillating at light loads. Finally, the first non-dominant pole can be smoothly moved to higher frequency and back to lower frequency. It means that the phase margin is always enough to avoid incurring the unstable condition.

C. Design Methodology of the Power MOSFET Array for Achieving Smooth Pole Tracking Technique

The analysis of the power MOSFET array can be simplified by modeling one MOSFET stage in Fig. 6 at first. Two equivalent capacitances $C_{\rm in}$ and C_o are used to express the input and output capacitances seen at input and output nodes, respectively. Resistance $R_{\rm in}$ is composed of $1/g_{\rm ms}$ due to diode connected MOSFET switch and resistor R_S. The value of resistance $R_{\rm in}$ is written as

$$R_{\rm in} = R_s + \frac{1}{g_{\rm ms1}}. \tag{1}$$

Beside, the input impedance of a single stage is

$$Z_{\rm in} = \left(R_s + \frac{1}{g_{\rm ms}}\right) \left\| \frac{1}{s g_m R_o C_{gd}}. \right. \tag{2}$$

Thus, if the power MOSFET array contains two stages, the small signal can be expressed in Fig. 7. Z_1 and Z_2 are the equivalent input impedances seen at the gates of the first and second power MOSFET stages, respectively. The values of V_{p1} and $V_{\rm out}$ can be expressed by (3) and (4), respectively

$$V_{P1} = \left[\frac{R_1 \| Z_1}{(R_1 \| Z_1) + R_{12}}\right] V_{\rm in} \tag{3}$$

$$\frac{V_{\rm out}}{V_{\rm in}} = -\frac{g_{m2} + g_{m1}\left[\frac{R_1 \| Z_1}{(R_1 \| Z_1)+R_{12}}\right]}{\frac{1}{R_{o1}} + \frac{1}{R_{o2}} + \frac{1}{R_L} + \frac{sC_{\rm gd1}}{g_{m1}R_{o1}} + \frac{sC_{\rm gd2}}{g_{m2}R_{o2}} + sC_L}. \tag{4}$$

From (4), there are two poles in this transfer function. The $\rm pole_1$ is at the output node and written as (5). As we expect, the $\rm pole_1$ is the first non-dominant pole see at the output of the whole LDO system. The second pole $(\rm pole_2)$ can be derived and proportional to (6)

$$\rm pole_1 = \frac{\frac{1}{R_{o1}} + \frac{1}{R_{o2}} + \frac{1}{R_L}}{2\pi\left(\frac{C_{\rm gd1}}{g_{m1}R_{o1}} + \frac{C_{\rm gd2}}{g_{m2}R_{o2}} + C_L\right)} \tag{5}$$

$$\rm pole_2 \propto \frac{R_1 + R_{12} + R_1 R_s g_{ms1} + R_1 R_{12} g_{ms1} + R_s R_{12} g_{ms1}}{g_{m1}R_{o1}R_1R_{12}C_{gd1} + g_{m1}g_{ms1}R_{o1}R_1R_sR_{12}C_{gd1}}. \tag{6}$$

Assume that the orders of g_{m1} and $g_{\rm ms1}$ are probably equal to those of $1/R_{o1}$ and $1/R_s$, respectively. The second pole can be approximated as (7) because resistors R_S and R_{12} are much less than R_1 and R_S is less than R_{12}

$$\rm pole_2 \propto \frac{g_{ms1}}{C_{gd1}}. \tag{7}$$

The second pole contributes a second non-dominant pole to the whole LDO system. However, the power-on sequence of the power MOSFET array is from the power MOSFET with large size to the power MOSFET with small size. Thus, it means that we have to move this second non-dominant pole a high frequency. According to (7), the design methodology is expressed as (8).

$$g_{\rm ms1} > g_{\rm ms2} \text{ if } g_{\rm mp1} < g_{\rm mp2}. \tag{8}$$

Similarly, we can derive the transfer functions of the smooth pole-tracking structure that is composed of three power MOSFET stages in Fig. 5. If the input signal of power MOSFET array is at node V_{p3}, we can express the voltages of V_{p2} and V_{p1} by (9) and (10)

$$V_{P2} = \frac{[(R_1 \| Z_1) + R_{12}] \| Z_2}{\{[(R_1 \| Z_1) + R_{12}] \| Z_2\} + R_{23}} V_{P3} \tag{9}$$

$$V_{P1} = \frac{R_1 \| Z_1}{(R_1 \| Z_1) + R_{12}} V_{P2} = \frac{R_1 \| Z_1}{(R_1 \| Z_1) + R_{12}} \cdot \frac{[(R_1 \| Z_1) + R_{12}] \| Z_2}{\{[(R_1 \| Z_1) + R_{12}] \| Z_2\} + R_{23}} V_{\text{in}}. \tag{10}$$

Then, the transfer function can be expressed as shown in (11) at the bottom of the page.

The transfer function contains a second order denominator coefficient. Thus, we need to determine the positions of the two non-dominant poles. Similarly, the design methodology infers to a conclusion, which is expressed by (12)

$$g_{\text{ms1}} > g_{\text{ms2}} > g_{\text{ms3}} \text{ if } g_{\text{mp1}} < g_{\text{mp2}} < g_{\text{mp3}}. \tag{12}$$

Based on (12), the power MOSFET array can provide a smooth pole tracking mechanism in case of load variations. A larger power MOSFET is turned on prior to the smaller power MOSFET or vice versa. The inrush current is alleviated by the smaller switch for the large power MOSFET. The turn-on sequence of the switches $M_{\text{PS1}} \sim M_{\text{PS3}}$ can be determined by (12) when load current changes. Therefore, the relationship between power MOS transistors and switches are based on a rule that a large power MOSFET is driven by a small switch and a small power MOSFET is driven by a large switch. The overestimation condition is eliminated by our proposed power MOSFET array. The following subsection will discuss the design methodology of the values of Q and ω_0.

D. Decision of the Values of Q and ω_0 in the LDO Regulator

We adapt our proposed power MOSFET array to an LDO regulator with a four-stage error amplifier as an experimental circuit to decide the values of Q and ω_0. The architecture of the four-stage LDO regulator is shown in Fig. 8. In order to maintain the stability, we should determine the location of poles for different load conditions. At very light load condition, based on Miller compensation, there are two separate poles, which are expressed by (13) and (14). Owing to the frequency of the first non-dominant pole is higher than that of the crossover frequency. It means that the system has an enough phase margin. Certainly, the second non-dominant that is contributed by the gate capacitance of the power MOSFET is far away from these two poles

$$p_1 = \frac{1}{C_m G_{m2} G_{m3} G_{m4} R_{o1} R_{o2} R_{o3} R_{o4}} \tag{13}$$

$$p_2 = \frac{G_{m2} G_{m3} G_{m4} R_{o2} R_{o3}}{C_L}. \tag{14}$$

Basically, the transfer function can be easily derived and shown in (15) at the bottom of the next page. As we know, the

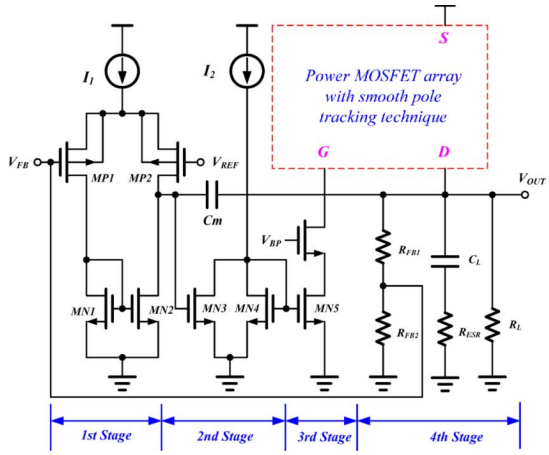

Fig. 8. LDO regulator that is composed of four gain stages is improved by the proposed power MOSFET array for achieving smooth pole tracking.

increased first non-dominant pole and the decreased second non-dominant pole form the complex poles when load current increases. It is obvious that the left term at the denominator contributes a dominant pole. Besides, the right term at the denominator is a second order polynomial and determines the existence of the complex poles. The existence condition of the complex poles is expressed by (16) shown at the bottom of the next page. The frequency of the complex poles and the Q-factor are described by (17) and (18), respectively, shown at the bottom of the next page.

The value of the transconductance G_{m4} is gradually increased by the conduction condition of the power MOSFET array. Owing to the increase of transconductance G_{m4} contributed by the smooth pole-tracking technique, it makes sure that the complex poles is at higher frequency than that of conventional design. Importantly, the increase of the Q-factor is also proportional to the value of G_{m4}. In other words, the transition from light load condition to heavy load condition, the value of the Q-factor is smoothly and slightly increased when we compare it to the high-Q condition occurred in the design with the simple pole-tracking technique. However, according to (18), the decreasing output impedance of the third stage effectively dominates the Q value. It makes sure that the high-Q condition will not happen in the proposed smooth pole tracking technique. In other words, the high-Q problem can be alleviated. The simulation results of the loop gain demonstrate the correctness of the analysis in Fig. 9.

The root loci of simple pole tracking and our proposed pole tracking techniques are shown in Fig. 10. The root locus of our proposed technique reveals that a high frequency complex pole is achieved compared to the low frequency complex pole in simple pole tracking technique [9]. It means that our proposed

$$\frac{V_{\text{out}}}{V_{P3}} = -\frac{g_{m3} + g_{m2} \frac{[(R_1 \| Z_1) + R_{12}] \| Z_2}{\{[(R_1 \| Z_1) + R_{12}] \| Z_2\} + R_{23}} + g_{m1} \frac{R_1 \| Z_1}{(_1 \| Z_1) + R_{12}} \cdot \frac{[(R_1 \| Z_1) + R_{12}] \| Z_2}{\{[(R_1 \| Z_1) + R_{12}] \| Z_2\} + R_{23}}}{\frac{1}{R_{o1}} + \frac{1}{R_{o2}} + \frac{1}{R_{o3}} + \frac{1}{R_L} + \frac{sC_{\text{gd1}}}{g_{m1} R_{o1}} + \frac{sC_{\text{gd2}}}{g_{m2} R_{o2}} + \frac{sC_{\text{gd3}}}{g_{m3} R_{o3}} + sC_L} \tag{11}$$

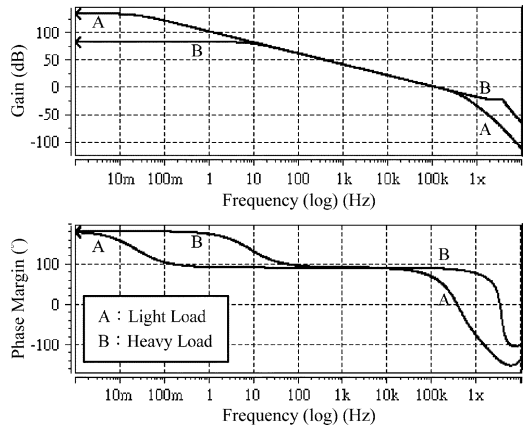

Fig. 9. Frequency response of closed loop-gain of the LDO with the proposed smooth pole tracking technique. (Curve A and B are simulated at load current equal to 1 and 400 mA, respectively).

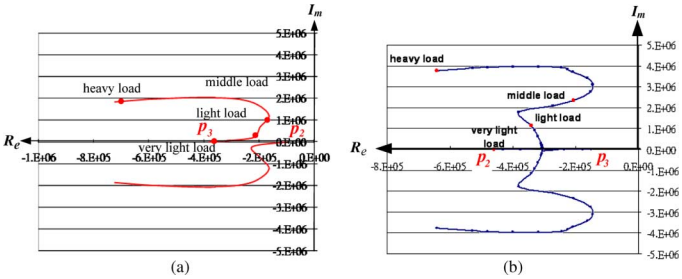

Fig. 10. Root loci of two types of pole tracking. (a) With simple pole tracking technique. (b) With our proposed pole tracking technique.

pole tracking can alleviate the high-Q problem in LDO regulators with a small output capacitor. It is obvious that we can use this power MOSFET array to substitute the power MOSFET of the LDO regulator with a small output capacitor. Therefore, the pole at the gate of power MOS transistor can have a good tracking with the pole at the output of the LDO regulator.

III. Experimental Results

The proposed LDO was fabricated in TSMC double-poly quadruple-metal 0.35-μm CMOS technology. The threshold voltages of nMOSFET and pMOSFET are 0.55 and 0.65 V, respectively. The chip micrograph is shown in Fig. 11 and the total silicon area is about 1315 μm $*$ 1430 μm, including the testing pads. The LDO can operate from 3.6 to 4.7 V with a

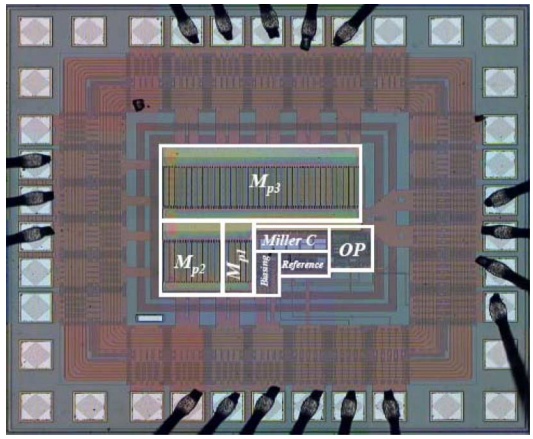

Fig. 11. Micrograph of chip.

regulated output voltage of 3.3 V. The dropout voltage at output current of 400 mA is 200 mV. The maximum ground current is about 100 μA at $V_{\text{in}} = 4.7$ V.

Load transient response with off-chip capacitor $C_L = 1$ μF at $V_{\text{IN}} = 3.6$ V has been tested to verify the stability of the proposed LDO. As shown in Fig. 12, the LDO output voltage has no oscillation when the load current changes from 100 uA to 400 mA in 1 μs or vice versa. The performance of transient response is critical in case of load variations. In order to achieve the better load transient response, the overshoot and undershoot voltages should be reduced to reasonable values. Moreover, the response time should be speed up to meet the specification of SoC systems.

Fig. 12(a) and (b) show the simple pole tracking result and the proposed smooth pole tracking result, respectively. When load current changes from light load to heavy, the dropout voltage of the smooth pole tracking is reduced from 10 mV got by simple pole tracking technique to 6.5 mV, which is shown in Fig. 12. While changing from heavy load to light load, the overshoot voltage of the smooth pole tracking technique is reduced from 47 to 5.5 mV. Importantly, there is no unstable condition occurred in our proposed technique at right-hand side of Fig. 12(b). However, we can find the scenario occurred in simple tracking technique at right side of Fig. 12(a). Furthermore, the transient response time is reduced from 52 to 7 μs. Smooth pole tracking technique promises low output ripples and small transient response time.

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{G_{m1}G_{m2}G_{m3}G_{m4}R_{o1}R_{o2}R_{o3}R_{o4}\left[1 - s\left(\frac{C_m}{G_{m2}G_{m3}G_{m4}R_{o2}R_{o3}} + \frac{C_{\text{gd3}}}{G_{m4}}\right) - s^2\left(\frac{C_m C_{\text{gd3}}}{G_{m2}G_{m3}G_{m4}R_{o2}}\right)\right]}{(1 + sC_m G_{m2}G_{m3}G_{m4}R_{o1}R_{o2}R_{o3}R_{o4})\left(1 + s\frac{C_L}{G_{m2}G_{m3}G_{m4}R_{o2}R_{o3}} + s^2\frac{C_{\text{gd3}}C_L}{G_{m2}G_{m3}G_{m4}R_{o2}}\right)} \tag{15}$$

$$\left(\frac{C_L}{G_{m2}G_{m3}G_{m4}R_{o2}R_{o3}}\right)^2 < 4 \cdot \frac{C_{\text{gd3}}C_L}{G_{m2}G_{m3}G_{m4}R_{o2}} \tag{16}$$

$$\omega_o = \sqrt{\frac{G_{m2}G_{m3}G_{m4}R_{o2}}{C_{\text{gd3}}C_L}} \tag{17}$$

$$Q = \sqrt{\frac{C_{\text{gd3}}C_L}{G_{m2}G_{m3}G_{m4}R_{o2}}}\frac{G_{m2}G_{m3}G_{m4}R_{o2}R_{o3}}{C_L} \tag{18}$$

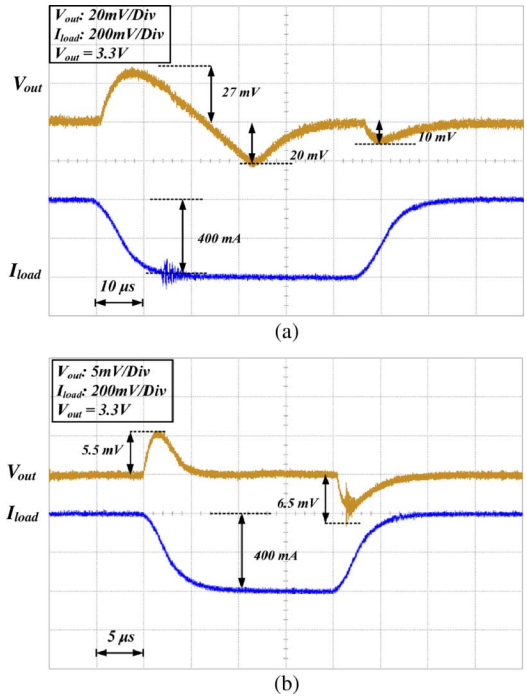

Fig. 12. Comparison of load transient response between smooth pole tracking and simple pole tracking techniques. Load current changes from 0.1 to 400 mA or vice versa. (a) With simple pole-tracking technique. (b) With the proposed smooth pole-tracking technique.

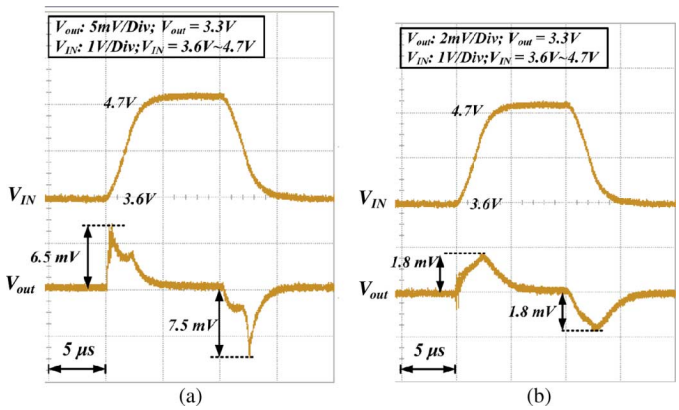

Fig. 13. Comparison of line transient response between smooth pole tracking and simple pole tracking techniques. Input voltage changes from 3.6 to 4.7 V or vice versa. (a) With simple pole-tracking technique. (b) With the proposed smooth pole-tracking technique.

Line transient response is illustrated in Fig. 13 when the input supply voltage changes from 3.6 to 4.7 V in 5 μs or vice versa. Both the results of output ripples are smaller than 1.8 mV. A summary of the proposed LDO regulator design parameters is shown in Table I.

IV. Conclusion

This paper proposes an equivalent power MOSFET array with a smooth pole tracking technique in low-dropout linear regulator. The power MOSFET array is turned on/off in a proper sequence to suppress the output ripples when a sudden variation occurs in load current. Furthermore, the proposed structure also provides a smooth pole tracking technique by tracking the load-dependent first non-dominant pole smoothly for alleviating the high-Q problem. The new proposed smooth pole tracking technique presents low output ripples and fast response time compared to conventional simple pole tracking technique. Experimental results promise the stability and show the improvement of load and line regulations.

TABLE I
Summary of the Proposed LDO Performance

Technology		*TSMC 0.35μm CMOS 2P4M*
Threshold Voltage		V_{THN}=0.55V and $\|V_{THP}\|$=0.75V
Input Voltage (V_{IN})		3.6V to 4.7V
Temperature Range		-40 °C ~ 95 °C
Output Voltage		3.3 V
Output Current		100μA to 400mA
Dropout Voltage		200mV@400mA
Output Capacitance		1μF, R_{ESR}=10mΩ
Line Regulation		400μV/V@400mA
Load Regulation		-0.153μV/mA@V_{IN}=3.6V
Loop-gain		138.6dB@0.1mA 82.8dB@400mA
Load Transient Response		5.5mV@0.1mA to 400mA 6.5mV@400mA to 0.1mA
Line Transient Response		1.8mV@V_{IN}=3.6V to 4.7V 1.8mV@ V_{IN}=4.7V to 3.6V
PSRR		
	f=2kHz	87dB@0.1mA 59dB@400mA
	f=100kHz	55dB@0.1mA 33dB@400mA
Active Chip Area		1315μm*1430μm (including testing pads)

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