# Method for Extracting Gate-Voltage-Dependent Source Injection Resistance of Modified Schottky Barrier (MSB) MOSFETs

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***Abstract*—The modified Schottky barrier (MSB) MOSFET with low-resistance metal source/drain and good short-channel effect immunity is one of the promising nanoscale device structures. In this letter, a modified external load resistance method was proposed to extract the bias-dependent source injection resistance of the MSB MOSFET for the first time. The effect of the thermal budget of the MSB process on the source injection resistance is reported. The injection resistance is exponentially proportional to $(V_{GS} - V_{th} - 0.5V_{DS})$ and would be close to the source/drain resistance of conventional MOSFETs at high gate bias. This work provides a good method to directly evaluate the efficiency of the MSB junction.**

***Index Terms*—Carrier injection, implantation-to-silicide (ITS), modified Schottky barrier (MSB), multigate FET (MuGFET).**

## I. Introduction

THE SCHOTTKY barrier (SB) MOSFET is one of the candidates for future nanoscale devices because of its easy processing, ultrashallow junction, and low source/drain (S/D) external resistance compared to the conventional p-n junction MOSFETs [1]–[5]. Recently, modified SB (MSB) MOSFETs have been proposed to improve the driving current and reserve the advantages of SB MOSFETs. The MSB junction is a Schottky junction with a very thin but high doping concentration layer located at silicide/Si-channel interface, which not only drastically improves driving capability by reducing and thinning the SB at source junction but also can significantly suppress the OFF-state leakage due to the thick SB at the drain junction. The MSB junction can be accomplished by either the implantation-to-silicide (ITS) method or the dopant segregation method [6], [7]. Several researches have been devoted to evaluate the efficiency of the MSB junction. Zhang *et al.* reported that the effective Schottky barrier height can be reduced to about 0.1 eV at high gate bias [8]. Kinoshita *et al.* reported the carrier injection velocity enhancement associated with the velocity overshoot [9]. It has been also reported that the current transport mechanism of SB and MSB MOSFETs may change from thermionic emission and tunneling to drift diffusion as the gate bias increases [10]. The gate bias for transport mechanism change decreases with the increase of the thermal budget for MSB junction formation. However, the source injection resistance and its gate bias dependence have not been reported. In this work, a modified external loading method is proposed to extract the bias-dependent S/D resistance. The bias-dependent source injection resistance of MSB MOSFETs provides a good indicator to evaluate the efficiency of the MSB junction and would be useful for device and circuit simulation.

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## II. Device Fabrication

Fully depleted n-channel SOI MSB MOSFETs fabricated by the ITS technique are used in this work. The process flow of an MSB MOSFET has been previously described in detail [11]. Therefore, we list some important process and structure parameters here. The thicknesses of the Si active layer and buried oxide layer were 40 and 150 nm, respectively. A thick $SiO_2$ hard mask layer was deposited on the Si layer so that only sidewall channels could be conducted. A 3-nm-thick $SiO_2$ was thermally grown as the gate dielectric followed by a 150-nm-thick poly-Si film deposition. The poly-Si gate was doped by $P_{31}^+$ ion implantation at 40 keV to a dose of $5 \times 10^{15}$ cm$^{-2}$ followed by a rapid thermal activation at 1025 °C for 10 s. Then, a $SiO_2$ (10 nm)/$Si_3N_4$ (20 nm) composite spacer was formed. The S/D region was completely converted into NiSi by a two-step annealing silicidation process. To form the MSB S/D junction, $P_{31}^+$ ions were implanted into the nickel silicide (ITS) at 20 keV to a dose of $5 \times 10^{15}$ cm$^{-2}$ followed by a post-ITS annealing step at 600 °C for 30 min or 30 s. During this annealing step, phosphorus ions diffused out of the silicide and piled up at the Si/silicide interface to form the MSB junction [11]. For the reference devices, phosphorus ions were implanted into the S/D region at 10 keV to a dose of $5 \times 10^{15}$ cm$^{-2}$ followed by a rapid thermal activation at 1025 °C for 20 s before the Ni-salicide process. The silicide thickness is about 25 nm.

Fig. 1 shows the typical transfer characteristics of an MSB MOSFET with $W/L = 80$ nm$/5$ $\mu$m biasing at $V_{DS} = 0.05$ V and operating at different temperatures. The inset shows the

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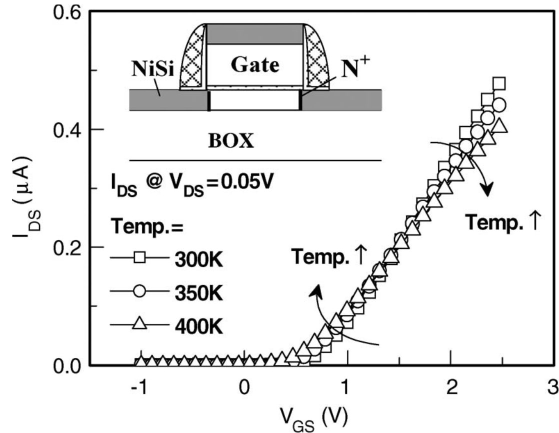


Fig. 1. Typical transfer characteristics of an MSB MOSFET with $W/L = 80$ nm/5 $\mu$m biasing at $V_{\rm DS} = 0.05$ V and operating at a different device temperature. The inset shows the device structure. The reversal of temperature dependence at $V_{\rm GS} = 1.35$ V indicates the change of current transport mechanism.

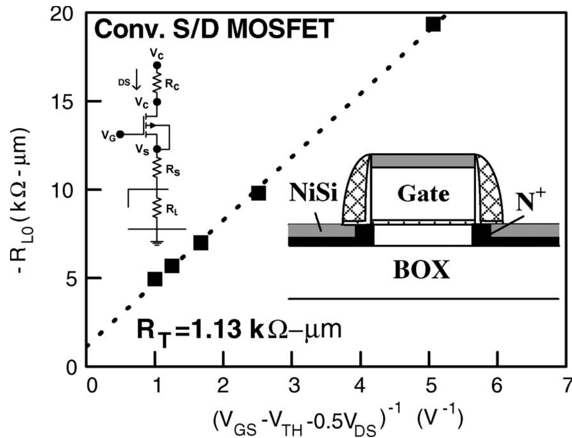


Fig. 2. $-R_{\rm L0}$ versus $1/(V_{\rm GS} - V_{\rm TH} - 0.5V_{\rm DS})$ plot of the conventional MOSFET. The insets show the circuit diagram of the external loading method and the device structure. The $V_{\rm DS}$ is 0.05 V.

schematic device structure. The ON-state current increases with temperature, increasing at low $V_{\rm GS}$. While at high $V_{\rm GS}$, the temperature dependence is reversed, and the intersecting point occurs at about $V_{\rm GS} = 1.35$ V. This intersection indicates that the ON current of the MSB MOSFET is dominated by a thermionic emission mechanism or a tunneling mechanism at low gate bias [10].

## III. Modified External Loading Method

The external loading method was proposed to extract the S/D resistance of the MOSFET by Hsu [12]. The benefit of this method is that only one device is measured, and the extracted result is exactly the S/D resistance of the measured device. The inset in Fig. 2 shows the circuit diagram of this method. An external load resistor with a suitable range of impedance is connected to the source terminal. The total resistance of the circuit is composed of external load resistance ($R_{\rm L}$), source resistance ($R_{\rm S}$), drain resistance ($R_{\rm D}$), and channel resistance,

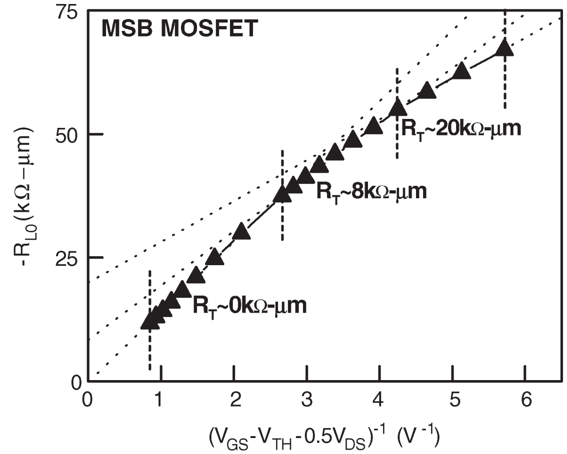


Fig. 3. $-R_{\rm L0}$ versus $1/(V_{\rm GS} - V_{\rm TH} - 0.5V_{\rm DS})$ plot of the MSB MOSFET with $W/L = 80$ nm/5 $\mu$m obtained by the modified external loading method. The $V_{\rm DS}$ is 0.05 V, and the post-ITS annealing time is 30 min.

where $R_{\rm S}$ and $R_{\rm D}$ depend on the properties of the MSB junction. The channel current ($I_{\rm DS}$) of the MOSFET operating at a linear region is given by

$$\begin{aligned} I_{\rm DS} &= \frac{W}{L}\mu C_{\rm ox}\left(V'_{\rm GS} - V_{\rm TH} - \frac{1}{2}V'_{\rm DS}\right)V'_{\rm DS} \\ &= K\Big\{\left[V_{\rm GS} - I_{\rm DS}(R_{\rm S} + R_{\rm L}) - V_{\rm TH}\right] \\ &\qquad - \frac{1}{2}\left[V_{\rm DS} - I_{\rm DS}(R_{\rm S} + R_{\rm D} + R_{\rm L})\right]\Big\} \\ &\quad \times \left[V_{\rm DS} - I_{\rm DS}(R_{\rm S} + R_{\rm D} + R_{\rm L})\right] \end{aligned}$$

where $K = (W/L)\mu C_{\rm ox}$, $W$ is the channel width, $L$ is the channel length, $\mu$ is carrier mobility, and $C_{\rm ox}$ is gate capacitance. This equation models the intrinsic channel property and is independent of the S/D junction. After some manipulations, this equation becomes

$$\frac{1}{I_{\rm DS}} = \frac{R_{\rm T} + R_{\rm L}}{V_{\rm DS}} + \frac{1}{K\left(V_{\rm GS} - V_{\rm TH} - \frac{1}{2}V_{\rm DS}\right)V_{\rm DS}} \tag{1}$$

where $R_{\rm T} = R_{\rm S} + R_{\rm D}$, and $R_{\rm T}$ represents the total external resistance of this MOSFET. Then, by plotting $1/I_{\rm DS}$ versus $R_{\rm L}$ with $V_{\rm GS}$ as a parameter, the $x$-axis intersection $R_{\rm L0}$ could be expressed as

$$-R_{\rm L0}(V_{\rm GS}) = R_{\rm T} + K^{-1}\left(V_{\rm GS} - V_{\rm TH} - \frac{1}{2}V_{\rm DS}\right)^{-1}. \tag{2}$$

By plotting $-R_{\rm L0}$ versus $1/(V_{\rm GS} - V_{\rm TH} - 0.5V_{\rm DS})$, the $y$-axis intersection gives $R_{\rm T}$.

The $-R_{\rm L0}$ versus $1/(V_{\rm GS} - V_{\rm TH} - 0.5V_{\rm DS})$ plot of the MOSFET with a conventional S/D junction is shown in Fig. 2, where the $V_{\rm DS}$ is 0.05 V. The good linearity as predicted by (2) confirms that the external loading method can be applied to SOI devices well. However, Fig. 3 shows that when using

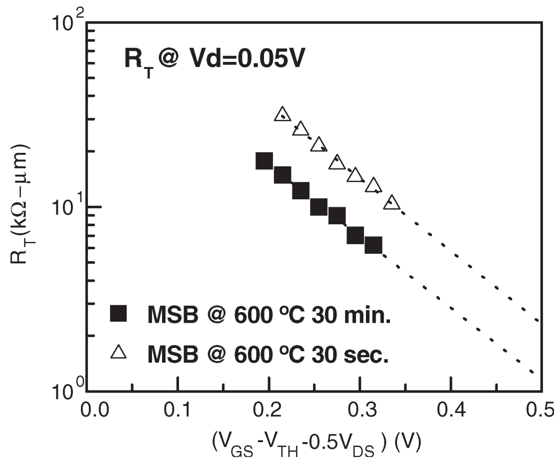


Fig. 4. Extracted $R_{\mathrm{T}}$ as a function of the $(V_{\mathrm{GS}} - V_{\mathrm{TH}} - 0.5V_{\mathrm{DS}})$ of the MSB MOSFET with $W/L = 80$ nm/5 $\mu$m. The $V_{\mathrm{DS}}$ is 0.05 V.

this method to the MSB MOSFET, the nonlinear $-R_{\mathrm{L0}}$ versus $1/(V_{\mathrm{GS}} - V_{\mathrm{TH}} - 0.5V_{\mathrm{DS}})$ plot deviates from (1). This difference arises from that the $R_{\mathrm{T}}$ of the MSB MOSFET is dependent on the bias condition, which conflicts with the basic assumption of the external loading method.

To solve this problem, we assume that $R_{\mathrm{T}}$ can be treated as a constant in a small $\Delta V_G$ range $(V_{\mathrm{GX}} \pm \Delta V_G/2)$. The $x$-axis intersection of the $-R_{\mathrm{L0}}$ versus $1/(V_{\mathrm{GS}} - V_{\mathrm{TH}} - 0.5V_{\mathrm{DS}})$ plot extracted at $V_{\mathrm{GS}} = V_{\mathrm{GX}} - \Delta V_G/2$, $V_{\mathrm{GX}}$, and $V_{\mathrm{GX}} + \Delta V_G/2$ could be explained as the $R_{\mathrm{T}}$ at $V_{\mathrm{GX}}$. Consequently, the bias dependence of $R_{\mathrm{T}}$ can be obtained by repeating this procedure. Fig. 4 shows the extracted $R_{\mathrm{T}}$ of the MSB MOSFET with 30-min and 30-s post-ITS annealing as a function of $(V_{\mathrm{GS}} - V_{\mathrm{TH}} - 0.5V_{\mathrm{DS}})$, where the $V_{\mathrm{DS}}$ is 0.05 V. It is observed that the $R_{\mathrm{T}}$ is exponentially proportional to the bias condition of $(V_{\mathrm{GS}} - V_{\mathrm{TH}} - 0.5V_{\mathrm{DS}})$. This is reasonable because the S/D resistance is dominated by the effective SB height at the source side, and the effective SB height is linearly proportional to $V_{\mathrm{GS}}$ in the measured $V_{\mathrm{GS}}$ range [8]. The $R_{\mathrm{T}}$ of the device with 30-min post-ITS annealing is much lower than that with 30-sec post-ITS annealing. This result indicates that a sufficient thermal budget is required to form an efficient MSB junction. Extrapolating $R_{\mathrm{T}}$ to $(V_{\mathrm{GS}} - V_{\mathrm{TH}} - 0.5V_{\mathrm{DS}}) = 0.5$ V, $R_T$ is 1.17 $K\Omega{-}\mu$m and is very close to that of the conventional MOSFET. It should be noted that as the device is biased at the ON state, the effect of MSB at the drain side is much smaller than the MSB at the source side. Therefore, the decrease of $R_{\mathrm{T}}$ is mainly attributed to the decrease of the source injection resistance.

## IV. Conclusion

In this letter, a modified external load resistance method has been proposed to extract the bias-dependent source injection resistance of the MSB MOSFET. It is observed that the source injection resistance is exponentially proportional to $(V_{\mathrm{GS}} - V_{\mathrm{TH}} - 0.5V_{\mathrm{DS}})$ and the S/D resistance of the MSB MOSFET would be close to that of the conventional MOSFET at moderate high gate bias. Without a sufficient post-ITS thermal budget, the source injection resistance cannot be effectively suppressed at reasonable $V_{\mathrm{GS}}$. This work provides a good method to directly evaluate the efficiency of the MSB junction.

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