A Millisecond-Anneal-Assisted Selective Fully Silicided (FUSI) Gate Process

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***Abstract*—We demonstrate, for the first time, an integration-friendly selective PMOSFET fully silicided (FUSI) gate process. In this process, a millisecond-anneal (MSA) technique is utilized for the nickel silicide phase transformation. A highly tensile FUSI gate electrode is created and hence exerts compressive stress in the underlying channel. The highly flexible integration scheme successfully, and exclusively, implements uniform P^+ FUSI gates for PMOSFETs while preserving a FUSI-free N^+ poly-Si gate for NMOSFETs with the feature size down to 30 nm. A 20% improvement in FUSI-gated PMOSFET I_{on}–I_{off} is measured, which can be attributed to the enhanced hole mobility and the elimination of P^+ poly-gate depletion.**

***Index Terms*—Fully silicided (FUSI), millisecond-anneal (MSA), MOSFET.**

I. Introduction

FULLY silicided (FUSI) gates have been intensively evaluated as an alternative to metal gates due to their excellent technological compatibility with current ULSI poly-Si gate processes. In previous works on the FUSI gate formation [1]–[4], poly-Si gates and source/drain (S/D) regions have undergone separate silicidation processes. In addition, both the extra CMP and lithography mask layers have been required. Consequently, greater process complexities are inevitable in conventional FUSI gate formation.

In this letter, we introduce, for the first time, a millisecond-anneal (MSA)-assisted nickel silicide phase transformation process, which forms FUSI gates and silicided S/D regions simultaneously. With the incorporation of nitrogen dopant in the N^+ poly-Si gates during the front-end fabrication processes, the MSA-assisted silicidation process can provide excellent selectivity to form a highly tensile FUSI solely on the P^+ poly-Si gates. This, in turn, delivers compressive stress in the PMOSFET channel region and hence enhances hole mobility without degrading electron mobility of NMOSFETs. The proposed method is fully compatible with existing strain engineering techniques such as SiGe S/D and strained contact etch-stop layers.

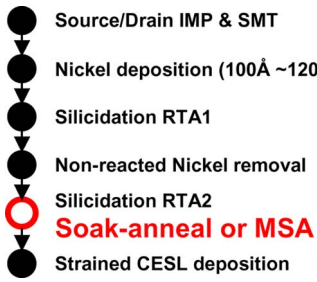

Fig. 1. Main process steps in the vicinity of silicidation process. Either a soak anneal or an MSA is utilized for RTA2 of silicidation.

II. Device Fabrication and Experiments

The devices under study are fabricated with a 1.2-nm (equivalent oxide thickness) nitrided gate oxide. A variety of strained silicon technology is used as described in [5] and [6]. Other device and process features can also be found elsewhere [6]. Fig. 1 shows the main process steps in the vicinity of silicidation. A two-step silicidation is adopted for both the regular and FUSI gate processes. After silicidation RTA1 and nonreacted nickel removal, the traditional soak RTA2 is replaced with the MSA. Without any additional process steps, the selective P^+ FUSI gate formation is realized by optimizing the MSA conditions.

III. Results and Discussion

Fig. 2 shows the relevant process conditions and TEM cross-sectional pictures of both the NMOSFETs and PMOSFETs under different MSA conditions. It is speculated that the effective temperature in the poly-Si gate is higher than that in the active area during MSA. This is reasonable because the poly-Si gate is surrounded by the spacer liner oxide and gate oxide, which are harmful to heat dissipation. However, the substrate serves as a heat sink for the active area and leads to a relatively lower temperature during the MSA process. There is a process window for MSA conditions, which allows for

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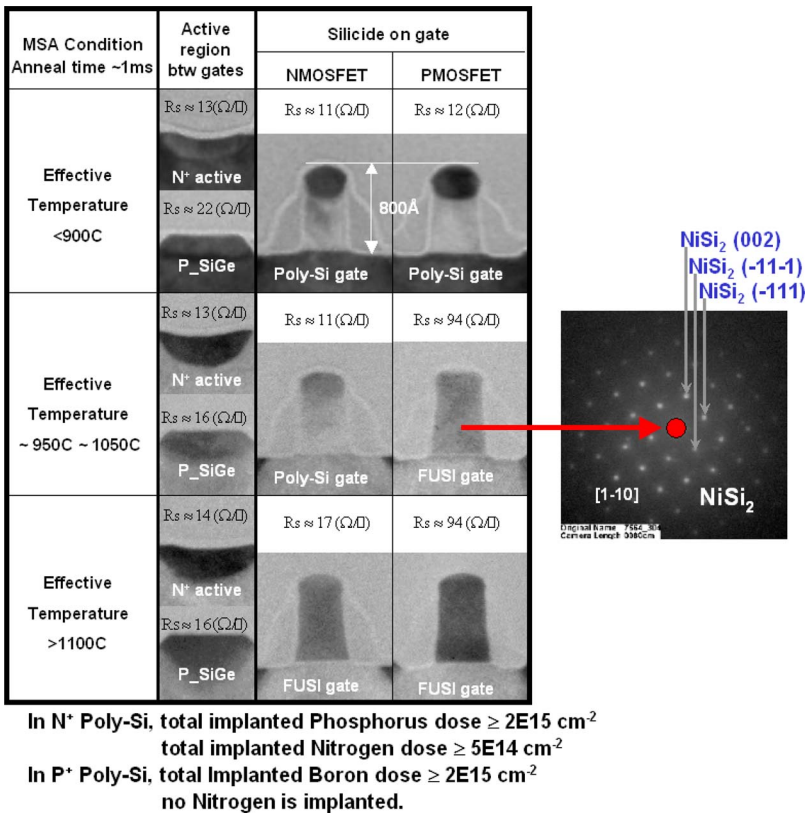

Fig. 2. TEM cross-sectional pictures of NMOSFET and PMOSFET under three MSA conditions. All the TEM pictures are shown in the same scale. The FUSI gate forms exclusively on the PMOSFET, whereas the N^+ poly-Si gate remains without FUSI under a moderate MSA condition. The silicide phase of the P^+ FUSI gate is $NiSi_2$. Sheet resistances of silicide in active regions and gate electrodes under different MSA conditions are shown in this figure. Relevant phosphorus, boron, and nitrogen I/I conditions in the gate electrodes are also exhibited.

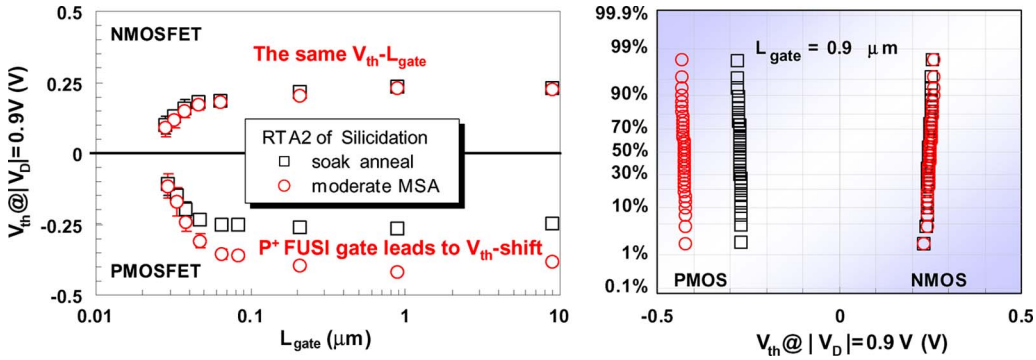

Fig. 3. (a) $V_{\rm th}$ versus $L_{\rm gate}$ behavior. Only PMOSFETs exhibit $V_{\rm th}$ shift. This indicates a selective FUSI gate formation exclusively on the PMOSFET. A lower halo I/I dose is used for the FUSI-gated PMOSFET to compensate for the WF shift. Smooth $V_{\rm th}$ roll-off curve indicates single-phase P^+ FUSI gate. (b). Tight $V_{\rm th}$ distributions are observed under a moderate MSA condition. $V_{\rm th}$ is unchanged for the NMOSFET. An obvious PMOSFET $V_{\rm th}$ shift with a tight distribution indicates a uniform P^+ FUSI gate formation.

both the FUSI gate and the normal active area silicidation to be formed at the same time. Because of the incorporation of nitrogen dopant in the N^+ poly-Si gate, silicidation is retarded [4]. Consequently, selective P^+ FUSI gate is formed under moderate MSA conditions. The silicide phase of the P^+ FUSI gate, confirmed by analyzing the electron diffraction pattern, is $NiSi_2$ (also shown in Fig. 2).

Both the threshold-voltage $(V_{\rm th})$ shift of long-channel PMOSFETs, as shown in Fig. 3(a), and the flatband-voltage $(V_{\rm FB})$ shift of the PMOSFET C–V curve (Fig. 4) clearly demonstrate a work-function (WF) shift. In order to provide similar $V_{\rm th}$ level for FUSI-gated and non-FUSI-gated short-channel devices, a lower halo ion-implantation (I/I) dose has been utilized with the FUSI process, in this case, to compensate for the WF shift. A steeper PMOSFET $V_{\rm th}$ roll-off slope arises from the lower halo I/I dose. Smooth PMOSFET $V_{\rm th}$ roll-off behavior also indicates single-phase P^+ FUSI gates for gate lengths $(L_{\rm gate})$ ranging from 10 μm to 30 nm. Further evidence of the uniformity of P^+ FUSI gate formation is seen in the tight PMOSFET $V_{\rm th}$ distribution shown in Fig. 3(b). As for the NMOSFET, a moderate MSA condition leads to little $V_{\rm th}$ difference compared to soak RTA2 for all gate lengths shown in the upper part of Fig. 3(a). A tight NMOSFET $V_{\rm th}$ distribution, as shown in Fig. 3(b), indicates that all of the

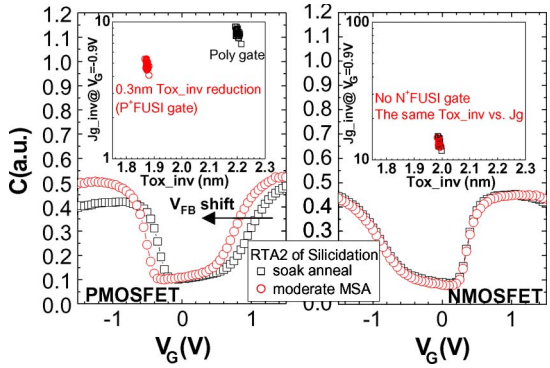

Fig. 4. C–V curves of NMOS and PMOS using a moderate MSA condition for silicidation. The PMOS shows a clear $V_{\rm FB}$ shift that indicates WF shift for only the PMOSFET. The FUSI-gated PMOSFET shows a 0.3-nm thinner $T_{\rm ox\_inv}$ because of the reduction of poly-gate depletion. The NMOSFET shows no noticeable change under a moderate MSA condition.

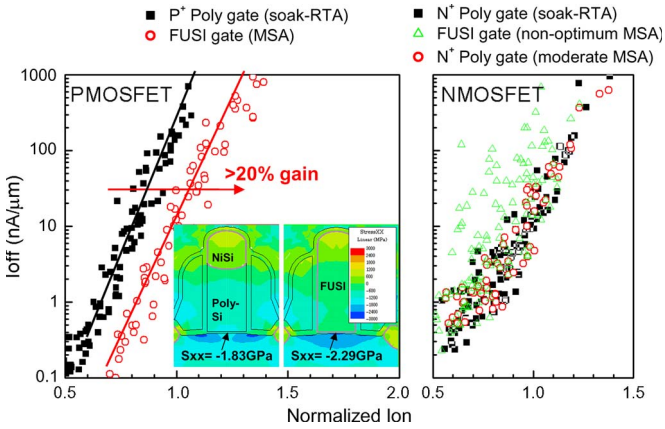

Fig. 5. P^+ FUSI gate improves PMOSFET $I_{\rm on}$–$I_{\rm off}$ by more than 20%. The NMOSFET keeps similar $I_{\rm on}$–$I_{\rm off}$ performance when a moderate MSA condition is utilized for FUSI gate formation exclusively on P^+ poly-Si while preventing FUSI gate formation on N^+ poly-Si. The highly tensile FUSI gate imposes a stronger compressive stress in the channel region compared to the poly-Si gate.

N^+ poly-Si gates remain without FUSI. The NMOSFET shows an unchanged inversion gate oxide thickness $(T_{\rm ox\_inv})$ versus gate current (J_g) characteristic, whereas the PMOSFET clearly demonstrates a 0.3-nm thinner $T_{\rm ox\_inv}$ for a given (J_g), as shown in the inset of Fig. 4. This can serve as experimental evidence of the reduction in PMOSFET gate depletion, which is valid only for P^+ FUSI gate formation.

Fig. 5 shows the difference in device $I_{\rm on}$–$I_{\rm off}$ performance between non-FUSI and FUSI gates. The NMOSFET undergoes an obvious degradation when N^+ FUSI gates are formed under nonoptimum MSA conditions. This indicates that the "memorized" strain resulting from SMT is relaxed due to consumption of N^+ poly-Si gate. This is consistent with experimental observations published in the literature [4]. To avoid this $I_{\rm on}$–$I_{\rm off}$ degradation in NMOSFETs, we further optimize the MSA-assisted silicidation process to minimize N^+ poly-Si consumption while maintaining FUSI gate formation on P^+ poly-Si. The NMOSFET $I_{\rm on}$–$I_{\rm off}$ degradation is thereby prevented, whereas the PMOSFET FUSI gate devices reveal substantial enhancement in $I_{\rm on}$–$I_{\rm off}$ performance of more than 20%. The PMOSFET enhancement can be attributed to the following two factors: first, the thinner $T_{\rm ox\_inv}$ resulting from reduction of poly-gate depletion, and second, the change in mechanical stress induced by the FUSI gate. Based on measurement data, the stress level of the MSA-assisted FUSI gate is found to be ∼500 MPa more tensile than that of the poly-Si gate after silicidation. Hence, a FUSI gate imposes a stronger compressive stress on the underlying PMOSFET channel region (see the inset of Fig. 5 for the simulated stress distributions), which, in turn, enhances hole mobility.

IV. Conclusion

An MSA-assisted FUSI gate silicidation process has been, for the first time, proposed in this letter. By means of the optimum MSA conditions for silicide phase transformation, single-phase FUSI gates have been uniformly formed for PMOSFETs while preserving a FUSI-free N^+ poly-Si gate for NMOSFETs with the feature size down to 30 nm. The enhancement factor of the FUSI-gated PMOSFET $I_{\rm on}$–$I_{\rm off}$ has been measured to exceed 20%. Silicidation for both the active areas and poly-Si gates has been achieved simultaneously, without requiring conventional CMP, lithography layers, or poly-Si etch-back processes. It has therefore been argued that these unique features make the presented method very friendly with the process integration.

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