Design and Analysis of CMOS Subharmonic Injection-Locked Frequency Triplers

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Abstract—K- and V-band CMOS differential subharmonic injection-locked frequency triplers (ILFTs) are proposed, analyzed, and designed. Based on the proposed ILFT structure, models for the injection-locking range and the output phase noise are developed. A K-band ILFT is designed and fabricated using 0.18-μm standard CMOS technology. The measured injection-locking range is 1092 MHz with a dc power consumption of 0.45 mW and an input injection power of 4 dBm. The harmonic rejection ratios are 22.65, 30.58, 29.29, 40.35 dBc for the first, second, fourth, and fifth harmonics, respectively. The total injection-locking range of the K-band ILFT can achieve 3915 MHz when the varactors are used and the dc power consumption is increased to 2.95 mW. A V-band ILFT is also designed and fabricated using 0.13-μm standard CMOS technology. The measured injection-locking range is 1422 MHz with 1.86-mW dc power consumption and 6-dBm input injection power. The injection-locking range of the proposed ILFT is similar to the tuning range of a conventional varactor-tuned bulk-CMOS voltage-controlled oscillator (VCO). Moreover, the proposed ILFT has a greater output power and a lower dc power consumption level than a VCO. As a result, it is feasible to use the proposed ILFT in low-power millimeter-wave synthesizers.

Index Terms—Frequency tripler, injection-locked oscillators (ILOs), RF CMOS, voltage-controlled oscillator (VCO).

I. INTRODUCTION

IN THE millimeter-wave band, there are two methods to generate local oscillator (LO) signals. In the first method, LO signals are generated directly by using fundamental frequency oscillators [1]–[3]. In the second one, they are generated by using lower frequency oscillators cascaded with frequency multipliers to obtain signals at the desired frequencies [4]–[6]. Due to the limited performance of active and passive devices at high frequency, it is easier to design high-performance voltage-controlled oscillators (VCOs) at low frequency rather than at high frequency. Moreover, high-frequency dividers operated at the carrier frequency with a significant amount of power dissipation are not needed when using a low-frequency VCO. Therefore, the second method is advantageous in CMOS circuit implementation. However, the key design requirement of the second method is to increase the frequency conversion gain of the frequency multipliers. In order to achieve this requirement, low input injection power and low dc power consumption are necessary to obtain the desired output power level.

Frequency multipliers integrated with injection-locked oscillators (ILOs) [7]–[9] can efficiently increase the conversion gain because ILOs have the superior properties of frequency stabilization and high gain amplification with a narrow bandwidth [10]. Such a frequency multiplier with an ILO is called a subharmonic injection-locked frequency multiplier (ILFM). It offers great potential use with millimeter-wave frequency synthesizers because of its low input injection power. Even with low input injection power, the proposed subharmonic ILFM can provide the same performance as a conventional frequency multiplier [11]. Thus far, all the proposed subharmonic ILFMs [7]–[9] have not been implemented using the silicon CMOS process and they are only suitable for single-ended modulation applications.

In this paper, a new CMOS fully differential subharmonic injection-locked frequency tripler (ILFT) is proposed and analyzed. It is suitable for complex modulation schemes because of its fully differential structure. The injection-locking range of the proposed ILFT is improved by inserting the frequency pre-generator circuit before the ILO. The main advantage of a frequency pre-generator is that the injection-locking range can be maximized with little degradation of ILO output performance. An analytical model is developed to characterize both the injection-locking range and the output phase noise of the proposed ILFT. The proposed K-band ILFT is fabricated using 0.18-μm CMOS technology. According to the measured results, it has an injection-locking range of 1092-MHz width with an input injection power of only 4 dBm and a dc power consumption of 0.45 mW. Moreover, the output power can achieve -9.4 dBm with 10.5-dB phase noise higher than that of the input injection signal. This paper shows that the key design requirement can be achieved in the proposed ILFT. Finally, the theoretical results are verified by the experimental results.

In Section II, the model for the proposed ILFT is derived. The CMOS circuit implementation is described in Section III. The experimental results are presented in Section IV. Finally, a conclusion and summary are given in Section V.

II. THEORETICAL MODEL

Based upon the locking mechanism for a small injection signal [10] and the simple ILO model [12], a physical representation of the proposed ILFT with a frequency pre-generator to generate the third harmonic signal connected to an ILO is shown in Fig. 1. In the ILO model, $H(j\omega)$ is the transfer function of the bandpass LC-tank filter used to eliminate undesired frequencies generated by the frequency pre-generator. The active devices of the ILO are modeled as the linear constant transconductance stage G_m. The frequency pre-generator is modeled as the nonlinear characteristic function $f(v_I)$. Both the G_m and $H(j\omega)$ with a feedback path form the ILO.
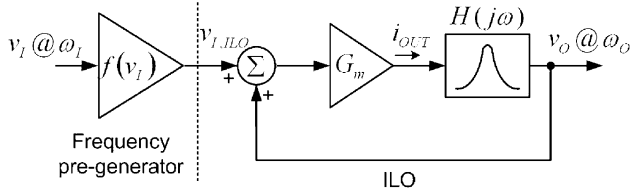
Fig. 1. Model of the proposed ILFT.

Without any input signal, the ILO has a steady output signal if the Barkhausen criterion is satisfied in the close-loop structure. An incident signal $v_I(t)$ with input frequency ω_I is injected into the oscillator via a frequency pre-generator. The output frequency ω_O is the function of input frequency ω_I while the oscillator is under the locked situation.

If the ILFT is under the locked condition, the following apply:

$$v_I(t) = V_i \cos(\omega_I t + \theta) \tag{1}$$

$$v_O(t) = V_o \cos(\omega_O t) \tag{2}$$

$$v_{I,\text{ILO}}(t) = f(v_I(t)) = f(V_i \cos(\omega_I t + \theta)) \tag{3}$$

where $v_I(t)$ is the incident signal with input frequency ω_I, amplitude V_i, and phase θ, $v_O(t)$ is the output signal with frequency $\omega_O = 3\omega_I$ and amplitude V_o, and $v_{I,\text{ILO}}(t)$ is the output signal of the frequency pre-generator.

From [13], $v_{I,\text{ILO}}(t)$ can be expressed as a polynomial series

$$\begin{aligned} v_{I,\text{ILO}}(t) &= f(v_I(t)) \\ &= \sum_{n=0}^{\infty} a_n (v_I(t))^n \\ &= a_0 + a_1 v_I(t) + a_2 (v_I(t))^2 + a_3 (v_I(t))^3 \\ &\quad + O((v_I(t))^4) \end{aligned} \tag{4}$$

where a_n is the coefficient of polynomial f, and $O((v_I(t))^4)$ is the terms of order higher than three. The coefficient a_3 is proportional to the conversion gain of the third harmonic frequency generator. The output current of the transconductance stage G_m can been written as

$$i_{\text{OUT}} = G_m[f(v_I(t)) + v_O(t)] = G_m[v_{I,\text{ILO}}(t) + v_O(t)]. \tag{5}$$

Using (4) and (5), the normalized injection-locking range can be derived as

$$\frac{|\omega - \omega_r|}{\omega_r} \le \frac{1}{2Q} \sqrt{\frac{(a_3 V_i^3)^2}{(4V_o)^2 - (a_3 V_i^3)^2}} \approx \frac{1}{2Q} \left| \frac{a_3 V_i^3}{4V_o} \right| \tag{6}$$

where ω_r and Q are the resonant frequency and quality factor of the LC tank in the bandpass filter, respectively. The output voltage amplitude can be expressed as

$$V_o = G_m H_0 \sqrt{\left[V_o + \left(\frac{a_3 V_i^3}{4} \right) \cos 3\theta \right]^2} \tag{7}$$

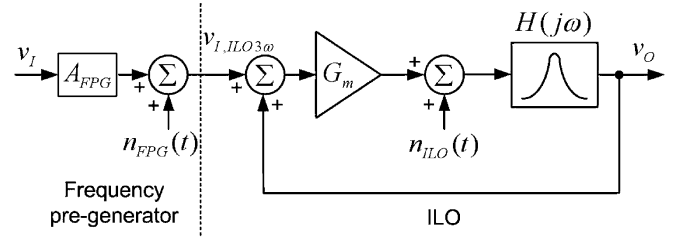where H_0 is the impedance of the LC tank at resonant frequency.

Fig. 2. Simplified noise source model in the proposed ILFT.

Assuming $V_o + (a_3 V_i^3 \cos 3\theta / 4) > 0$, the expression of the output amplitude can be rewritten as

$$V_o = \frac{a_3 G_m H_0 V_i^3 \cos 3\theta}{4(1 - G_m H_0)}. \tag{8}$$

The detailed derivations are given in Appendix A.

In general, the injection-locking range is limited by failure of either the phase condition (6) or the gain condition (7) [12]. From (6), it can be seen that the injection-locking range increases with an increase in either the conversion gain of the frequency pre-generator or the incident amplitude V_i. The degradation of the LC-tank quality factor Q can also improve the injection-locking range. However, the latter causes a decrease in the impedance of the LC tank H_0 and, thus, the output voltage amplitude also decreases (8). This result is consistent with the results in [10]. According to the proposed ILFT model, the design principle can be developed. It can be seen from (8) that the quality factor of the LC tank can be maximized in order to obtain increased output amplitude. The resulting degradation of the injection-locking range can be improved by increasing of the conversion gain of the frequency pre-generator (6).

The overall ILO output phase noise is characterized by the noise contributions of all blocks in an ILO [14]. The simplified noise source model of the proposed ILFT is shown in Fig. 2 where the conversion gain of the third harmonic signal in the frequency pre-generator is simplified to be a constant value A_{FPG}, and $v_{I,\text{ILO}3\omega}$ is the signal with frequency $3\omega_I$. The noise contribution from the frequency pre-generator and the ILO are modeled as $n_{\text{FPG}}(t)$ and $n_{\text{ILO}}(t)$, respectively. The linear phase-domain model [15] is adopted to calculate the output phase noise.

The derived output phase noise can be expressed as

$$\begin{aligned} S_{\text{OUT}}(\omega_m) &= \frac{3^2}{1 + \left(\dfrac{\omega_m}{\omega_p} \right)^2} S_{\text{INJ}}(\omega_m) \\ &\quad + \frac{1}{1 + \left(\dfrac{\omega_m}{\omega_p} \right)^2} S_{\text{FPG}}(\omega_m) \\ &\quad + \frac{\left(\dfrac{\omega_m}{\omega_p} \right)^2}{1 + \left(\dfrac{\omega_m}{\omega_p} \right)^2} S_{\text{FreeRun}}(\omega_m) \end{aligned} \tag{9}$$

where the corner frequency of the ILFT noise transfer function ω_p can be written as

$$\omega_p = \frac{\omega_r}{2Q}\frac{\eta}{1+\eta} \qquad (10)$$

$$\eta = \frac{A_{\mathrm{FPG}}V_i}{V_o}. \qquad (11)$$

In the above equations, ω_m is the offset frequency from output frequency ω_O and $S_{\mathrm{OUT}}(\omega_m), S_{\mathrm{INJ}}(\omega_m), S_{\mathrm{FPG}}(\omega_m)$, and $S_{\mathrm{FreeRun}}(\omega_m)$ are the phase noise spectral densities of output, input injection signal, frequency pre-generator, and internal circuits, respectively. The detailed derivation of the output phase noise is given in Appendix B.

As may be seen from the first and the second terms in (9), the noise from the input injection signal and frequency pre-generator are passed through the low-pass filter so that their noise transfer functions have low-pass transfer characteristics. Thus, the output phase noise is dominated by these two noise sources at small offset frequency ω_m. If the noise contribution from the frequency pre-generator is negligible, the output phase noise is 9.5 dB $[= 10\log(3^2)]$ higher than that from the input injection signal with a small offset frequency. The noise from internal circuits, as given in the third term of (9), has a high-pass transfer characteristic. At large offset frequency ω_m, the output phase noise is dominated by this noise and has a high-pass shape. To minimize the output phase noise, the corner frequency ω_p can be increased to filter out the internal noise. As may be seen from (10) and (11), ω_p can be increased by either degradation of the LC-tank quality factor Q or the high incident amplitude V_i.

A summary of the proposed ILFT can be developed from (6)–(11). The quality factor Q of the LC tank is maximized for a large output voltage swing and low-power consumption. The degradation of the injection-locking range and the output phase noise from the increase in quality factor Q can be compensated for by increasing the conversion gain of the frequency pre-generator.

III. CIRCUIT IMPLEMENTATION

The proposed CMOS ILFT circuit is shown in Fig. 3. The off-chip transformer T1 is designed to generate the differential input signal. The function of the frequency pre-generator is implemented by M1 and M2. The design guideline of M1 and M2 is the same as for the conventional frequency multipliers in [16]. The gate bias V_{BIAS} of M1 and M2 is fed from the input off-chip transformer T1 and the conversion gain of the frequency pre-generator can be maximized with an appropriate V_{BIAS} value. The tripled-frequency signal generated by the frequency pre-generator is injected into the ILO formed by M3, M4, C1, C2, L1, and L2. The selected values of inductors L1/L2 and varactors C1/C2 are chosen so that their resonant frequency is close to the third harmonic frequency of the input injection signal. According to the design guideline in Section II, the quality factor of the LC tank is maximized for a large output swing and low power consumption. V_{TUNE} is the external controlled signal used to increase the injection-locking range. M3
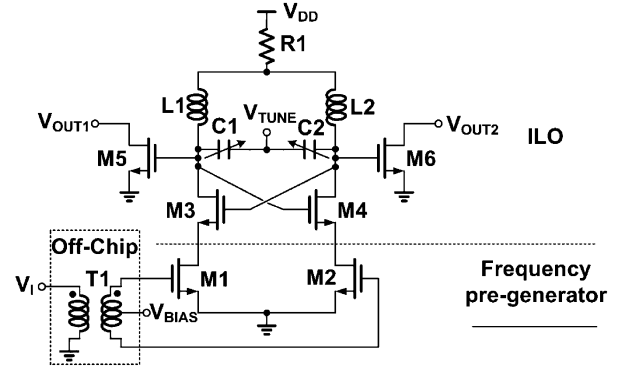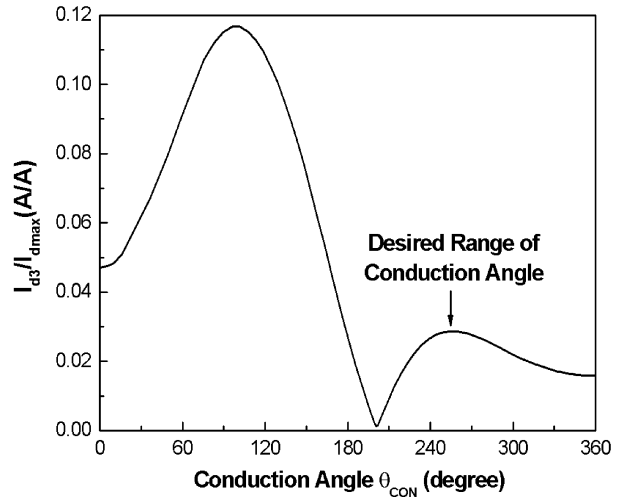

Fig. 3. Schematic of the proposed ILFT.

Fig. 4. HSPICE simulated coefficient of output harmonic current as a function of conduction angle.

and M4 are used to generate the negative resistance to compensate for the loss of the LC tank. R1 is designed for the improvement of the harmonic rejection ratios (HRRs). Finally, the output signals are taken from the open-drain buffers for test purposes. The proposed ILFT has a current-reuse structure between the frequency pre-generator and the ILO for low power operation.

Fig. 4 shows the HSPICE simulated normalized third harmonic currents $I_{d3}/I_{d\max}$ of the frequency pre-generator M1/M2 as a function of conduction angle (θ_{CON}), where I_{d3} is the output amplitude of the drain current at the third harmonic frequency, $I_{d\max}$ is defined as the maximum peak-to-peak output drain current, and conduction angle is the device turn-on angle within one period of the input signal. The simulation condition involves an 8-GHz input signal with 4-dBm input injection power and a MOS device with dimensions of W/L $= 18 \ \mu$m/0.18 μm with gate–source bias voltage changing from 0.03 to 1.03 V. Due to the parasitic capacitance of the device, the ac current between the gate and drain is included in the output drain current $I_{d\max}$. Thus, the normalized harmonic current curve in Fig. 4 is not the same as the ideal switch condition in [16]. The maximum output third harmonic current occurs when the conduction angle is 100°. With this conduction angle, the devices M1/M2 must be biased at the
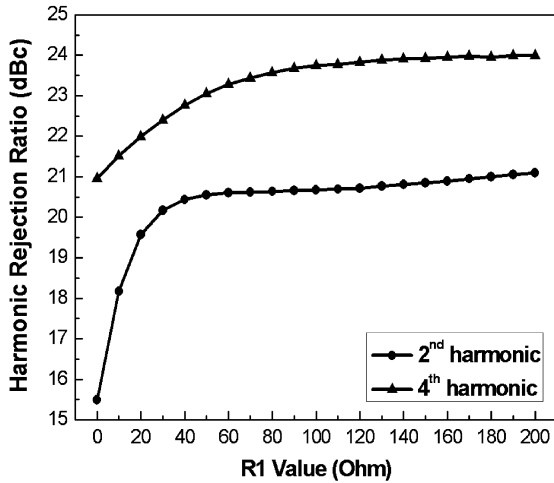
Fig. 5. HSPICE simulated HRRs for various value of R1.

Fig. 6. Chip microphotograph of K-band ILFT (0.66 mm $\times$ 0.69 mm).

Fig. 7. Chip microphotograph of V-band ILFT (0.59 mm $\times$ 0.66 mm).

weak-inversion region. Under this condition, the ILO circuits may not satisfy the oscillation condition with such a small dc current. In the proposed ILFT, the frequency tripled function devices (M1 and M2) are biased at a conduction angle of 250° for higher frequency conversion efficiency while maintaining oscillation. V_{BIAS} can be calculated by a given input injection power, a device threshold voltage, and a suitable conduction angle [16].

Since the even harmonic signals are common-mode signals, an appropriate value for resistor R1 is set to eliminate the undesired even harmonic signals. To verify the effect of R1, Fig. 5 shows the HSPICE simulation results of the second and fourth HRRs for various values of R1 in the K-band ILFT design. It can be seen that the HRR can be improved with a small R1 value. When the R1 value is 90 Ω, the HRRs improve with only a small voltage drop for the K-band ILFT. However, for the V-band ILFT, the R1 value needs only to be 55 Ω because of the low nominal power supply voltage in 0.13-μm CMOS technology.

IV. EXPERIMENTAL RESULTS

Based upon the proposed ILFT circuit structure, both K- and V-band ILFTs are designed and fabricated using 0.18- and 0.13-μm CMOS technologies, respectively. The chip microphotograph of the K-band ILFT is shown in Fig. 6: the chip area is 0.66 mm $\times$ 0.69 mm. The varactors C1/C2 are not included in the V-band ILFT. Hence, the selected value of inductors L1/L2 is chosen so that they can resonate with the total parasitic capacitances at the drain of M3/M4 at the third harmonic frequency of the input injection signal. The chip photograph of the V-band ILFT is shown in Fig. 7: the chip area is 0.59 mm $\times$ 0.66 mm. The chip areas of both the proposed ILFTs are limited by the minimum distance between the pads.

An on-wafer measurement system incorporating a probe station, ground–signal–ground (GSG) coplanar probes (up to 67 GHz), and high-speed cable (up to 50 GHz) is used to measure chip performance. The input injection signal for the fabricated K-band ILFT is from an analog signal generator and is connected to a 180° hybrid coupler. The output power is measured by a spectrum analyzer. A waveguide harmonic mixer is used to measure the output power of the fabricated
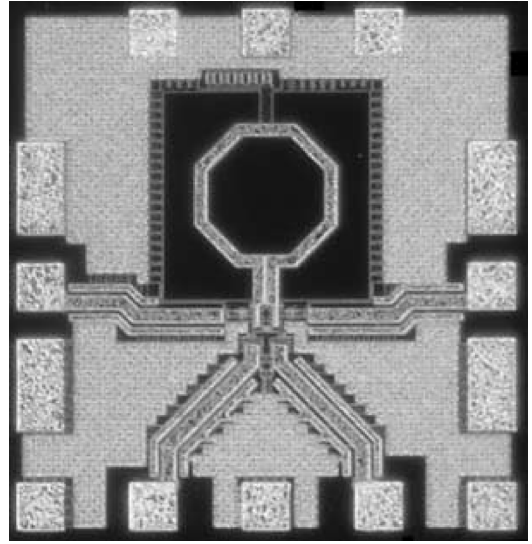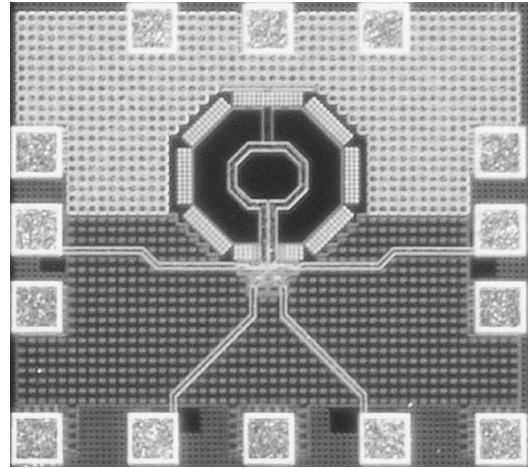
V-band ILFT. Additionally, due to the higher cable loss of input signal for the V-band ILFT, a microwave system amplifier is used to compensate the loss.

A. K-Band ILFT

The fabricated K-band ILFT starts to oscillate at a bias current of 0.79 mA from 1.5 V. The measured output spectra of the K-band ILFT versus the output frequency under free-running and locked conditions with probe and cable losses are shown in Fig. 8(a) and (b), respectively. The measured peak output power is -22 dBm at 26.486 GHz under free-running condition and -9.4 dBm at 26.486 GHz under locked condition with a 4-dBm input injection power, a V_{BIAS} of 0.56 V, and 4.7-dB power loss from cable and probe. Due to the contribution of input injection power, the locked ILFT has a higher output power than the free-running ILFT. The expected output power under locked conduction is -2 dBm, which is a 2.7-dB difference from the measurement result.

The measured input injection power versus the output frequency when the input bias V_{BIAS} is set at 0.56 V is shown
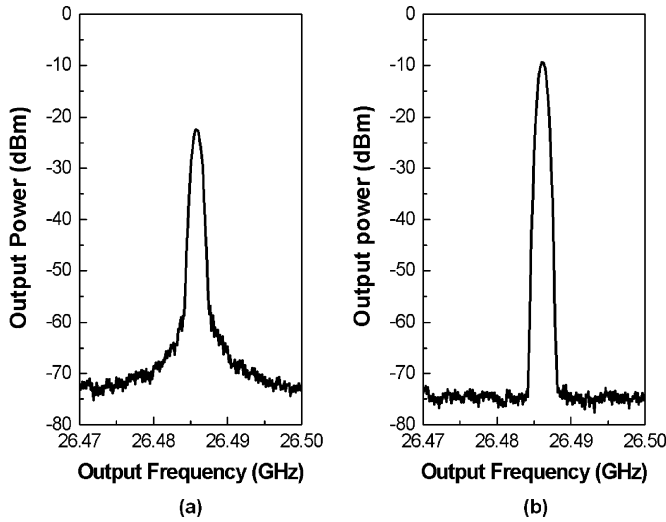
Fig. 8. Measured output spectra of the fabricated K-band ILFT under: (a) free-running and (b) locked conditions with probe and cable losses.
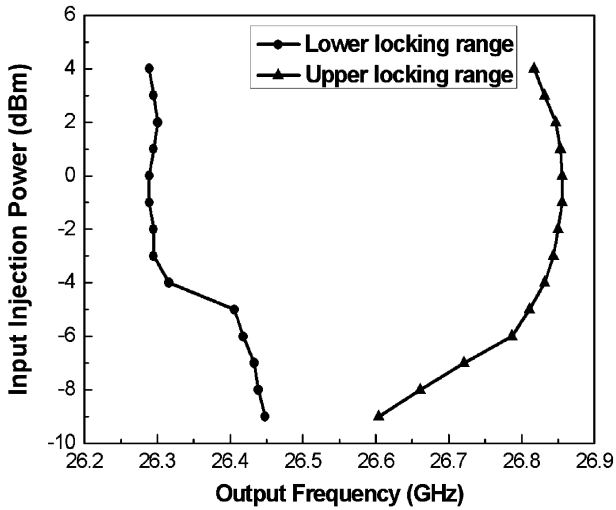

Fig. 10. Simulated and measured injection-locking ranges versus input injection power with 1.5-V V_{TUNE} for K-band ILFT.

Fig. 9. Measured input injection power versus output frequency with 1.5-V V_{TUNE} for K-band ILFT.

Fig. 11. Injection-locking range as a function of input bias V_{BIAS} with 4-dBm input injection power and 1.5-V V_{TUNE} for K-band ILFT.

in Fig. 9. The upper and lower locking ranges are labeled as the maximum and minimum output frequencies under locked condition, respectively. The simulated and measured injection-locking ranges versus input injection power are shown in Fig. 10 where the measured injection-locking range is from 156 to 567 MHz, while the input injection power varies from -9 to -1 dBm. At an input injection power greater than 0 dBm, the injection-locking range decrease slightly, as shown in Fig. 10. With small input injection power, the measurement result is close to the simulation result. With large input injection power, the measured injection-locking range is smaller by 100 MHz. This is because the valid frequency range of the simulation model is not completely covered with the desired frequency range.

The injection-locking range is mainly determined by two important factors. One is the nonlinear term a_3 of the frequency pre-generator, whereas the other is the nonlinear characteristic of the ILO. As input inj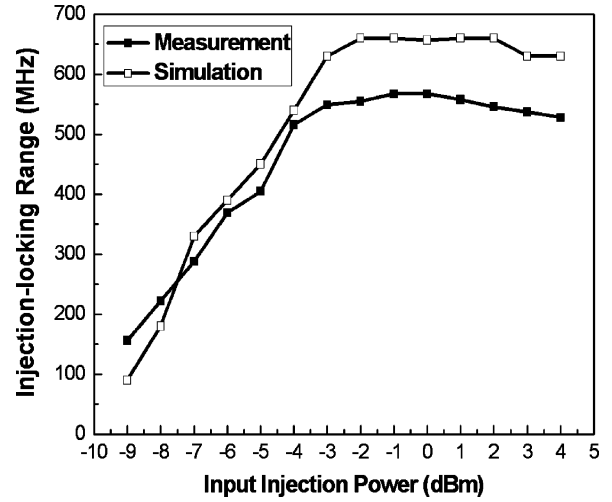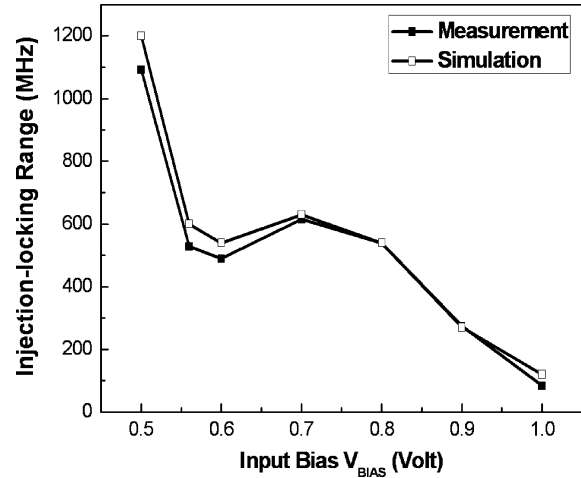ection power is small, the linear model of the ILO is valid. Thus, the injection-locking range is dominated by the nonlinear term a_3, as can be seen from (6). As the input injection signal is increased, the injection-locking range is increased due to the increase of V_i and a_3. If the input signal is increased to a moderate value, which causes the conduction angle smaller than $250°$, this leads to the large decrease of a_3, as can be seen from Fig. 4. Thus, the injection-locking range is almost saturated.

The simulated and measured injection-locking range versus the input bias voltage V_{BAIS} of M1/M2 are shown in Fig. 11. It can be seen from Fig. 11 that the injection-locking range increases with a decrease in the input bias. This result can be explained by the fact that the lower input bias allows only a small current through M3/M4. Thus, the weaker negative-resistance generated from M3/M4 reduces the effective quality factor of the LC tank. The conversion gain of the frequency pre-generator also increases because of the shift of the conduction angle into the higher third harmonic current region, as can be seen from Fig. 4.
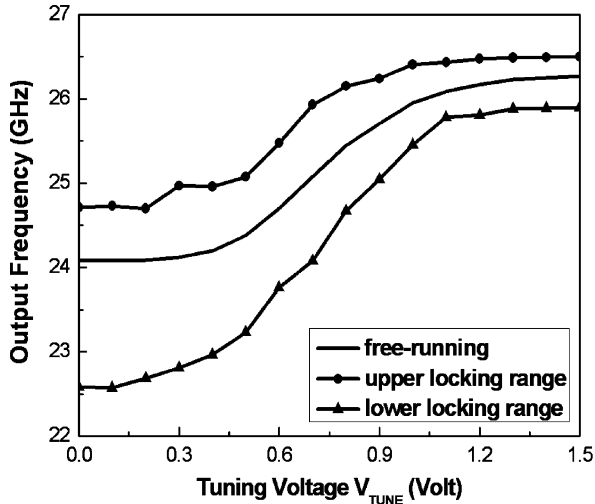
Fig. 12. Measured output frequency versus varactors bias V_{TUNE} with 0.65-V V_{BIAS} and 4-dBm input injection power for K-band ILFT.

Fig. 14. Measured phase-noise characteristics of locked output as a function of input injection power with 0.65-V V_{BIAS} for K-band ILFT.
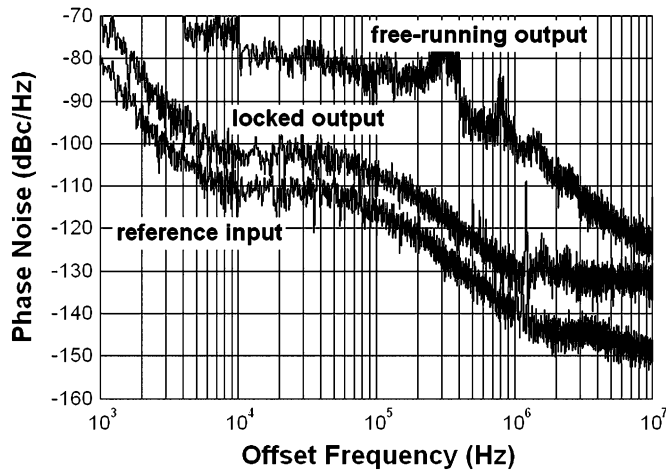

Fig. 13. Measured phase noise of reference input, free-running output, and locked output with 0.65-V V_{BIAS} and 4-dBm input injection power for K-band ILFT.

Fig. 15. Measured output power spectra of first, second, third, fourth, and fifth harmonics with 0.65-V V_{BIAS} and 4-dBm input injection power for K-band ILFT.

The varactors C1/C2 are designed in the K-band ILFT. In Fig. 12, the total output frequency under locked condition is 3915 MHz, as the varactors tuning voltage V_{TUNE} varies from 0 to 1.5 V with a dc power consumption of 2.95 mW and an input injection power of 4 dBm. Since the quality factor of the varactor decreases as the tuning voltage V_{TUNE} decreases, the extra dc power consumption is required to maintain the free-running output in the entire tuning range. In Fig. 12, the frequency range under locked condition with 1.5-V V_{TUNE} is different from that in Fig. 9 due to the different V_{BIAS} value.

The measured phase noises of the reference input, free-running output, and locked output from 1 kHz to 10 MHz is shown in Fig. 13. It shows that the phase-noise difference between the reference input and the locked output is 10.5 dB from 1 kHz to 1-MHz offset. The slightly larger output phase noise at a signal frequency higher than 1-MHz offset is due to excess noise from the internal circuit and output buffer. The measured output phase noise as a function of input injection power is shown in Fig. 14. At large input injection power levels, the measured
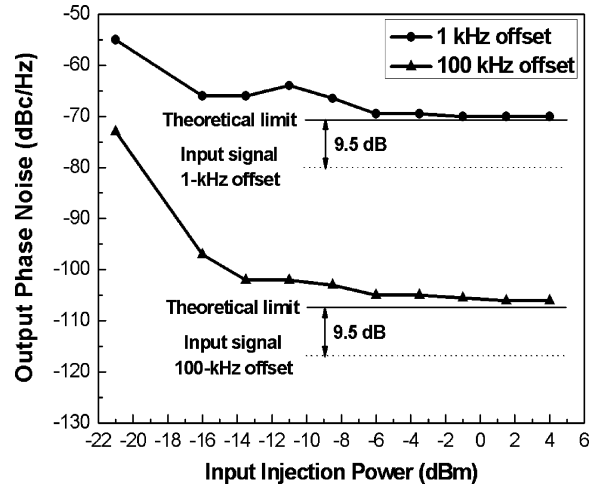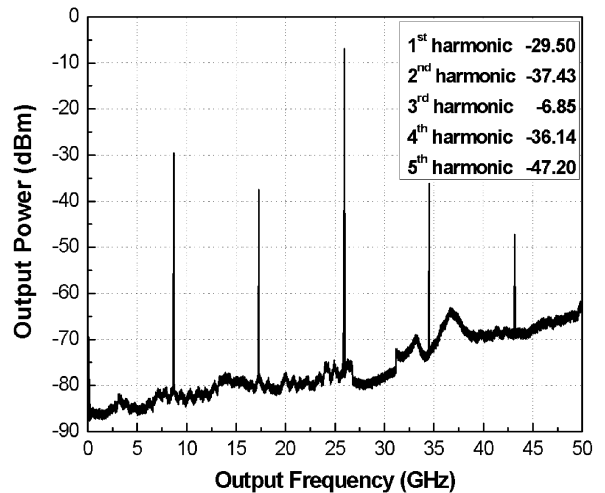
phase noise of the locked output can approach the theoretical limit of $10\log(3^2) = 9.5$ dB, as derived in Section II. The phase-noise degradation from the frequency pre-generator is 0.8 dB at 1-kHz offset and 1.5 dB at 100-kHz offset, respectively. In addition, the phase noise at small frequency offset can be close to the theoretical limit as compared to that at large frequency offset with the same input incident amplitude V_i due to the low-pass frequency response.

The measured output spectrum is shown in Fig. 15 where the HRRs compared to the desired third harmonic are 22.65, 30.58, 29.29, 40.35 dBc for the first, second, fourth, and fifth harmonics, respectively. The HRRs of even-order harmonics are 6.64 dB higher than those of odd-order harmonics because of the common-mode rejection capability of R1. In general, R1 does not affect the output performance for odd-order harmonics.

B. V-Band ILFT

The V-band ILFT starts to oscillate at a bias current of 1.55 mA from 1.2 V. The measured output spectra of the
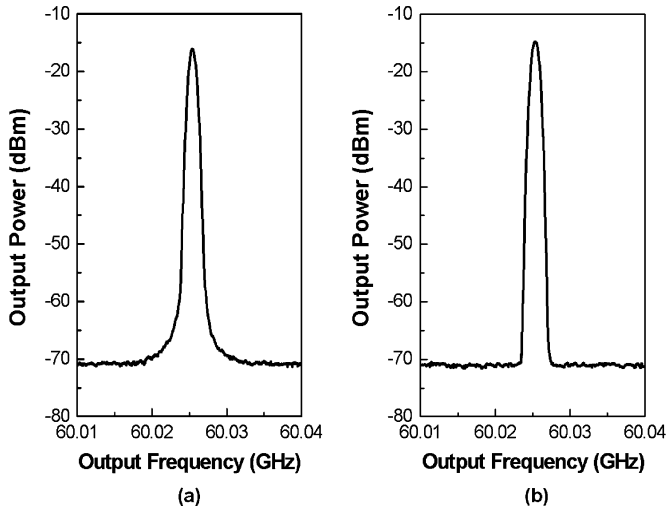
Fig. 16. Measured output spectra of the fabricated V-band ILFT under: (a) free-running and (b) locked conditions with probe and cable losses.
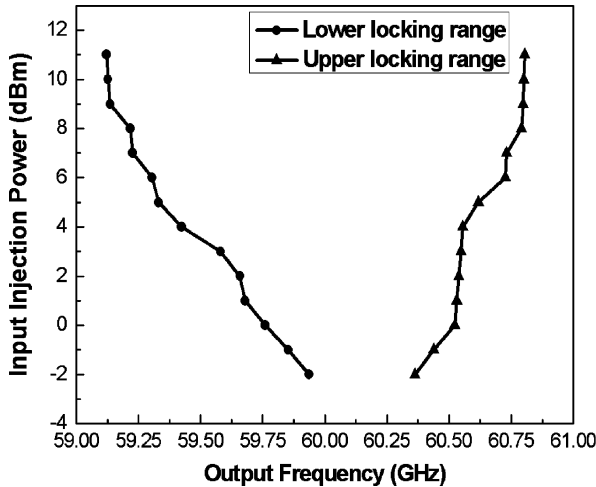

Fig. 18. Simulated and measured injection-locking range versus input injection power for V-band ILFT.

Fig. 17. Measured input injection power versus output frequency for V-band ILFT.

TABLE I
COMPARISON WITH PUBLISHED SUBHARMONIC ILFMs

Ref.	Technology	Frequency (GHz)	Subharmonic number	Locking range / input power (MHz / dBm)	Supply voltage (V)	P_{DC} (mW)
This Work	0.18-μm CMOS	26.5	3	1092 / 4	1.5	0.45
This Work	0.18-μm CMOS	26.5	3	3915ᵃ / 4	1.5	2.95
This Work	0.13-μm CMOS	60.0	3	1422 / 6	1.2	1.86
[18]	0.2-μm HEMT	20	2	200 / 10	-2	200
[18]	0.1-μm pHEMT	52	2	550 / 15	1.5	52.5
[8]	0.15-μm pHMET	60	2	120 / 9	-3	225
[18]	0.2-μm HEMT	20	3	350 / 10	-2	200
[18]	0.1-μm pHEMT	52	3	350 / 15	1.5	52.5
[17]	0.2-μm HEMT	20	4	1780ᵃ /10	-2	200
[8]	0.15-μm pHMET	60	4	30 / 9	-3	225
[9]	0.15-μm HEMT	62	4	760 / 2	N/A	N/A

a The tuning varactors are used.

V-band ILFT versus the output frequency under free-running and locked conditions with probe and cable losses are shown in Fig. 16(a) and (b), respectively. The loss from the external waveguide subharmonic mixer is deembedded by the spectrum analyzer. The measured peak output power is −16.14 dBm at 60.025 GHz under free-running condition and −14.81 dBm at 60.025 GHz under locked condition with 4-dBm input injection power, a V_{BIAS} of 0.55 V, and 9.6-dB power loss from the cable and probe. The expected output power under locked conduction is −3.1 dBm, which is a 2.1-dB difference from the measurement result.

The measured input injection power versus the output frequency when the input bias V_{BIAS} is set at 0.55 V is shown is Fig. 17. It can be seen from Fig. 18 that the injection-locking range achieves 1422 MHz with 6-dBm input injection power and 1662 MHz with 9-dBm input injection power. As the input injection power is smaller than 1 dBm, the ILO stage is linear and a_3 is nearly constant. Thus, the injection-locking range is increased with V_i. With the input injection power greater than
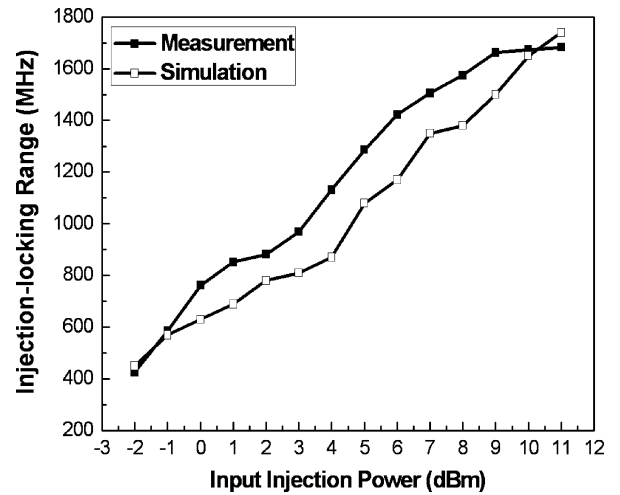
1 dBm, the injection-locking range is nearly saturated because of the large decrease of the nonlinear term a_3. If the incident signal is increased to be larger than 2 dBm, the ILO becomes nonlinear and (6) is not valid. Under this condition, the extra third-order harmonic is generated by the nonlinear ILO. Therefore, the injection-locking range is increased instead of saturated.

Due to the limitations of the instruments currently available, the log plot of phase noise and HRR cannot be measured. From the simulation results, the phase-noise difference between the reference input and the locked output is 10 dB within 1-MHz offset with 4-dBm input injection power and the HRRs are higher than 20 dBc for every undesired harmonics.

In Table I, the published non-CMOS subharmonic ILFMs worked at the K- and V-band are compared with the proposed ILFTs. It can also be seen that the proposed ILFTs, in contrast to the corresponding non-CMOS subharmonic ILFMs, can operate with a lower dc power consumption, a wider injection-locking range, and reasonable input injection power. Moreover, this design is the first CMOS ILFT in the millimeter-wave band. The published bulk-CMOS VCOs worked at the K- and V-band listed in Table II are compared with the proposed ILFTs. It can be seen that the injection-locking range of the proposed ILFT is similar to the tuning range of a bulk-CMOS VCO. The proposed

TABLE II
COMPARISON WITH PUBLISHED BULK-CMOS VCOs

Ref.	Technology	Frequency (GHz)	Tuning range (MHz)	Locking range (MHz)	Supply voltage (V)	P_{DC} (mW), P_{INJ} (dBm)	Output power (dBm)
This Work	0.18-μm CMOS	26.5	-	1092	1.5	0.45, 4	-9.4
This Work	0.18-μm CMOS	26.5	-	3915	1.5	2.95, 4	-6.85
This Work	0.13-μm CMOS	60.0	-	1422	1.2	1.86, 6	-14.81[d]
[19]	0.18-μm CMOS	19.9	510	-	1.8	32	-3.0
[20]	0.18-μm CMOS	25.1	3012[a]	-	2.2	11	-29.77
[21]	0.1-μm CMOS	25.9	600	-	1.5	24	-22.0
[22]	0.12-μm CMOS	51.6	700[b]	-	1.0	1	-30.0
[3]	0.13-μm CMOS	59.5	5800[c]	-	1.5	9.8	-10.0
[23]	0.09-μm CMOS	60.0	100	-	1.0	1.9	-30.5

a The tuning voltage is 4 V and higher than supply voltage.

b The tuning voltage is 1.5 V and higher than supply voltage.

c Two stage output buffer with on-chip inductors is used for low output loading of VCO.

d The total loss from cable and probe is 9.6 dB which is not deembedded.

ILFT can provide higher output power and lower power consumption even when the input injection power P_{INJ} is considered, as compared with the corresponding bulk-CMOS VCOs. Furthermore, it can also be seen from comparisons in Tables I and II that the proposed ILFTs offer better performance in the generation of LO signals in the millimeter-wave band.

V. CONCLUSION

A millimeter-wave CMOS subharmonic ILFT with a triple-frequency pre-generator has been proposed and analyzed. A model for the proposed ILFT has been developed to calculate both the injection-locking range and the output phase noise. Based on the model, the design guideline for the maximization of the injection-locking range and the minimization of the output phase noise has been developed. The quality factor of the LC tank and the conversion gain of the frequency pre-generator have been maximized to obtain a wider injection-locking range, higher output voltage, and lower output phase noise with low dc power consumption.

According to the developed design guidelines, both the K- and V-band CMOS ILFTs have been designed and fabricated using 0.18- and 0.13-μm technologies, respectively. As seen from the measurement results, the fabricated CMOS K-band ILFT can achieve the injection-locking range of 4.83% with 4-dBm input injection power and 0.45-mW dc power consumption. Moreover, the injection-locking range of 15.06% is performed using varactors. The fabricated V-band CMOS ILFT has an injection-locking range of 2.3% with 6-dBm input injection power and 1.86-mW dc power consumption. The measurement results have verified the performance of the proposed ILFTs.

Since it is feasible to design a high-performance VCO at low frequency without the use of full-speed frequency dividers, the proposed CMOS ILFT offers great potential application in LO signal generators for frequency synthesizers in the millimeter-wave band or even in the sub-millimeter-wave band.

APPENDIX A

By substituting (1)–(3) into (5),

$$i_{OUT} = G_m[f(v_I(t)) + v_O(t)]$$
$$= G_m[f(V_i \cos(\omega_I t + \theta)) + V_o \cos(\omega_o t)] \quad (A.1)$$

where G_m is the transconductance stage with output current i_{OUT} in the ILO; $v_I(t)$ is the incident signal with input frequency ω_I, amplitude V_i, and phase θ; and $v_O(t)$ is the output signal with frequency $\omega_O = 3\omega_I$ and amplitude V_o.

By neglecting the $O((v_I(t))^4)$ term in (4), by substituting other terms in (4) into (A.1), by assuming that any frequency not close to ω_O is filtered out by the frequency selective load $H(j\omega)$, and by rearranging the terms, (A.1) can be rewritten as

$$i_{OUT} = \text{Re}\left\{e^{j\omega_O t}\left[G_m V_o + \frac{a_3 G_m V_i^3}{4}e^{j3\theta}\right]\right\}$$
$$= |i_{OUT}| \cos(\omega_O t + g(\theta)) \quad (A.2)$$

where

$$|i_{OUT}|$$
$$= \sqrt{\left[G_m V_o + \left(\frac{a_3 G_m V_i^3}{4}\right)\cos 3\theta\right]^2 + \left[\left(\frac{a_3 G_m V_i^3}{4}\right)\sin 3\theta\right]^2} \quad (A.3)$$

$$g(\theta)$$
$$= \arctan\left\{\frac{a_3 G_m V_i^3 \sin 3\theta}{4 G_m V_o + a_3 G_m V_i^3 \cos 3\theta}\right\} \quad (A.4)$$

and a_3 is the coefficient of the cubic term in the nonlinear characteristic function of the frequency pre-generator.

The approximate transfer function of the bandpass LC-tank filter $H(j\omega)$ can be written as

$$H(j\omega) = \frac{H_0}{1 + j2Q\left(\frac{\omega - \omega_r}{\omega_r}\right)} \quad (A.5)$$

where ω_r and Q are the resonant frequency and quality factor of the LC tank, respectively. H_0 is the impedance of the LC tank at resonant frequency.

If the Barkhausen criterion is satisfied in the closed loop, the phase shift of the closed loop should be zero. Thus,

$$-\arctan\left[\frac{2Q(\omega - \omega_r)}{\omega_r}\right] + g(\theta) = 0. \quad (A.6)$$

Combing (A.4) and (A.6) gives

$$\left[\frac{2Q(\omega - \omega_r)}{\omega_r}\right] = \left\{\frac{a_3 G_m V_i^3 \sin 3\theta}{4 G_m V_o + a_3 G_m V_i^3 \cos 3\theta}\right\}. \quad (A.7)$$

By rearranging (A.7) and finding the solution for θ, the following is derived:

$$\sin(3\theta - \phi) = \frac{\frac{4V_o}{a_3 V_i^3}\left[\frac{2Q(\omega - \omega_r)}{\omega_r}\right]}{\sqrt{1 + \left[\frac{2Q(\omega - \omega_r)}{\omega_r}\right]^2}} \quad (A.8)$$

where

$$\phi = \arcsin\left\{\frac{\frac{2Q(\omega - \omega_r)}{\omega_r}}{\sqrt{1 + \left[\frac{2Q(\omega - \omega_r)}{\omega_r}\right]^2}}\right\}. \quad (A.9)$$

Since $|\sin(3\theta - \phi)| \leq 1$, (A.8) can be rewritten as

$$\frac{|\omega - \omega_r|}{\omega_r} \leq \frac{1}{2Q}\sqrt{\frac{(a_3 V_i^3)^2}{(4V_o)^2 - (a_3 V_i^3)^2}} \approx \frac{1}{2Q}\left|\frac{a_3 V_i^3}{4V_o}\right|. \tag{A.10}$$

If $4V_o >> a_3 V_i^3$, the approximation in (A.10) is valid.

The output voltage amplitude can be written as

$$V_o = |i_{\text{OUT}}||H(j\omega)|$$
$$= G_m H_0 \sqrt{\left[V_o + \left(\frac{a_3 V_i^3}{4}\right)\cos 3\theta\right]^2}. \tag{A.11}$$

By solving (A.11) and assuming $V_o + (a_3 V_i^3 \cos 3\theta / 4) > 0$, the expression of the output amplitude can be rewritten as

$$V_o = \frac{a_3 G_m H_0 V_i^3 \cos 3\theta}{4(1 - G_m H_0)}. \tag{A.12}$$

If the frequency pre-generator is removed from the ILFT, the nonlinear characteristic function is performed by the ILO. Thus, the injection-locking range can be derived as

$$\frac{|\omega - \omega_r|}{\omega_r}$$
$$\leq \frac{1}{2Q}\sqrt{\frac{(a_3 V_i^3)^2}{(4a_1 V_o + 6a_3 V_i^2 V_o + 3a_3 V_o^3)^2 - (a_3 V_i^3)^2}}$$
$$\approx \frac{1}{2Q}\left|\frac{a_3 V_i^3}{4a_1 V_o + 6a_3 V_i^2 V_o + 3a_3 V_o^3}\right|. \tag{A.13}$$

Whereas the output amplitude is represented as

$$V_o = G_m H_0 \sqrt{\left[a_1 V_o + \left(\frac{a_3 V_i^3}{4}\right)\cos 3\theta + \frac{3}{2}a_3 V_i^2 V_o + \frac{3}{4}a_3 V_o^3\right]^2}. \tag{A.14}$$

It can be seen from (A.13) that the injection-locking range can be increased by increasing $|a_3|$. In general, the value of a_3 is negative, and an $|a_3|$, which is too large, would degrade the output amplitude of the ILFT in (A.14) significantly. Obviously, if an ILFT works without the frequency pre-generator, the extra power consumption is required for both a large injection-locking range and large output amplitude.

APPENDIX B

To derive (9), the simplified noise source model of the proposed ILFT, as shown in Fig. 2, can be divided into two parts. One part is the noise calculation of the frequency pre-generator and the other is the noise analysis of the ILO. First, the noise characteristic between v_I and $v_{I,\text{ILO}3\omega}$ is considered. The phase noise spectral density $S_{\text{IN,ILO}}(\omega_m)$ at the $v_{I,\text{ILO}3\omega}$ node can be expressed as [14]

$$S_{\text{IN,ILO}}(\omega_m) = 3^2 \cdot S_{\text{INJ}}(\omega_m) + S_{\text{FPG}}(\omega_m) \tag{B.1}$$

where $S_{\text{INJ}}(\omega_m)$ and $S_{\text{FPG}}(\omega_m)$ are phase noise spectral densities of the injection signal and frequency pre-generator, respectively. ω_m is the offset frequency from output frequency ω_O.

The noise relation between $v_{I,\text{ILO}3\omega}$ and v_O can be written as [14]

$$S_{\text{OUT}}(\omega_m) = \frac{1}{1 + \left(\frac{\omega_m}{\omega_p}\right)^2}S_{\text{IN,ILO}}(\omega_m)$$
$$+ \frac{\left(\frac{\omega_m}{\omega_p}\right)^2}{1 + \left(\frac{\omega_m}{\omega_p}\right)^2}S_{\text{FreeRun}}(\omega_m) \tag{B.2}$$

where the corner frequency of the ILFT noise transfer function ω_p can be written as

$$\omega_p = \frac{\omega_r}{2Q}\frac{\eta}{1 + \eta} \tag{B.3}$$
$$\eta = \frac{A_{\text{FPG}}V_i}{V_o}. \tag{B.4}$$

In the above equations, $S_{\text{OUT}}(\omega_m)$ and $S_{\text{FreeRun}}(\omega_m)$ are phase noise spectral densities of output and internal circuits, respectively; A_{FPG} is the conversion gain of the third harmonic signal in the frequency pre-generator; ω_r and Q are the resonant frequency and the quality factor of the LC tank in the bandpass filter, respectively; H_0 is the impedance of the LC tank at resonant frequency; and V_i and V_o indicate the amplitudes of input and output, respectively.

The combination of (B.1) and (B.2) results in the following:

$$S_{\text{OUT}}(\omega_m) = \frac{3^2}{1 + \left(\frac{\omega_m}{\omega_p}\right)^2}S_{\text{INJ}}(\omega_m)$$
$$+ \frac{1}{1 + \left(\frac{\omega_m}{\omega_p}\right)^2}S_{\text{fpg}}(\omega_m)$$
$$+ \frac{\left(\frac{\omega_m}{\omega_p}\right)^2}{1 + \left(\frac{\omega_m}{\omega_p}\right)^2}S_{\text{FreeRun}}(\omega_m). \tag{B.5}$$

REFERENCES

[1] A. P. van der Wel, S. L. J. Gierkink, R. C. Frye, V. Boccuzzi, and B. Nauta, "A robust 43-GHz VCO in CMOS for OC-768 SONET applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1159–1163, Jul. 2004.

[2] F. Ellinger, T. Morf, G. Buren, C. Kromer, G. Sialm, L. Rodoni, M. Schmatz, and H. Jackel, "60 GHz VCO with wideband tuning range fabricated on VLSI SOI CMOS technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2004, pp. 1329–1332.

[3] C. Cao and K. K. O, "Millimeter-wave voltage-controlled oscillators in 0.13-μm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1297–1304, Jun. 2006.

[4] J.-C. Chiu, C.-P. Chang, M.-P. Houng, and Y.-H. Wang, "A 12-36 GHz pHEMT MMIC balanced frequency tripler," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 1, pp. 19–21, Jan. 2006.

[5] A. Boudiaf, D. Bachelet, and C. Rumelhard, "A high-efficiency and low-phase-noise 38-GHz pHEMT MMIC tripler," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 12, pp. 2546–2553, Dec. 2000.

[6] Y. Campos-Roca, L. Verweyen, M. Fernández-Barciela, E. Sánchez, M. C. Currás-Francos, W. Bronner, A. Hülsmann, and M. Schlechtweg, "An optimized 25.5–76.5 GHz pHEMT-based coplanar frequency tripler," *IEEE Microw. Guided Wave Lett.*, vol. 10, no. 6, pp. 242–244, Jun. 2000.

[7] J. F. Buckwalter, A. Babakhani, A. Komijani, and A. Hajimiri, "An integrated subharmonic coupled-oscillator scheme for a 60-GHz phased-array transmitter," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4271–4280, Dec. 2006.

[8] F.-H. Huang, C.-K. Lin, and Y.-J. Chan, "V-band GaAs pHEMT cross-coupled sub-harmonic oscillator," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 8, pp. 473–475, Aug. 2006.

[9] S. Kishimoto, K. Maruhashi, M. Ito, T. Morimoto, Y. Hamada, and K. Ohata, "A 60-GHz-band subharmonically injection locked VCO MMIC operating over wide temperature range," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2005, pp. 1689–1692.

[10] R. Adler, "A study of locking phenomena in oscillators," *Proc. IEEE*, vol. 61, no. 10, pp. 1380–1385, Oct. 1973.

[11] T. Tokumitsu, K. Kamogawa, I. Toyoda, and M. Aikawa, "A novel injection-locked oscillator MMIC with combined ultrawide-band active combiner divider and amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 42, no. 12, pp. 2572–25787, Dec. 1994.

[12] H. R. Rategh and T. H. Lee, "Superharmonic injection-locked frequency dividers," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 813–821, Jun. 1999.

[13] S. Verma, H. R. Rategh, and T. H. Lee, "A unified model for injection-locked frequency dividers," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1015–1027, Jun. 2003.

[14] X. Zhang, X. Zhou, and A. S. Daryoush, "A theoretical and experimental study of the noise behavior of subharmonically injection locked local oscillators," *IEEE Trans. Microw. Theory Tech.*, vol. 40, no. 5, pp. 895–902, May 1992.

[15] A. Mazzanti, P. Uggetti, and F. Svelto, "Analysis and design of injection-locked *LC* dividers for quadrature generation," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1425–1433, Sep. 2004.

[16] S. A. Maas, "Active frequency multipliers," in *Nonlinear Microwave and RF Circuits*, 2nd ed. Norwood, MA: Artech House, 2003, ch. 10, sec. 2, pp. 477–490.

[17] K. Kamogawa, T. Tokumitsu, and I. Toyoda, "A 20-GHz-band subharmonically injection-locked oscillator MMIC with wide locking range," *IEEE Microw. Guided Wave Lett.*, vol. 7, no. 8, pp. 233–235, Aug. 1997.

[18] K. Kamogawa, T. Tokumitsu, and M. Aikawa, "Injection-locked oscillator chain: A possible solution to millimeter-wave MMIC synthesizers," *IEEE Trans. Microw. Theory Tech.*, vol. 45, no. 9, pp. 1578–1584, Sep. 1997.

[19] H.-H. Hsieh and L.-H. Lu, "A low-phase-noise K-band CMOS VCO," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 10, pp. 552–554, Oct. 2006.

[20] D. Ozis, N. M. Neihart, and D. J. Allstot, "Differential VCO and passive frequency doubler in 0.18 μm CMOS for 24 GHz applications," in *IEEE Radio Freq. Integr. Circuits Symp. Dig.*, Jun. 2006, 4 pp.

[21] C.-M. Hung, L. Shi, and K. K. O, "A 25.9-GHz voltage-controlled oscillator fabricated in a CMOS process," in *VLSI Circuits Symp. Tech. Dig.*, Jun. 2000, pp. 100–101.

[22] M. Tiebout, H.-D. Wohlmuth, and W. Simburger, "A 1 V 51 GHz fully-integrated VCO in 0.12 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2002, pp. 300–301.

[23] D. Huang, W. Hant, N.-Y. Wang, T. W. Ku, Q. Gu, R. Wong, and M.-C. Chang, "A 60 GHz CMOS VCO using on-chip resonator with embedded artificial dielectric for size, loss, and noise reduction," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2006, pp. 1218–1227.

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