A Fully Integrated Spread-Spectrum Clock Generator by Using Direct VCO Modulation

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Abstract—A compact architecture for a fully-integrated spread-spectrum clock generator (SSCG) using voltage-controlled oscillator direct modulation is presented in this paper. A dual-path loop filter in the phase-locked loop is employed to reduce the size of the capacitance in the filter with the aid of an extra charge pump and a unity gain amplifier. At the same time, a third-charge pump which generates triangular waves is used to perform the function of a spread-spectrum. The proposed circuit has been fabricated using a 0.35-μm CMOS single-poly quadruple-metal process. The clock rate from 50 to 480 MHz with a center spread range of between 0.5% and 2% are verified and are close to the theoretical analyses. The size of the chip area is 0.82×0.8 mm^2 (including the loop filter) and the power consumption was 27.5 mW at 400 MHz.

Index Terms—Phase-locked loop (PLL), spread-spectrum clock generator (SSCG).

Fig. 1. Proposed SSCG.

I. INTRODUCTION

THE electromagnetic interference (EMI) in electronic devices such as a PC, printer, PCI Express and SATA increases rapidly as the clock speed is raised. In many applications, clock generators are one of the major contributors of EMI. Spread-spectrum clock generators (SSCG) are proven to be an efficient way to reduce EMI levels [1]–[7]. A SSCG is basically a phase-locked loop (PLL) with an appropriate frequency-modulated output. The frequency modulation is used to spread the output spectrum. There are three kinds of modulation schemes employed in PLLs. The first type involves a change to the divider made by a sigma-delta modulator [2]–[4]. The second type includes either digital manipulation of the output of a multiphase PLL or the use of a delay-locked loop (DLL)/phase interpolator combo on the output of a standard PLL [5]–[7]. The last type involves direct modulation of the voltage-controlled oscillator (VCO) in PLL [8]–[11]. The latter has the advantages of a simple circuit structure and the absence of sigma-delta modulator noise. But the loop bandwidth of a PLL has to be much less than the modulation frequency to allow the frequency variation of the VCO. In general, the required loop bandwidth is about one of ten times that in the modulation. The modulation frequency is typically around 30 to 50 kHz so that the loop bandwidth is around 3 to 5 kHz. This leads to a large capacitor of more than
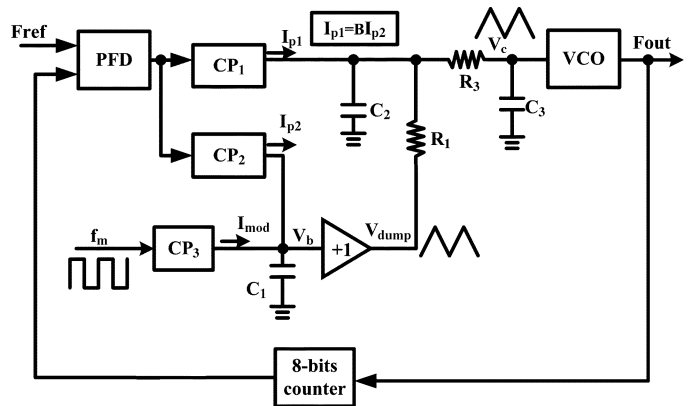
10 nF in the loop filter, which becomes too large to be integrated in the chip [8], [9].

Recently, the technique of capacitance multiplication is proposed to eradiate this problem [9], [12]–[14]. However, in order to accommodate another charge pump to generate the triangular modulation, a floating capacitor is connected [9]. The floating capacitor in a standard CMOS process can be poly-to-poly (PIP) or metal-to-metal (MIM) and needs extra masks and process steps. It also has the area and cost penalties comparable to those of a MOS capacitor. In this paper, a modified architecture with a grounded capacitor in mixed configuration containing both a dual-path loop filter (DPLF) [12] and an extra charge-pump circuit is proposed to attain a smaller size and triangular modulation. This method also reduces both hardware complexity and chip area. Although, a nonlinear modulation profile known as the "Hershey-Kiss" profile [1] shows a better EMI performance, its nonlinear equations make it more expensive due to a larger area and power consumption. Therefore, the linear triangular profile is adopted in this paper.

Section II describes the architecture and presents an analysis of the proposed SSCG. The CMOS circuits used in this work are presented in Section III and the measurement results are presented in Section IV. Finally, the conclusions are given in Section V.

II. PROPOSED SSCG AND ITS THEORETICAL ANALYSIS

A. Proposed SSCG

The proposed SSCG is shown in Fig. 1. It consists of a phase-frequency detector (PFD), a dual-path loop filter [12] which is composed of two charge pumps CP_1 and CP_2, a unity-gain buffer, two capacitors C_1 and C_2 and a resistor R_1, a charge pump CP_3, a VCO, and a 8-bits programmable counter. The

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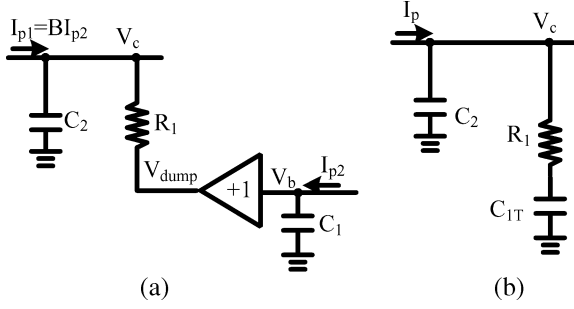
Fig. 2. (a) Dual-path loop filter. (b) Traditional loop filter.

Fig. 3. Block diagram with relevant noise sources.

CP_1 and CP_2 provide the dual-path charging currents I_{p1} and I_{p2}, respectively, to the loop capacitors. The CP_3 provides the charging current I_{mod} to the grounded capacitor C_1 in order to form the triangular waveform of the control voltage V_c. The first path composed of the R_1 and C_2 is a low-pass filter. The second path composed of the C_1 and unity gain buffer acts as an integrator. The voltages from these two paths are combined together so that a zero is created in transfer function. In order to obtain the multiplication effect of the capacitance C_1, the pumping current I_{p1} is set at $I_{p1} = BI_{p2}$ with a factor $B \gg 1$. To simplify the analysis, the higher order filtering effect of R_3 and C_3 is ignored in the following analysis. The relationship between the controlling voltage V_c and pumping current I_{p1} can be easily obtained via the dual-path loop filter redrawn in Fig. 2(a). The transfer function is given as

$$F(s) = \frac{V_c}{I_{p1}} = \frac{R_1\left(s + \frac{1}{R_1 B C_1}\right)}{s(1 + sR_1 C_2)}. \tag{1}$$

For a comparison, the conventional second-order loop filter with only one charge pump I_p is presented in Fig. 2(b), in which both the capacitor C_1 and the unity gain buffer are replaced by an equivalent capacitor C_{1T}. The corresponding transfer function is given by

$$F(s) = \frac{V_c}{I_p} = \frac{R_1\left(s + \frac{1}{R_1 C_{1T}}\right)}{s\frac{C_{1T}+C_2}{C_{1T}}\left(1 + sR_1\frac{C_{1T}C_2}{C_{1T}+C_2}\right)}. \tag{2}$$

When compared with (1), it was found that two circuits have the same zero response under the condition of $BC_1 = C_{1T}$. It implies that capacitance C_1 in the former case is B times smaller than C_{1T}. The area of capacitor C_1 can be reduced dramatically by using this technique. In this work, $B = 50$. Moreover, one of terminals in C_1 is grounded. Therefore, capacitor C_1 can be realized by using the MOS capacitor. The pole in (2) is caused from R_1 and a capacitor with C_{1T} and C_2 in series. If $C_{1T} \gg C_2$. it is almost equal to that of $R_1 C_2$ in (1), it is generally the case that the pole is about ten to hundred times the zero, depending on the damping ratio of the system.
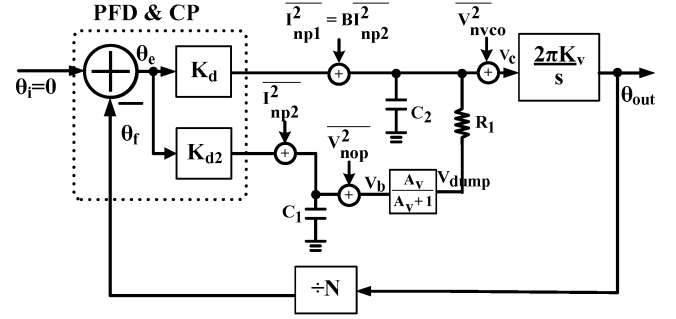
B. Analysis of Nonideality of Dual-Path Loop Filter

The nonideality of the dual-path loop filter can be viewed in two ways: filter transfer function and phase noise. The unity gain buffer is built by an opamp, which can be modeled by the dc gain A_v and the gain-bandwidth product ω_t. The transfer function of unity gain buffer can be expressed as

$$A(s) = \frac{A_v/(A_v + 1)}{1 + \frac{s}{\omega_t}} = \frac{A_{\mathrm{err}}}{1 + \frac{s}{\omega_t}} \tag{3}$$

where A_{err} denotes the gain error and is less than 1.

By using (3) and re-calculating $F(s)$, one can get

$$F(s) = \frac{R_1}{(1 + sR_1 C_2)} + \frac{1}{sBC_1(1 + sR_1 C_2)}\frac{A_{\mathrm{err}}}{1 + \frac{s}{\omega_t}}. \tag{4}$$

Equation (4) can be reduced to

$$F(s) \approx \frac{R_1\left(s + \frac{A_{\mathrm{err}}}{R_1 B C_1}\right)}{s(1 + sR_1 C_2)} \tag{5}$$

when $\omega_t \gg 1/(R_1 C_2)$. When (5) is compared to (1), it can be expected that the gain error will cause the ratio of capacitance multiplication to be higher than the expected.

With reference to phase noise analysis, the block diagram with relevant noise sources is shown in Fig. 3. Here, noises from CP_1, CP_2, the unity-gain buffer and VCO are considered and denoted as $\overline{I_{np1}^2}$, $\overline{I_{np2}^2}$, $\overline{V_{nop}^2}$, and $\overline{V_{nvco}^2}$, respectively. The unity buffer is only modeled by its gain error for the worst case scenario and the second-order loop filter is adopted for the purpose of simplification. It should be noted that all noise sources are assumed to be white although this is only an approximate for VCO.

The noise spectral density at the PLL output $S_{\Phi n}(f)$ is represented as

$$S_{\Phi n}(f) = S_{\Phi nvco}(f) + S_{\Phi np}(f) + S_{\Phi nop}(f)$$
$$= |H_{vco}|^2 \overline{V_{nvco}^2} + |H_{cp}|^2 \overline{I_{np1}^2} + |H_{op}|^2 \overline{V_{nop}^2} \tag{6}$$

where $S_{\Phi nvco}(f)$, $S_{\Phi np}(f)$, and $S_{\Phi nop}(f)$ are the noise spectral densities of VCO, both charge-pump currents, and the unity gain buffer, respectively. The definition of $\overline{V_{nvco}^2}$ can be found
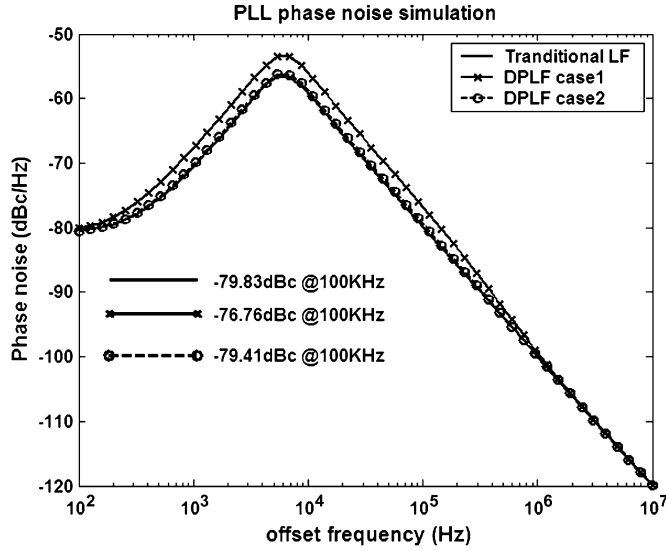
Fig. 4. Phase noise simulation results.

Fig. 5. (a) Proposed technique of triangular modulation (b) waveform of V_c and V_b.

in [17]. From the PLL linear model shown in Fig. 3, the transfer functions are calculated as follows:

$$H_{cp} = \frac{2\pi N K_v F_1(s)}{sN + 2\pi K_d F_1(s) K_v} \tag{7}$$

$$H_{op} = \frac{2\pi N K_v}{sN + 2\pi K_d F(s) K_v} \frac{A_{err}}{1 + sR_1 C_2} \tag{8}$$

$$H_{vco} = \frac{2\pi N K_v}{sN + 2\pi K_d F(s) K_v} \tag{9}$$

where K_v is the gain of the VCO in hertz/volts, $K_d = I_{p1}/2\pi$ is the gain of the PFD and CP, $F(s)$ is the transfer function of loop filter of (5), and N is value of the divider. $F_1(s)$ is the noise transfer function from CP_1 and CP_2 and can be found using

$$F_1(s) = \frac{R_1 \left(s + \frac{A_{err}}{R_1 \sqrt{B C_1}} \right)}{s(1 + sR_1 C_2)}. \tag{10}$$

From (10) it can be seen that the noise transfer function is slightly different to the signal transfer function (5). The capacitor multiplication factor in noise analysis is $\sqrt{B}$ not B. In addition, by comparing (8) and (9), the noises from the unity gain buffer and from the VCO have the same contribution when frequency is below $1/R_1 C_2$. The PLL phase noise simulation results are shown in Fig. 4, where the solid line uses the traditional loop filter presented in Fig. 2(b). The solid line with a cross mark denoted by DPLF case1 uses the dual-path loop filter seen in Fig. 2(a) with $\overline{V_{nop}^2} = \overline{V_{nvco}^2}$. Finally, the dashed line with a circle mark denote by DPLF case 2 uses the dual-path loop filter shown in Fig. 2(a) with $\overline{V_{nop}^2} = 0.1 \times \overline{V_{nvco}^2}$. Here, the VCO phase noise is assumed to be -100 dBc at 1-MHz offset frequency. From Fig. 4, it can be seen that the phase noise of solid line, solid line with a cross mark and dashed line with a circle mark at the offset frequency of 100 kHz are -79.83, -76.76, and -79.41 dBc, respectively. The phase noise is degraded by 3.07 dB at the 100-kHz offset frequency if unity
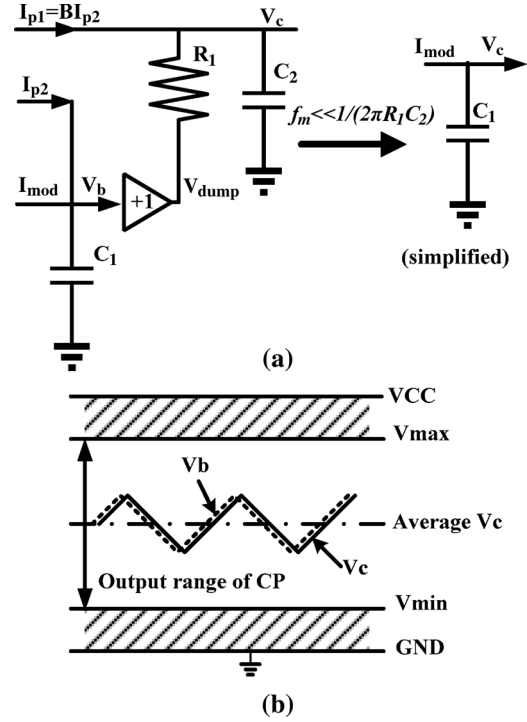
gain buffer noise is the same as the VCO noise, while the phase noise is only degraded by 0.42 dB if the unity gain buffer noise is one order less than the VCO noise. Therefore, it is necessary to design a unity gain buffer with a low phase noise.

In addition to the filter transfer function and the phase noise, the offset of opamp is also considered. If some offsets appear, they are the result of a voltage difference between V_c and V_b. But CP_2 will automatically adjust V_b to compensate for the voltage difference between V_b and V_c.

C. Analysis of Modulation

The realization of a triangular waveform for controlling voltage is illustrated in Fig. 5(a). The current I_{mod} from CP_3, which is controlled by an external pulse, is also applied to C_1. By superposition, the transfer function between I_{mod} and V_c can be expressed as

$$\frac{V_c}{I_{mod}} = \frac{1}{sC_1(1 + sR_1 C_2)}. \tag{11}$$

By assuming that the modulation frequency is much smaller than the pole, $f_m \ll 1/(2\pi R_1 C_2)$, (11) can be further simplified as

$$\frac{V_c}{I_{mod}} \approx \frac{1}{sC_1}. \tag{12}$$

Then the controlled voltage is integrated from the modulation current. The requested triangular signal at the input node of the VCO is created as a square wave I_{mod}. According to (12), the triangular voltage of modulation is easily obtained by just
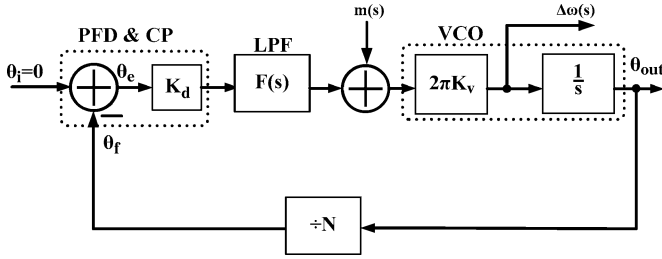
Fig. 6. Linear model of PLL with frequency modulation.

adding an extra charge-pump circuit without an additional passive component. The particular third charge pump circuit combined with the dual-path loop filter can easily generate the triangular modulation and considerably reduces the chip area. Here C_1 plays an important role that it not only acts as the loop filter in PLL as indicated in [12] but also serves the integration function in triangular wave generation. Unlike [8], the proposed model does not require the parameters C_1, C_2, R_1 and R_2 to meet the special theory requirement $R_1C_1 = R_2C_2$, nor does it require a large capacitor.

The waveforms of V_c and V_b are shown in Fig. 5(b), where V_b is the voltage at the input of the buffer and V_b is almost the equivalent of V_c with only a slightly phase leading. The output range of the charge pump is from $V_{\min}$ to $V_{\max}$ which are the ground voltage plus a saturation voltage and the supply voltage minus a saturation voltage, respectively, as shown in Fig. 5(b). This suggests that CP_3 has enough headroom to generate the triangular wave. Therefore, the output swing deduced from the three charge pumps can be safely operated without distortion. In [9] with floating capacitance, the output voltage of CP_2 seems to be equal to zero in steady state. Thus, extra bias circuit might be needed.

The choice of loop bandwidth is essential to achieve a uniform spread. The modulated behaviors in the closed loop are analyzed through the linear model as shown in Fig. 6. The modulated voltage denoted as $m(t)$ is applied to the input of the VCO. The instantaneous output frequency is $\omega_{\text{out}} = \omega_o + \Delta\omega(t)$, where ω_o is the un-modulated carrier frequency and $\Delta\omega$ is the frequency deviation. The transfer function from m(s) to $\Delta\omega(s)$ is obtained as

$$\frac{\Delta\omega(s)}{m(s)} = \frac{2\pi K_v s}{s + \frac{2\pi K_d F(s) K_v}{N}}. \tag{13}$$

From (1), $F(s)$ can be rewritten as

$$F(s) = \frac{R_1\left(s + \frac{1}{R_1 B C_1}\right)}{s} \tag{14}$$

when $f_m \ll 1/(2\pi R_1 C_2)$. By substituting (14) into (13), the following results:

$$\frac{\Delta\omega(s)}{m(s)} = \frac{2\pi K_v s^2}{s^2 + \frac{2\pi K_d K_v R_1}{N}s + \frac{2\pi K_d K_v}{N C_1 B}}. \tag{15}$$

Actually, its behavior is a high-pass characteristic. As indicated earlier, the loop bandwidth is roughly equal to $K = K_d K_v R_1 / N$ around a unity damping constant. Equation (15) can be further simplified to

$$\frac{\Delta\omega(s)}{m(s)} \approx 2\pi K_v \tag{16}$$

if the modulation frequency is much larger than the loop bandwidth. This means that the frequency deviation is proportional to the input amplitude with a coefficient of $2\pi Kv$. By definition, the feedback phase signal is θ_f

$$\theta_f(t) \equiv \int \frac{\Delta\omega(t)}{N} dt. \tag{17}$$

In a steady state, the phase error of the PFD output is $\theta_e = -\theta_f$ with the assumption that the input phase signal is $\theta_i = 0$. To satisfy the linear operation, the phase error is limited by the following relationship:

$$|\theta_e(t)| = \left| \int \frac{\Delta\omega(t)}{N} dt \right| \leq \theta_{e,\max} \tag{18}$$

where $\theta_{e,\max}$ is the limit of the linear range of the PFD. Here $\theta_{e,\max}$ equals 2π as a typical phase-frequency detector. The triangle waveform $m(t)$ with a mean of zero can be written as

$$m(t) = 2V_m(2f_m t - 0.5), \quad \text{for} \quad 0 \leq t < \frac{1}{2f_m}$$
$$= 2V_m(1.5 - 2f_m t), \quad \text{for} \quad \frac{1}{2f_m} \leq t < \frac{1}{f_m} \tag{19}$$

where V_m is the amplitude and f_m is the frequency. By substituting (19) and (16) into (17), the following is obtained:

$$V_m \leq 8\frac{N}{K_v} f_m \tag{20}$$

under the constraint of (19) with its lower limit of 0 and its upper limit of $1/(4f_m)$. It can be seen that the maximum amplitude of the triangle wave is proportional to the divider value and modulation frequency, and is inversely proportional to the VCO gain. Accordingly, the upper bond of a peak to peak spread ratio $\delta\%$ is found as

$$\delta\% = \frac{2V_m K_v}{f_o} \leq \frac{16N f_m}{f_o} \tag{21}$$

where f_o is the center frequency of the VCO output. The distortion occurs if the spread ratio exceeds this limit. The upper bond is limited by the divider value and the modulation frequency, and is independent of VCO gain.

The spread ratio can be controlled by adjusting the value of I_{mod}. According to (12) and (21), the I_{mod} can be determined by using

$$I_{\text{mod}} = \delta\%\frac{2C_1 f_m}{K_v} f_o. \tag{22}$$
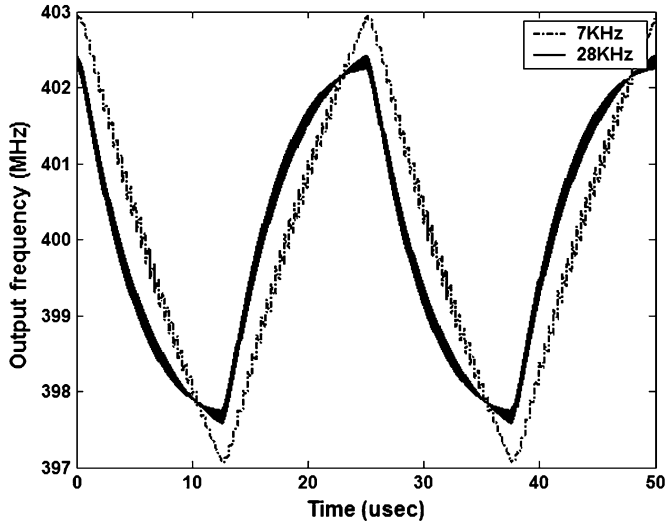
(a)
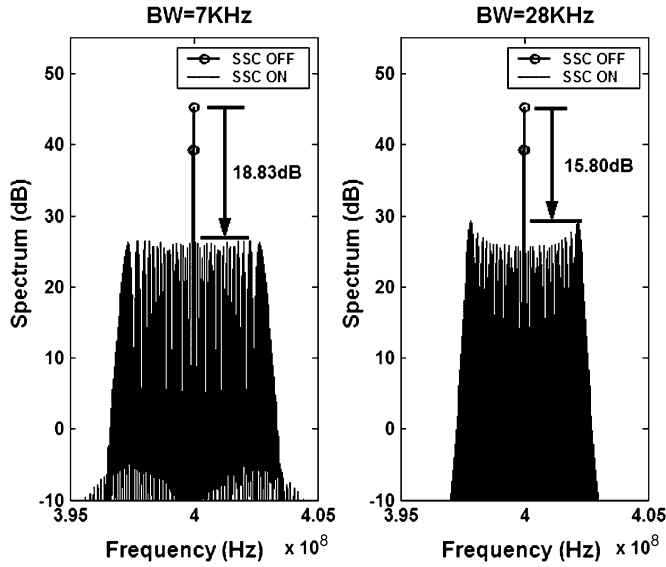
(b)

Fig. 7. Simulation results of (a) frequency profile, and (b) spectra under different loop bandwidth with $f_m = 40$ kHz.

Fig. 8. Simulation results of output frequency for different poles.

Equation (22) indicates that the variation in the spread ratio comes from the process variations of K_v, C_1 and I_{mod}. In this work, I_{mod} is about 1.05 uA for a 1.5% spread ratio with $K_v = 275$ MHz/V, $f_m = 40$ kHz, $C_1 = 600$ pF, and $f_o = 400$ MHz.

Based on condition (12), the loop bandwidth is required to be much less than the modulation in order to achieve linear integration. The effect of the loop bandwidth on the modulation profile is examined as follows. The simulated frequency deviation and suppressed spectra of a 400-MHz output signal by Matlab under different bandwidths are shown in Fig. 7(a) and (b), respectively. In Fig. 7(a), the frequency variation becomes nonlinear (solid line) and smaller as the loop bandwidth is raised toward the modulation frequency. The simulated spread ratio is 1.47% for a 7-kHz loop bandwidth, while it is reduced to 1.21% for a 28-kHz loop bandwidth with $f_m = 40$ kHz. The reason for this can be found in the fact that the PLL acts as a high-passed filter with a corner frequency at the loop bandwidth and the
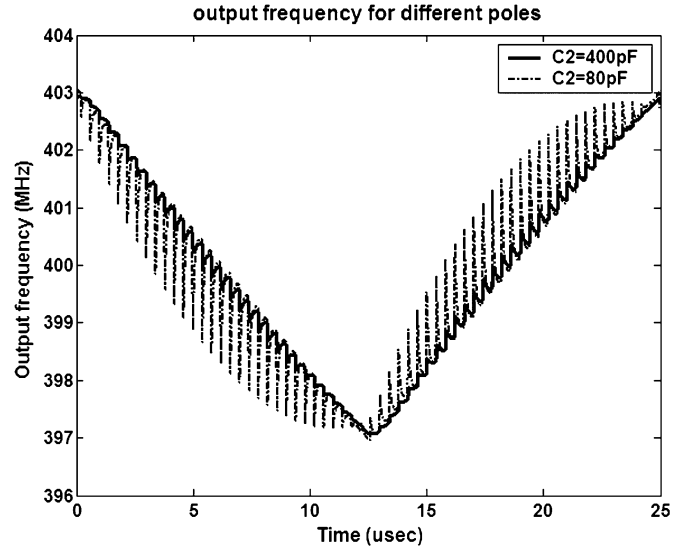
modulated signal is attenuated as the modulation frequency approaches the loop bandwidth. The EMI reductions for 7- and 28-kHz loop bandwidths are 18.83 and 15.80 dB, respectively. The spectra level for the latter is 3.03 dB worse than that for the former bandwidth. It is suggested that the loop bandwidth should be at least five times less than modulation frequency.

D. Spurious Modulation

In addition to the requirement of a loop bandwidth, the spurious effect is also taken into account. The spurious effect is mainly caused by the mismatch of the pumping currents and the switches in the charge pump circuits. As modulated in a SSCG, the phase error of the PFD output is periodically perturbed by the triangular profile. As a result of the loop bandwidth being small, the modulation signal is not cancelled. The high frequency components of the phase error may pass through the loop filter and deteriorate the jitter. This spurious modulation can be suppressed by appropriately adding a pole, i.e., $1/(R_1C_2)$. The variations in output frequency under the influence of different poles are illustrated in Fig. 8. The solid and doted lines are with 0.4- and 2-MHz poles, respectively. The corresponding values of C_2 are 400 and 80 pF which both have $R_1 = 1$ kΩ. It is clearly seen that except for the sweep, there exist instantaneous frequency spikes. The higher the frequency of the pole has, the greater the variation of the spike has. These undesired frequency spikes result in a poor triangular modulation profile and generate extra jitter. Accordingly, the pole is traded off between the linear modulation and spurious rejection. In this work, the pole is chosen as 0.4 MHz. Extra poles composed of R_3 and C_3 are employed to further lower spurious modulation. Here, $R_3 = 10$ kΩ and $C_3 = 10$ pF are adopted and the pole is 1.59 MHz.

It is noted that there are many tradeoffs in frequency setting involving direct VCO modulation. First of all, the reference clock of the PFD is chosen as the guidepost, which is the highest one in the loop and is far from the loop bandwidth. Then, the zero BR_1C_1 is traded off between capacitance area and

TABLE I
CRITICAL PARAMETERS OF PLL

Reference Frequency	2.5MHz
Zero Frequency	5.3kHz
Loop Bandwidth	7kHz
Pole frequency	398kHz
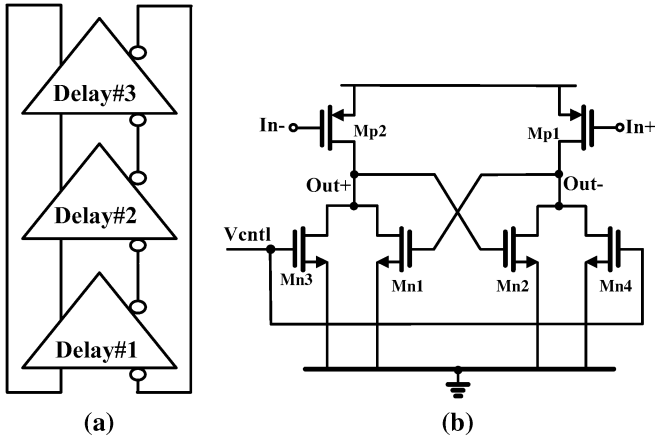
Fig. 9. (a) VCO. (b) Delay cell in VCO.
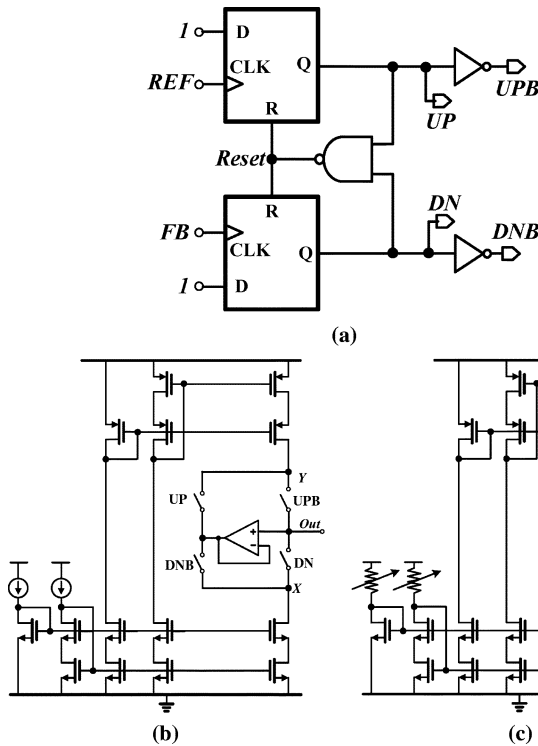
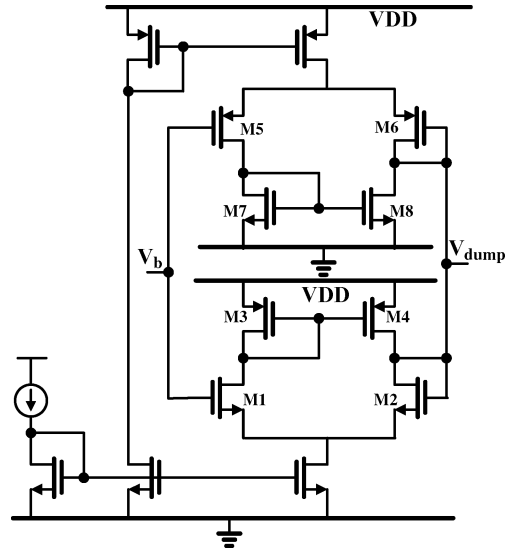Fig. 10 (a) PFD circuit. (b) CP_1 and CP_2 circuits. (c) CP_3 circuit.

Fig. 11. Unity gain buffer circuit used in dual-path loop filter.
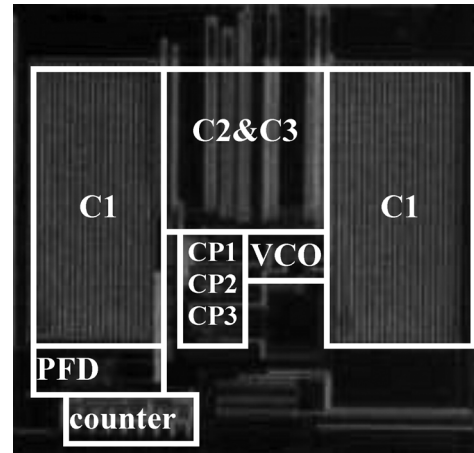
Fig. 12. Die photograph of the proposed SSCG.
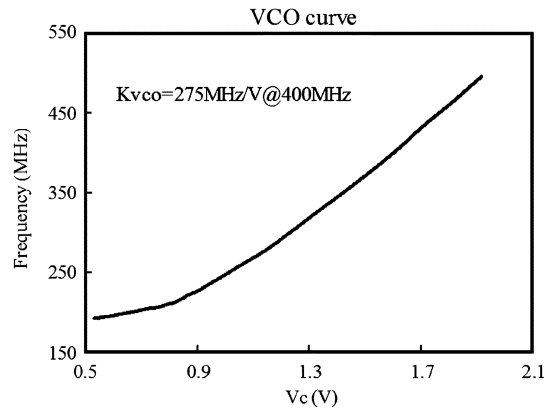
Fig. 13. Measured VCO frequency tuning curve.

damping constant. The loop bandwidth is traded off between stability and modulation. Modulation is set higher than the loop bandwidth. The pole is then traded off between linear integration and modulation spurious rejection. The critical parameters of the PLL are listed in Table I.

III. CMOS CIRCUITS

The circuits used in this work are briefly described next. The wide band VCO [15], which consists of the three stages of differential delay cells, is shown in Fig. 9(a). The schematic of each delay cell is shown in Fig. 9(b). A cross-coupled connection is
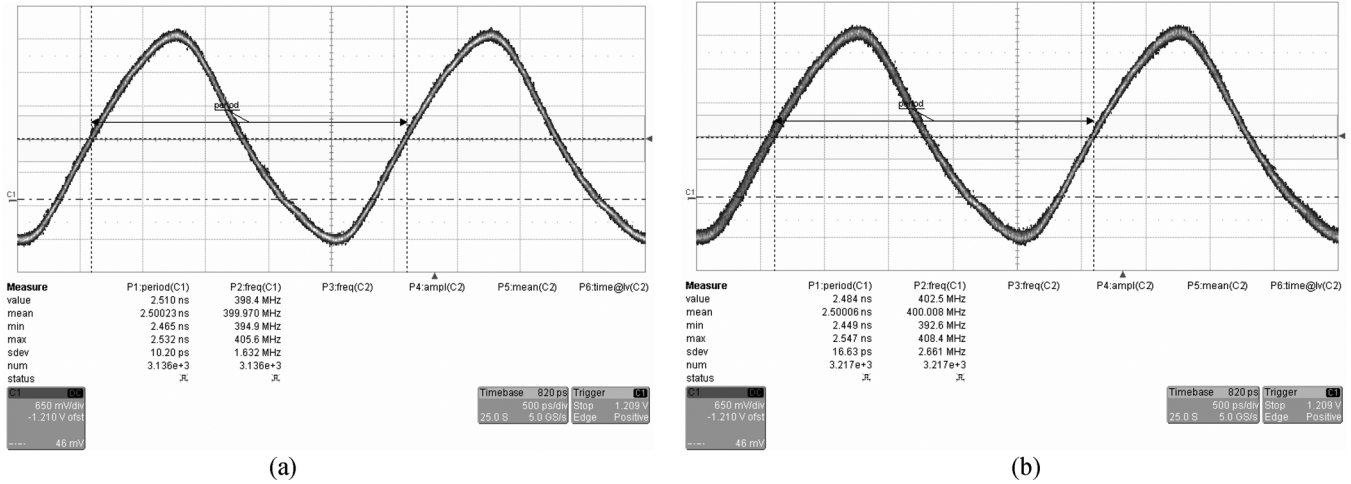
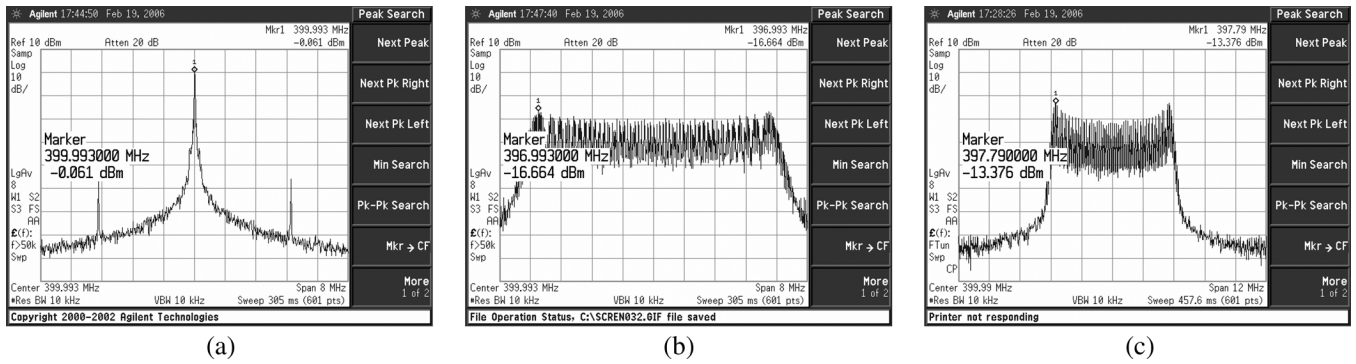Fig. 14. Measured jitter of SSCG output at 400 MHz when: (a) SSC off and (b) SSC on of 1.5% spread ratio.

Fig. 15. Measured spectra of the 400-MHz output signal: (a) without modulation, (b) with 1.5% center-spread and 7-kHz bandwidth, and (c) with center-spread 1.5% and 28-kHz bandwidth.

employed to obtain full swing and sharp output waveform to reduce the jitter. A conventional voltage to current converter and tail current source are omitted for low-voltage applications and for lower flicker noise up-conversion [15]. The PFD and charge pumps $CP_{1(2)}$ and CP_3 are shown in Fig. 10(a)–(c), respectively. The cascoded current sources with a wide-swing bias circuit in Fig. 10(b) are employed to achieve good immunity against the power supply noise. The controlling signals of UP, UPB, DN, and DNB switches are directly fed from the outputs of PFD represented in Fig. 10(a). A unity-gain buffer is used to clamp the terminal voltages of the current sources during the zero-current pumping period. In this way, voltage glitches on the loop filter resulting from charge sharing can be eliminated [16]. The currents I_{p1} and I_{p2} of CP_1 and CP_2 are 25 and 0.5 uA, respectively. The current I_{p3} is adjusted by using an external resistor to match the various spread ratios.

The unity gain buffer with rail-to-rail input and output used in the dual-path loop filter is shown in Fig. 11. The driving current is designed to be twice that of I_{p1} to provide enough driving capacity. The simple one-stage design is adopted for the low phase noise requirement discussed in part B of section II. In the mean time, the long channel devices are used for M1 through M8. The GBW is designed much larger than the poles of $1/R_3C_3$ and

$1/R_1C_2$ to maintain linear modulation. The load of the buffer comprises a resistor series with a capacitor; therefore, no driving stage is needed.

IV. MEASUREMENT RESULTS

The proposed SSCG has been fabricated using TSMC 0.35-μm single-poly quadruple-metal CMOS process. The die photograph with its area of 0.82×0.80 mm^2 is shown in Fig. 12. The tuning sensitivity of the VCO is shown in Fig. 13 with a gain of 275 MHz/V at 400-MHz output. The VCO reveals a good linear voltage to frequency transfer curve and has a maximum frequency of more than 500 MHz. The measured jitter with the SSC off and on is shown in Fig. 14(a) and (b), respectively. The peak-to-peak period jitter is 67 ps with the SSC off and 98 ps with it on, and with a 1.5% spread ratio. The measured spectra of the 400-MHz output signals without and with a center spread of 1.5% are shown in Fig. 15(a) and (b), respectively. The peak amplitude reduction is 16.603 dB, which is only 2.227 dB lower thans the simulation results, as shown in Fig. 7(b). For comparison, the measured result with the larger loop bandwidth of 28 kHz is shown in Fig. 15(c). The reduced peak amplitude is 13.315 dB, which is 3.288-dB deterioration

TABLE II
PERFORMANCE SUMMARIES AND COMPARISON WITH PREVIOUS WORKS

	[2]	[5]	[6]	[8]	[9]	[10]	This work	Unit
Modulation method	$\Sigma\Delta$	PI	PI	VCO	VCO	VCO	VCO	N/A
Modulation profile	Triangle	Triangle	Non-linear	Triangle	Triangle	Triangle	Triangle	N/A
EMI reduction	13.9	10.6	8.02	N/A	16	11.2	16.3	dB
Jitter (SSC OFF)	70	N/A	N/A	N/A	62	55.6	67	ps-pp
Jitter (SSC ON)	197	N/A	N/A	N/A	N/A	N/A	98	ps-pp
Modulation bandwidth	+0.12/ -0.12	+1.17/ -1.17	+0/ -0.50	+1.25/ -1.25	+0.75/ -0.75	+5/ -5	+0.75/ -0.75	%
Frequency	134	14.3	25	266	320	65	400	MHz
Technology	0.2	0.6	0.15	0.35	0.35	0.3	0.35	μm
Total capacitor	N/A	N/A	N/A	352.47	78.959	N/A	1.01	nF
Capacitor multiplication ratio	N/A	N/A	N/A	N/A	4	N/A	50	N/A
Power	N/A	99	N/A	300	150	N/A	27.5	mW

compared with Fig. 15(b). Thus, the effect of a higher loop bandwidth is clearly verified.

Table II summarizes the performances of the proposed SSCG and compares them with the others. The power consumption is only 27.5 mW and this is much lower than for the previous models in [8] and [9] with a similar frequency due to the benefits of full integration. The total capacitor used here $(C_1 + C_2 + C_3)$ is only 1.01 nF while it is 352.47 nF for the one in [8] and 78.959 nF for the one in [9]. Hence, the advantage of capacitor multiplication is clearly evident. The added jitter is in the proposed SSCG is only 31 ps while it is 127 ps in [2] due to the larger sigma-delta noise.

V. CONCLUSION

In this work, a new 400-MHz SSCG which adopts a direct VCO modulation is presented. By using a dual-path loop filter, the capacitance of the low-frequency loop filter is so significantly reduced such that full integration becomes possible. At the same time, a triangular modulation of spectral spread is easily obtained by the appropriate inclusion of both an extra charge-pump circuit and an isolated buffer in the loop filter. The determination of zero, loop bandwidth, modulation frequency, pole, and comparison clock are carefully studied. The chip is fabricated using a 0.35-μm standard CMOS process. The measurement results are mostly as predicted.

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