A Study of Gate-Sensing and Channel-Sensing (GSCS) Transient Analysis Method Part II: Study of the Intra-Nitride Behaviors and Reliability of SONOS-Type Devices

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***Abstract*—For the first time, we can directly investigate the charge transport and intra-nitride behaviors of SONOS-type devices by exploiting the gate-sensing and channel-sensing (GSCS) method. Our results clearly indicate that for electron injection (+FN program), the electron centroid migrates from the bottom toward the nitride center, whereas for hole injection (−FN erase), holes first recombine with the bottom electrons and then gradually move upward. For the electron de-trapping processes under $-V_G$ stressing, the trapped electrons de-trap first from the bottom portion of nitride. We also develop a method to distinguish the electron de-trapping and hole injection erasing methods by comparing the erasing current density (J) versus the bottom oxide electric field (E). At short-term high-temperature baking, the electrons move from the top portion toward the bottom portion, and this intra-nitride transport becomes more significant for a thicker nitride. On the other hand, after long-term baking, the charge loss mainly comes from the bottom portion of nitride.**

***Index Terms*—Gate-sensing and channel-sensing (GSCS), GSCS method, intra-nitride charge transport, nitride trap vertical location, SONOS.**

I. Introduction

THE MOST important difference of SONOS-type devices from the floating-gate devices is that charges are independently trapped inside the nitride, whereas charges are immediately spread out inside the floating gate. However, previous literatures [1]–[3] suggested that charges may migrate inside the nitride under high-temperature baking or internal electric field, and this contributes to reliability issues. Therefore, this "intra-nitride" transport is very important in understanding the detailed reliability physics of SONOS-type devices. However, such intra-nitride transport behavior can be only measured by indirect methods previously [1]–[3], which lacks accurate quantitative characterizations.

There are two possible mechanisms for the erase operation of SONOS. One is electron de-trapping from nitride, and the other is substrate hole injection to compensate the charge of trapped electrons. Both mechanisms result in the same V_T or $V_{\rm FB}$ decreases and cannot be easily distinguished. So far, there is no systematic method to discriminate the electron de-trapping from hole tunneling injection during erasing.

In this paper (Part II), the intra-nitride behaviors during various program/erase (P/E), cycling endurance, and reliability tests are examined extensively. Intra-nitride behaviors cannot be examined by using only the conventional channel-sensing (CS) method since the charge vertical location is not given. However, by using our gate-sensing and channel-sensing (GSCS) method, the trapped charge vertical location can be accurately calculated, and thus, it provides direct measurement about intra-nitride behaviors.

Based on our GSCS method, the evolution of electron and hole injection can be clearly measured. In addition, we propose a systematic way to identify the erase mechanism for various charge-trapping devices. The charge transport under high-temperature baking (from 150 °C to 250 °C) or medium field (< 5 MV/cm) at room temperature is also characterized.

II. Model for the Erase Mechanism

The samples used in this paper (Part II) are also illustrated in Table I of Part I. For each sample, both the CS and GS capacitors are tested under identical reliability tests, including −FN erase, $-V_G$ stress, or baking retention tests. Following the derivations of (3) and (4) in Part I, the total electron number $(Q_{\rm tot})$ and the mean vertical location $(\hat{x})$ at any given time can be calculated.

We can apply this GSCS method to study the erase mechanism. During −FN erasing or $-V_G$ stressing, the instantaneous

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erase current density (J) and the tunnel oxide electric field $(E_{\rm ox})$ can be given by

$$J = \frac{dQ(t)}{dt} \tag{1}$$

$$E_{\rm ox} = \frac{|V_{\rm gate} - V_{\rm FB,ch}|}{\rm EOT} \tag{2}$$

where $V_{\rm gate}$ is the erase voltage (negative value) applied to the gate, and EOT is the effective oxide thickness of ONO. The time differentiation in (1) can be directly calculated from the experimental data. Equation (2) is valid for any arbitrary charge distribution, and the detailed derivation is shown in Appendix A.

J–E curve is directly related to a certain physical mechanism. For example, if the erase mechanism comes from the hole tunneling, then the J–E curves should follow a tunneling equation, where J is only a function of tunnel oxide electric field and is independent of the trapped charge density or trap energy profile. Various J–E curves can be obtained by using different erase voltages or different initial $V_{\rm FB}$. Since J depends only on the electric field, various J–E curves should follow the same curve and merge together for different erase conditions.

On the other hand, if the erase mechanism comes from the electron de-trapping, then de-trapping current J depends not only on the electric field but also on the trapped energy spectrum and the trap vertical location. Then, the J–E curves from different erase conditions do not follow the same curve.

Therefore, the comparison of J–E curves from different erase conditions provides a systematic way to identify the erase mechanism for various charge-trapping devices.

III. Charge Transport During ±FN Injection

A. SONOS With a Thicker Bottom Oxide (+FN With Electron Injection and −FN With Electron Detrapping)

Fig. 1(a) and (b) show the +FN programming (electron injection) and $-V_G$ stressing (electron detrapping) characteristics, respectively, of sample S1 with O1/N/O2 = 54/70/90 Å. Since the bottom oxide is thick and thus the hole injection from Si substrate can be completely blocked, we expect that the major erase mechanism is electron de-trapping [4], [5]. Electron de-trapping speed is often very slow. Although a higher erase voltage may accelerate the de-trapping speed, however, gate electron injection also takes place under high field [6]. We must therefore decrease the ease voltage to below −14 V to avoid gate injection. Moreover, a very long time (1000 s) is used to get a sufficient $V_{\rm FB}$ shift.

The extracted x–Q plots are shown in Fig. 1(c) and (d). For the +FN programming, the electron centroid starts from the bottom nitride interface and then migrates toward the center of nitride, as illustrated in Part I. Next, the $-V_G$ stressing can expel (de-trap) some electrons and decrease $V_{\rm FB}$. The corresponding x–Q plot shows that as Q (electron number) is decreased, the mean vertical location is also shifted higher.

Fig. 1(d) is consistent with the simple intuitive model where electron detrapping happens first from the bottom portion of nitride, since out-tunneling is the easiest. After longer

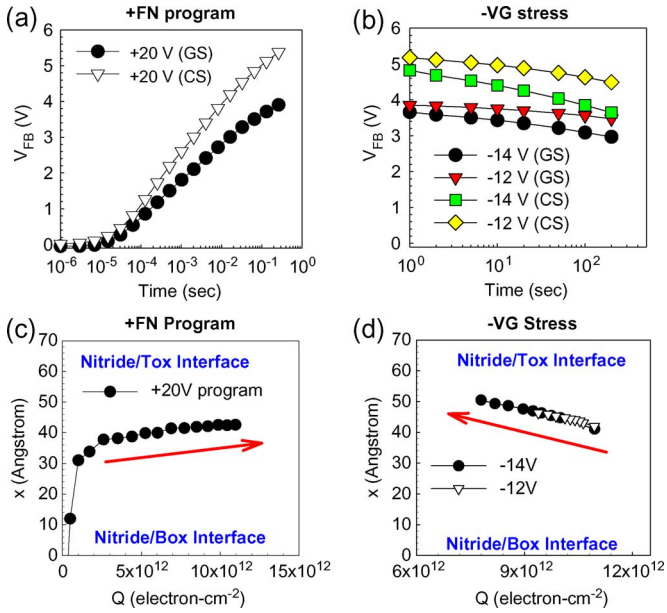

Fig. 1. (a) $V_{\rm FB}$ shifts of programming by +20 V. (b) $V_{\rm FB}$ shifts of erasing by $-V_G$ stressing. (c) Calculated Q–x plots for the +FN program. (d) Calculated Q–x plots for $-V_G$ stress. Sample S1 (O1/N/O2 = 54/70/90) is measured. For electron injection (+FN), the electron centroid gradually migrates toward the center of nitride. After $-V_G$ stressing, the electron density decreases, whereas the electron centroid moves upward. It indicates that electrons mainly de-trap from the bottom portion of nitride.

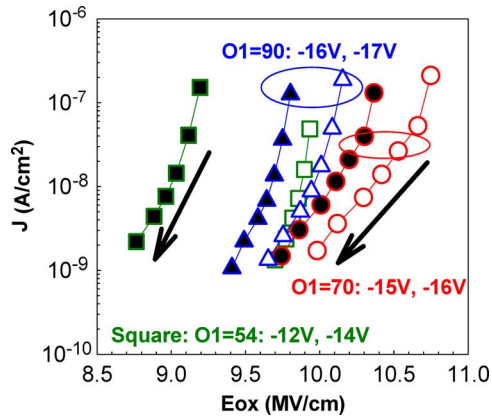

Fig. 2. J versus $E_{\rm ox}$ plots of S1 (O1 = 54 Å), S7 (O1 = 70 Å), and S8 (O1 = 90 Å). Plots with different erase voltages diverge. This indicates a complex, but not pure, tunneling process. Electron detrapping contributes heavily to charge loss for these samples.

$-V_G$ stressing, the mean vertical location moves up near the nitride/top oxide interface, indicating that most of the bottom portion electrons have been expelled.

We can use (1) and (2) to plot the erase current density (J) versus the bottom oxide electric field of S1, S7, and S8, as shown in Fig. 2. It shows that the J–E curves of electron de-trapping are very diverse and scattered with various applied voltages and different bottom oxide thickness. This suggests that electron detrapping is not just a function of the bottom oxide electric field. This can be understood considering that the electron detrapping is not an external injection and that it depends on the electron trapping energy as well as the trap vertical location. The $-V_G$ stressing not only expels the electrons but also changes the trapping energy spectrum [4], [5]

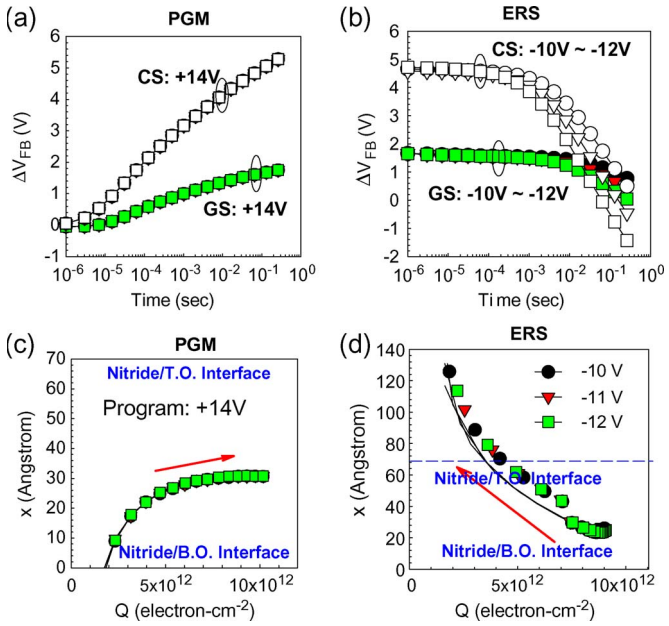

Fig. 3. (a) Programming and (b) erasing characteristics of SONOS device using ultra-thin tunnel oxide (sample S14, with ONO = 20/70/90 Å). The calculated $x-Q$ plots for +FN programming and −FN erasing are shown in (c) and (d), respectively.

and vertical distribution. After longer $-V_G$ stressing, most of the bottom electrons or shallowly trapped electrons are already expelled, leading to the decreased de-trapping current. Therefore, the de-trapping current density (J) at longer erase time is always smaller than that of the as-programmed cell, even at the same electric field. In other words, J depends not only on the instantaneous electric field but also on the history during erasing. It therefore leads to diverse J–E curves for various erase conditions.

B. SONOS With a Thin Bottom Oxide (+FN With Electron Injection and −FN With Hole Injection)

For comparison, we fabricate SONOS with a thin tunnel oxide (S14) to offer an efficient hole direct tunneling erase. The programming/erasing characteristics and the extracted $x-Q$ plots are shown in Fig. 3. Since direct tunneling injection using an ultra-thin tunnel oxide offers much more efficient erase speed, the erase time can be much smaller ($<$ 1 s) than that of S1. After +FN programming, the electron centroid also shows similar behavior as that for [Fig. 1(c)]. During −FN erasing, the mean vertical location of total net charges moves upward. Although the $x-Q$ plot in Fig. 3(d) is similar to Fig. 1(d), the detailed erase mechanisms are different. Fig. 3(d) is consistent with the model where the injected holes first recombine with the trapped electrons in the bottom portion of nitride and then gradually move upward, thus causing the upward motion of the charge centroid. Moreover, the mean vertical location moves even above and out of nitride after longer −FN erasing time.

Again, the above nitride mean vertical location does not mean that the charges are inside the top oxide. This is because both holes and electrons exist inside the nitride, which is similar to Section IV in Part I. At longer erasing time, more injected holes are accumulated at the bottom portion of nitride, whereas some electrons still remain in the top portion of nitride. Simple arithmetic verifies that it is possible to have the net charge centroid above the nitride (for example, $Q_e = +3 \times 10^{12}$ at 3/4 T_N, and $Q_h = -2 \times 10^{12}$ at 1/4 T_N, and then, $Q_{\rm tot} = +1 \times 10^{12}$ (electron), and x = 7/4 T_N: out of nitride).

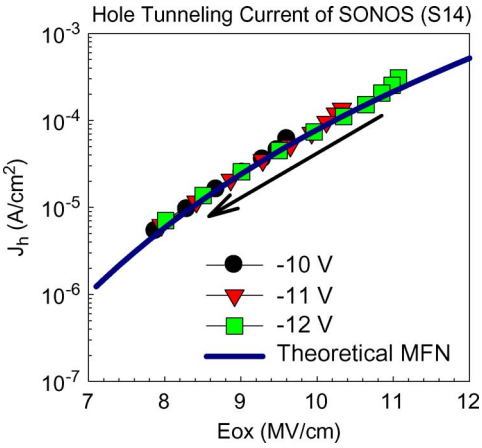

Fig. 4. J versus $E_{\rm ox}$ plots of S14 (SONOS, ONO = 20/70/90 Å). Plots with different erase voltages converge perfectly. This indicates that J is only a function of the tunnel oxide electric field.

We can extract the erase current density using (1) and (2), and the results are shown in Fig. 4. Contrary to Fig. 2, the J–E curves are very consistent under various bias voltages. It indicates that the erase current density comes from a tunneling mechanism, which mainly depends on the bottom oxide electric field.

In order to validate this point, we adopt a modified hole direct tunneling equation [7] to model the erase current. The detailed equations are listed in Appendix B. This model considers the modified FN equation through an ON double layer. Fig. 4 shows that the fitting result is generally quite consistent with the experimental result. Moreover, the fitting parameters are generally consistent with the published results [7]. This suggests that the erase mechanism of such SONOS (S14) is indeed well explained by the hole tunneling mechanism.

The J–E curves from various erasing conditions provide a way to systematically study the erase mechanism for charge-trapping devices. It is clear from Figs. 2 and 4 that the hole tunneling injection (S14) is indeed much more efficient than the electron detrapping (S1, S7, and S8). Moreover, hole tunneling shows consistent J–E curves for various voltages since hole tunneling current is only a function of the bottom oxide electric field and is independent of the electron trapping energy or the vertical location. On the other hand, electron detrapping is very slow, and the J–E curves are very scattered and cannot be explained by a consistent physical model.

It should be mentioned that great care must be taken during the measurement of S14 with such a thin tunnel oxide (20 Å) to avoid gate disturb during C–V measurement. Gate disturb easily happens even at a low voltage since direct tunneling from substrate is induced even at a low field. Gate disturb is another reason why SONOS with a thin bottom oxide has very poor reliability and is unsuitable for most practical applications.

In order to minimize the gate disturb, we limit the V_G sweeping range to be only $V_{\rm FB} \pm 1$ V during the C–V

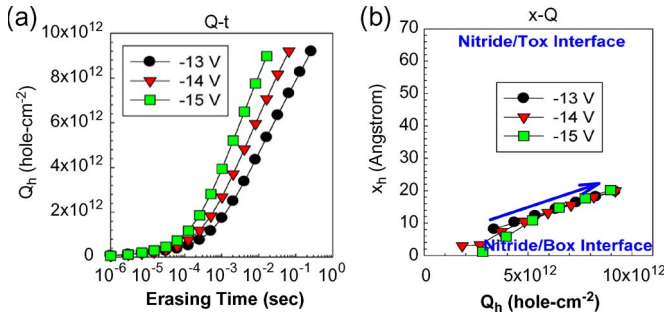

Fig. 5. (a) Q_h-t and (b) x_h-Q_h plots of sample S13 during $-$FN by using (A17) and (A18). Hole centroid also starts at the bottom interface. After longer injection, it gradually migrates upward. However, the centroid is much lower than the electrons.

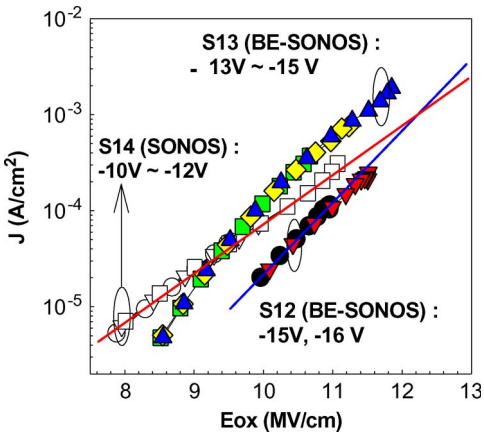

Fig. 6. Comparison of J versus $E_{\rm ox}$ curves for S12, S13, and S14. The J of BE-SONOS is larger than that of SONOS at high electric field but smaller at lower electric field.

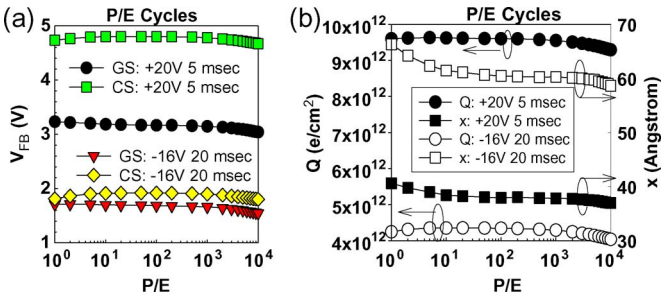

Fig. 7. (a) 10K P/E cycling endurance of BE-SONOS (S12). (b) Extracted Q and x during the P/E endurance testing.

measurement. During testing, the V_G-sweeping range automatically changes when $V_{\rm FB}$ is shifted during programming/erasing. This minimizes the tunnel oxide electric field during measurement, hence suppressing the gate disturb. We also apply the same measurement methods for the SNS, SONS, and SNOS devices in Part I.

C. BE-SONOS With an Ultra-Thin ONO Barrier ($+$FN With Electron Injection and $-$FN With Hole Injection)

We also measure the erasing characteristics of BE-SONOS (S13). The ultra-thin ONO barrier in BE-SONOS [8] offers efficient hole tunneling erase at high electric field while eliminating the direct tunneling leakage at low electric field. In order to further understand the hole injection profile, we plot the hole centroid during injection. The mathematical formulation is simple. We assume that the electrons are fixed during $-$FN erasing, we can subtract the contribution from the as-programmed condition, and we can transform $V_{\rm FB,ch}$ and $V_{\rm FB,pl}$ into the hole charge density (Q_h) and the hole mean vertical location (x_h). The detailed derivation of Q_h and x_h is shown in Appendix C. The calculated results are shown in Fig. 5. Similar to the electron injection, hole centroid also starts at the bottom interface and then migrates upward. For different erase voltages, the x_h-Q_h curves are merged together, which suggests that the x_h-Q_h plot describes the trajectory of hole injection. Compared with Fig. 4(c) in Part I, the hole centroid ($\sim$20 Å) is considerably lower than the electron centroid ($\sim$35 Å). Thus, after $-$FN erasing, the hole and electron centroids are still unmatched.

The erase current densities of BE-SONOS (S12 and S13) and SONOS (S14) are compared in Fig. 6. The J–E curves are consistent with various bias voltages. It suggests that BE-SONOS is erased by the same hole tunneling injection just like SONOS with a thin bottom oxide.

We have found that the erase speed of BE-SONOS is very sensitive to the first bottom oxide (O1) in the ONO barrier [8]. In comparing S13 (ONO = 13/20/25 Å) with S12 (ONO = 15/20/25 Å), S13 has much larger hole injection current than S12 due to thinner O1. Moreover, compared with SONOS with 20-Å tunnel oxide (S14), BE-SONOS shows a faster erase speed than SONOS at higher electric field. On the other hand, at lower electric field, BE-SONOS has lower hole current density, leading to the suppressed leakage current. Therefore, BE-SONOS can provide high erase speed as well as good data retention according to the J–E curves. Moreover, the gate disturb during measurement does not occur.

Since there is a strong electron and hole vertical mismatch during $-$FN erasing, we investigate the impact on the P/E cycling endurance. Fig. 7(a) shows the example of 10K P/E cycling tests of BE-SONOS device (S12). BE-SONOS shows excellent cycling endurance. The corresponding x and Q are calculated in Fig. 7(b). After $+$FN programming, the total net charge Q (electrons) is increased, and the mean vertical location x is close to the nitride center. After $-$FN hole injection, the total net charge Q (still more electrons since $Q>0$) decreases, and the mean vertical location x shifts higher. Moreover, at the initial few P/E cycles, the Q and the x are slightly varied after P/E cycling but then soon become very stable after many P/E cyclings.

Note that the mismatch in the vertical location of electrons and holes during programming and erasing reflects a simple (although not completely understood) phenomenon that holes do not travel as far as electrons in the nitride. Thus, this mismatch in electron and hole centroids should not be interpreted as accumulation of electrons in the upper portion and holes in the lower portion of the nitride, respectively. During the P/E cycling, most residual electrons/holes are neutralized by the programming or erasing electrons/holes. This well explains our observation that Q and x stay unchanged through many P/E cyclings. For example, after the $(n-1)$th erasing, there is a

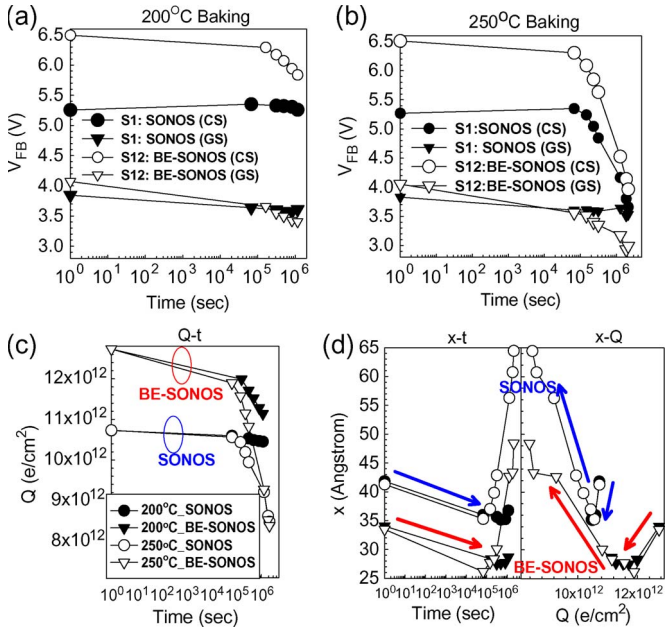

Fig. 8. S1 (SONOS) and S12 (BE-SONOS) baking retention of (a) 200 °C and (b) 250 °C, respectively. The devices are first programmed by +20 V 0.26 s. (c) $Q-t$ and (d) $x-t/x-Q$ plots during high-temperature baking. x first moves lower within one-day baking and then shifts upward after longer time baking. The $x-Q$ plots for different baking temperatures are similar.

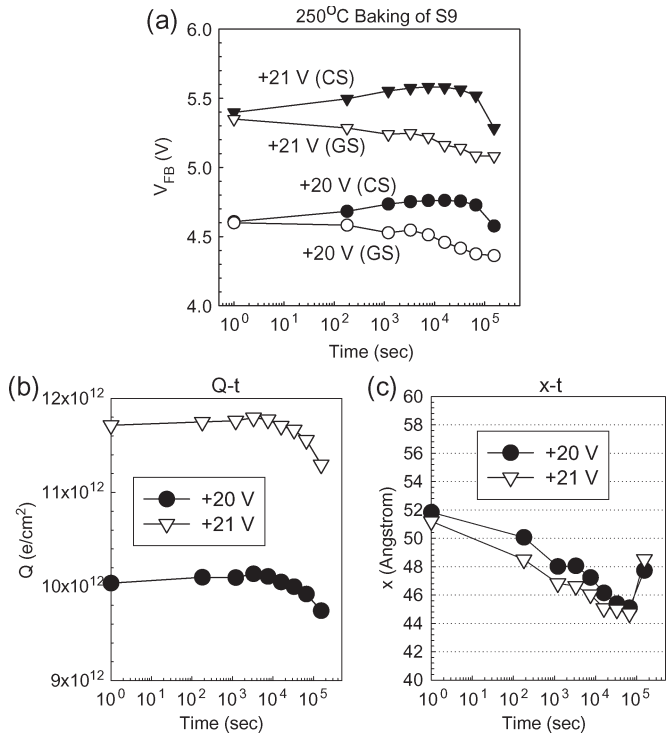

Fig. 9. (a) S9 (ONO = 70/95/75 Å) baking retention of 250 °C. The devices are programmed by +20 V 0.26 s or +21 V 0.26 s before baking. Within one-day baking, the CS device shows obvious $V_{\rm FB}$ gain, whereas the GS device shows $V_{\rm FB}$ loss. (b) $Q-t$ and (c) $x-t$ plots of sample S9 during 250-°C baking. During one-day baking, Q is almost unchanged, whereas x is significantly decreased. This indicates that the electron moves from the top portion toward the bottom portion.

significant population of electrons in the upper portion of the nitride and a population of holes in the lower portion of nitride, and the total charge (Q) is low. During the nth programming, most of the holes are neutralized, and the electron distribution is the same as that after the $(n-1)$th programming. Similarly, the hole distribution after the nth erasing is the same as that after the $(n-1)$th.

Therefore, the mismatch of the electron and hole centroids should be viewed as snapshots of programmed and erased states, respectively, and should not be interpreted as two separate pockets of charges co-inhabiting the nitride.

IV. Charge Transport During High-Temperature Baking

A. SONOS and BE-SONOS

The 200-°C and 250-°C baking characteristics of S1 (SONOS) and S12 (BE-SONOS) are shown in Fig. 8(a) and (b), respectively. The devices are first programmed by +20 V 0.26 s before high-temperature baking. For S1 (SONOS), the CS capacitor shows a slight $V_{\rm FB}$ gain, whereas the GS capacitor shows a slight $V_{\rm FB}$ loss within one-day baking. The extracted (Q, x) are shown in Fig. 8(c) and (d). For SONOS, there is almost no real charge loss after baking for approximately one day (Q is unchanged), but there is a significant decrease in the charge centroid (x). Therefore, the $V_{\rm FB}$ shift must be caused by trapped electrons that are moved to the lower portion of nitride. This is an evidence of intra-nitride transport. However, after long-term baking, significant real charge loss is observed (Q is decreased) while x shifts higher. This indicates that electrons mainly de-trap from the bottom portions of nitride after long-term baking. Since the bottom oxide of S1 is thick enough to block the trap to band tunneling and the charge loss increases with temperature, we expect that the charge loss mainly comes from thermal emission [9], [10]. The higher the baking temperature, the more significant the charge loss and the x shift. BE-SONOS also shows similar behavior as SONOS. However, in the first day of baking, we observed both intra-nitride transport and charge loss simultaneously. This may be due to the fact that BE-SONOS has more starting stored charges that cause larger built-in electric field in the tunnel barrier, leading to more real charge loss.

It is interesting to note that the $x-Q$ plots in Fig. 8(d) are very similar for different baking temperatures. It can be explained that the higher temperature increases the overall electron detrapping rate, but the ratio between the bottom and top portions of nitride is independent of temperature. In other words, the "x-dependence" of de-trapping rates is the same at different baking temperatures. It therefore leads to similar $x-Q$ plots at different baking temperatures.

B. SONOS With a Thicker Nitride

In order to enhance the signal of intra-nitride transport, we have investigated the baking characteristics (250 °C) of SONOS with a thicker nitride (S9, O/N/O = 70/95/75 Å), as shown in Fig. 9(a). Within one-day baking, CS shows obvious $V_{\rm FB}$ gain, whereas GS shows $V_{\rm FB}$ loss. This opposite shift of CS and GS clearly implies that there is intra-nitride transport inside nitride.

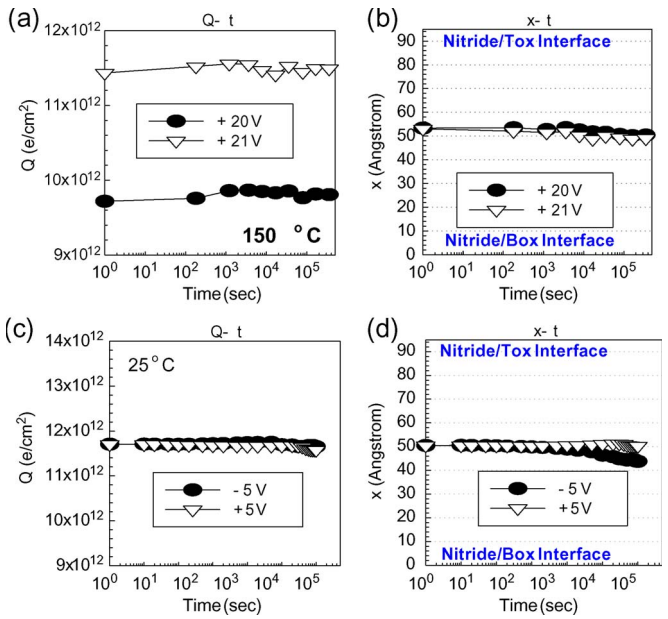

Fig. 10. (a) $Q-t$ and (b) $x-t$ plots of sample S9 during 150-°C baking. The amount of change in x is much smaller than that in Fig. 9. The devices are programmed by +20 V 0.26 s or +21 V 0.26 s before baking. (c) $Q-t$ and (d) $x-t$ plots of S9 during ±5-V gate stressing at 25 °C. The Q and the x are very steady at room temperature.

The extracted Q and x are shown in Fig. 9(b) and (c). Q is almost unchanged at $t < 10^4$ s, whereas x is significantly decreased. This implies that the total charge inside nitride is unchanged, but the trapped electrons move to the lower portion of nitride, i.e., the intra-nitride transport. The thicker nitride shows a slightly more significant change in x compared with the thinner nitride. The exact mechanism still needs to be examined.

It should be mentioned that the intra-nitride transport is observable only at very high-temperature baking (> 200 °C). At lower baking temperature (150 °C), the intra-nitride transport behavior is very minor, as shown in Fig. 10(a) and (b).

We also investigated the room-temperature intra-nitride transport under low bias voltage (±5 V) and long-time (1×10^5 s) stressing. We first program the devices to high $V_{\rm FB}$ states (+21 V, 0.26 s) and then apply ±5-V stress. The extracted Q and x are shown in Fig. 10(c) and (d). The results show that under +5-V stressing ($<$ 5 MV/cm in O1), the Q and the x are almost unchanged within 1×10^5 s. Moreover, under −5-V stressing ($>$ 5 MV/cm in O1), the x is slightly decreased after 1×10^3 s stressing, indicating that the charges inside nitride are very stable. Therefore, we conclude that the charge spreading inside nitride is not the dominant retention mechanism for SONOS-type devices at lower baking temperature ($<$ 150 °C) or under moderate internal electric field. Hence, nitride trap provides a very reliable charge storage material for non-volatile memory applications.

V. Summary

In this paper, we can directly investigate the charge transport and intra-nitride behaviors of SONOS-type devices by using the GSCS method. By using this novel method, we can monitor the charge centroid ($\hat{x}$) and the charge density (Q) during various P/E and reliability tests. Based on the Q and the $\hat{x}$, we can plot the erase current density (J) as a function of the bottom oxide electric field (E) during erasing and then identify the erase mechanism for various charge-trapping devices.

Our results clearly indicate that for the electron injection (+FN program), the electron centroid migrates from the bottom toward the nitride center. For the hole injection (−FN erase) in SONOS with a thin bottom oxide or BE-SONOS, holes first recombine with the bottom electrons and then gradually move upward. The J–E curves at different erasing conditions are consistent, and they almost follow the theoretical hole tunneling equation. We also prove that the electron and hole injection centroids have vertical mismatch. However, the mismatch of the electron and hole centroids should be viewed as snapshots of programmed and erased states, respectively, and should not be interpreted as segregated accumulation of electrons and holes. During the P/E cycling, most residual electrons/holes are neutralized by the programming or erasing electrons/holes. Therefore, SONOS-type devices can still possess excellent P/E cycling endurance.

On the other hand, for the electron de-trapping processes under $-V_G$ stressing (SONOS with a thicker bottom oxide), the trapped electrons de-trap first from the bottom portion of nitride, and their J–E curves are scattered for various erase conditions and bottom oxide thickness.

For the high-temperature retention, after short-term baking, the trapped electrons move to the lower portion of nitride, and this intra-nitride transport becomes more significant for a thicker nitride. On the other hand, after long-term baking, the charge loss mainly comes from the bottom portion of nitride.

It should be mentioned that the intra-nitride transport is significant only at very high-temperature baking (> 200 °C). The charge vertical or lateral spreading may not be the dominant retention mechanism at lower storage temperature.

In summary, this paper provides numerous observations of the intra-nitride charge-trapping behavior as well as crucial understanding of the nitride-trapping behavior.

Appendix A
Detailed Derivation of (2) for an Arbitrary Charge Distribution

We want to solve the bottom oxide electric field with an arbitrary charge distribution in nitride and an applied gate voltage. Since Poisson's equation is a linear equation, we can separately calculate the electric field contributed by each component using the principle of linear superposition. For example, we can first calculate the bottom oxide electric field induced by a sheet charge density Q located at x (without external voltage). The result is easily derived from Gauss' law

$$E = \frac{Q\left(x\varepsilon_{\rm ox} - T_N\varepsilon_{\rm ox} - T_{\rm Tox}\varepsilon_N\right)}{\varepsilon_0\varepsilon_{\rm ox}\left(T_{\rm Box}\varepsilon_N + T_N\varepsilon_{\rm ox} + T_{\rm Tox}\varepsilon_N\right)} \tag{A1}$$

where the E field is positive for the direction toward the gate, and Q is positive for the electron in our definitions. On the other

hand, the applied voltage also contributes to the electric field, which is simply given by

$$E = \frac{V_G}{\text{EOT}}. \tag{A2}$$

Based on the principle of superposition, the electric field can be calculated by the summation of electric field by each sheet charge density and the external voltage, which is given by

$$E = \int_0^{T_N} \frac{Q(x)(x\varepsilon_{\text{ox}} - T_N\varepsilon_{\text{ox}} - T_{\text{Tox}}\varepsilon_N)}{\varepsilon_0\varepsilon_{\text{ox}}(T_{\text{Box}}\varepsilon_N + T_N\varepsilon_{\text{ox}} + T_{\text{Tox}}\varepsilon_N)}dx + \frac{V_G}{\text{EOT}}. \tag{A3}$$

Define the mean value of charges as $\hat{x}$ and the total charge density as Q_{tot}

$$Q_{\text{tot}} = \int_0^{T_N} Q(x)dx \tag{A4}$$

$$\hat{x} = \frac{1}{Q_{\text{tot}}}\int_0^{T_N} Q(x)xdx. \tag{A5}$$

Equation (A3) can be reduced to

$$E = \frac{Q_{\text{tot}}(\hat{x}\varepsilon_{\text{ox}} - T_N\varepsilon_{\text{ox}} - T_{\text{Tox}}\varepsilon_N)}{\varepsilon_0\varepsilon_{\text{ox}}(T_{\text{Box}}\varepsilon_N + T_N\varepsilon_{\text{ox}} + T_{\text{Tox}}\varepsilon_N)} + \frac{V_G}{\text{EOT}}. \tag{A6}$$

Based on (1) in Part I

$$\Delta V_{\text{FB,ch}} = Q_{\text{tot}}\left(\frac{T_{\text{Tox}}}{\varepsilon_0\varepsilon_{\text{ox}}} + \frac{T_N - \hat{x}}{\varepsilon_0\varepsilon_N}\right). \tag{A7}$$

When we substitute (A7) into (A6), we simply obtain

$$E = \frac{V_G - \Delta V_{\text{FB,ch}}}{\text{EOT}}. \tag{A8}$$

Appendix B
Modified Hole Direct Tunneling Current Through an ON Double Layer [7]

Holes tunnel through the oxide potential barrier and part of the nitride potential barrier, and the MFN equation can be written as

$$J = \alpha E_{\text{ox}}^2 \exp\left(-\frac{E_c}{E_{\text{ox}}}\right). \tag{A9}$$

E_{ox} is the bottom oxide electric field, and

$$\alpha = \frac{m}{m_s}\frac{q^3}{16\pi\hbar\left(\phi_b^{1/2} - \phi^{1/2} + \gamma\sqrt{m_N/m_s}(\phi - \phi_2)^{1/2}\right)^2} \tag{A10}$$

$$E_c = \frac{4\sqrt{2m_s}\left(\phi_b^{3/2} - \phi^{3/2}\right) + 4\gamma\sqrt{2m_N}(\phi - \phi_2)^{3/2}}{3\hbar q} \tag{A11}$$

where m is the mass of a free hole, m_s is the effective mass of a hole in the oxide, m_N is the effective mass of a hole in the nitride, q is the electron charge, $\hbar$ is the reduced Planck constant, ϕ_b is the barrier height of oxide for hole tunneling, ϕ_2 is the energy difference between the oxide conduction band edge and the nitride conduction band edge and is referred to as the nitride barrier height, γ is the ratio of the oxide and nitride dielectric constants ($\gamma = \varepsilon_N/\varepsilon_{\text{ox}}$), T_{Box} is the thickness of the bottom oxide, and ϕ is the energy on T_{Box} location which is measured from the Si substrate/oxide interface. ϕ can be written as

$$\phi = \phi_b - qE_{\text{ox}}T_{\text{Box}}. \tag{A12}$$

In our fitting, we choose $T_{\text{Box}} = 20$ Å (the bottom oxide thickness of the S14), $\phi_b = 4.9q$, $\phi_2 = 2.2q$, $m_s = 0.48m$, and $m_N = 0.02m$.

Appendix C
Detailed Derivation of Total Hole Charge Q_h and Hole Mean Vertical Location x_h

We assume that the flat-band voltage shift only comes from the hole injection during $-$FN erasing, whereas the electrons are fixed. Therefore, we can define the hole flat-band voltage shift by

$$\Delta V_{\text{FBh,ch}}(t) = V_{\text{FB,ch}}(t) - V_{\text{FB,ch}}\ \text{(as-programmed)} \tag{A13}$$

$$\Delta V_{\text{FBh,pl}}(t) = V_{\text{FB,pl}}(t) - V_{\text{FB,pl}}\ \text{(as-programmed)}. \tag{A14}$$

Similar to the derivation of Section II in Part I, the hole flat-band voltage shifts are given by

$$\Delta V_{\text{FBh,ch}} = Q_h\left(\frac{T_{\text{Tox}}}{\varepsilon_0\varepsilon_{\text{ox}}} + \frac{T_N - \hat{x}_h}{\varepsilon_0\varepsilon_N}\right) \tag{A15}$$

$$\Delta V_{\text{FBh,pl}} = Q_h\left(\frac{T_{\text{Box}}}{\varepsilon_0\varepsilon_{\text{ox}}} + \frac{\hat{x}_h}{\varepsilon_0\varepsilon_N}\right) \tag{A16}$$

where $\hat{x}_h$ is the hole mean vertical location.

From (A15) and (A16), we can obtain Q_h and $\hat{x}_h$, as follows:

$$Q_h = \varepsilon_0\varepsilon_{\text{ox}}\frac{\Delta V_{\text{FBh,ch}} + \Delta V_{\text{FBh,pl}}}{\text{EOT}} \tag{A17}$$

$$\hat{x}_h = \frac{\Delta V_{\text{FBh,pl}}(T_{\text{Tox}}\varepsilon_N + T_N\varepsilon_{\text{ox}}) - \Delta V_{\text{FBh,ch}}T_{\text{Box}}\varepsilon_N}{\varepsilon_{\text{ox}}(\Delta V_{\text{FBh,ch}} + \Delta V_{\text{FBh,pl}})}. \tag{A18}$$

Equations (A17) and (A18) are also valid even for an arbitrary hole distribution, and the detailed derivation is similar to the Appendix in Part I.

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