IOPscience iopscience.iop.org

Home Search Collections Journals About Contact us My IOPscience

The Linear Combination Model for the Degradation of Amorphous Silicon Thin Film Transistors under Drain AC Stress

This content has been downloaded from IOPscience. Please scroll down to see the full text.

2008 Jpn. J. Appl. Phys. 47 6228

(http://iopscience.iop.org/1347-4065/47/8R/6228)

View the table of contents for this issue, or go to the journal homepage for more

Download details:

IP Address: 140.113.38.11
This content was downloaded on 25/04/2014 at 15:29

Please note that terms and conditions apply.

Japanese Journal of Applied Physics
Vol. 47, No. 8, 2008, pp. 6228–6235

©2008 The Japan Society of Applied Physics

The Linear Combination Model for the Degradation of Amorphous Silicon Thin Film Transistors under Drain AC Stress

Ya Hsiang TAI, Ming-Hsien TSAI[1], and Shih-Che HUANG[2]

Department of Photonics and Display Institute, National Chiao Tung University, Hsinchu, Taiwan 30010, R.O.C.
[1]*Industrial Technology R and D Master Program of Image Display Technologies, College of Engineering, National Chiao Tung University, Hsinchu, Taiwan 30010, R.O.C.*
[2]*Department of Photonics and Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu, Taiwan 30010, R.O.C.*

(Received December 20, 2007; accepted April 26, 2008; published online August 8, 2008)

The degradation behavior of hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) under steady-state (DC) and pulsed (AC) stress on drain electrode has been investigated in this paper. Signals with various peak levels, frequencies and duty ratios are applied onto the drain electrode to see their effects on device's reliability. The effects of state creation and removal are found to still be the dominant degradation mechanisms of drain stress. With the experiment data, it is significantly proved that the degradation behavior can be predicted by analyzing the gate-to-source and gate-to-drain vertical electric field during stress. Furthermore, a linear combination model has been contributed in this paper. By using this model, one can estimate the threshold voltage shift under drain AC stress of different voltage levels, frequencies, duty ratios for a given stress time. With satisfactory agreement between the real and estimated data, this model has been proved to be very useful in predicting and evaluating a-Si:H TFT reliability with both gate and drain signal applied. [DOI: 10.1143/JJAP.47.6228]

KEYWORDS: a-Si:H thin film transistor (TFT), drain stress, reliability model

1. Introduction

Hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) have been widely studied because of their various applications in liquid-crystal displays (LCDs). The electrical instability of a-Si:H TFTs is one of the most serious phenomena which may be the key factor in evaluating the performance of TFT products.

The most important instability issue in a-Si:H TFTs is the shift of threshold voltage caused by a prolonged application of gate bias stress. Many reports indicated that the instability of a-Si:H TFTs results from the effects of charge trapping and defect state creation.[1,2] The charge trapping is dominant at high electric fields and/or long stress time and is related to the trap sites in the silicon nitride (SiN_x) gate insulator. In contrast, the defect state creation is dominant at lower electric fields and associates with the breaking of Si–Si weak bonds in the a-Si:H layer and at the a-Si:H/SiN_x interface as well as the increase of density of defect states.[3] The charge trapping shows logarithmic time dependence while the state creation presents power-law time and thermally activated temperature dependence. In recent research, for transistors made with silicon nitride as the gate insulator, the threshold voltage shift for low negative gate-bias is proposed to be dominated by the bias-stress-induced removal of dangling-bond states because the zero-bias Fermi energy position for these transistors is near the conduction band.[4]

The degradation behavior of a-Si:H TFTs under gate DC and AC stress have been extensively discussed.[5–7] For positive gate DC stress, the combination of defect state creation and negative charge trapping can result in an additive effect of current transfer characteristics (*I*–*V*) curves to shift positively. But for negative gate DC stress, the decrease of deep-gap states in a-Si:H layer dominates the degradation while trapping of positive carriers may also occur, causing the *I*–*V* curve to shift negatively. The degradation of a-Si:H TFTs under gate AC stress is proposed to be treated as the composition of gate DC stress. The degradation depends on the frequencies for negative gate AC stress which can be explained by the resistance and capacitance (RC) time delay effect.[8] And the different effective stress time results in obvious duty ratio dependence of gate AC stress.

More recently, there has been significant progress in extending the applications of a-Si:H TFTs. The integration of row and column drivers on the backplane of LCDs is one of the promising applications. Unlike traditional application, a-Si:H TFTs in the column driver act no longer switch TFTs only but driver TFTs as well. Such application would require the device to withstand voltages stress on both gate and drain terminals. And as such, the instability will become a key concern for proper operation of the pixel circuit and would seriously affect its life time. However, in contrast of the widely discussed instability under gate stress, the degradation behavior of a-Si:H TFTs under drain stress has been paid much less attention. In this study, the instability of a-Si:H TFTs under drain DC and AC stress with various voltage level, signal frequency, and duty-cycle conditions is discussed to verify the degradation behavior under drain stress. Furthermore, based on the measured data from drain DC stress, a simple linear combination method is proposed to estimate the threshold voltage shift for the device under drain AC stress. By using this model, the degradation behavior and the life time of a-Si:H circuit can be easily predicted with simple equations.

2. Experimental Methods

The a-Si:H TFTs used in this study are the conventional bottom-gate inverted stagger structure on glass substrates. After the deposition and patterning of gate metal on the glass substrates, three layers, i.e., silicon nitride (SiN_x, 4000 Å), a-Si:H, and n+ a-Si:H films, are successively deposited in the plasma enhanced chemical vapor deposition (PECVD) system. After making the source/drain electrodes, the n+ a-Si:H region between the source/drain electrodes is etched off by reactive ion etch (RIE) method. Then, the passivation layer is used to cap the channel region to complete the fabrication procedure. All TFTs with the same length (*L*) of

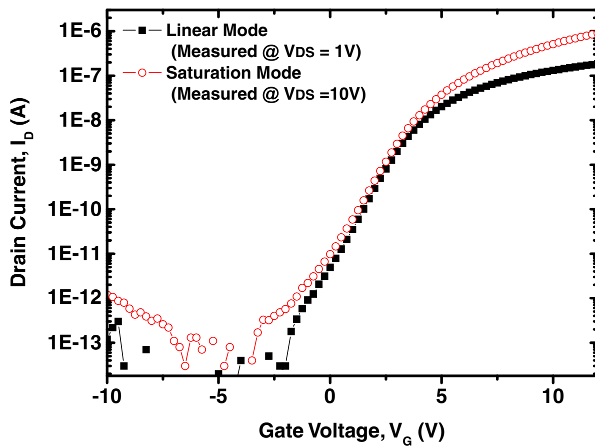


Fig. 1. (Color online) Current transfer characteristics for the fresh a-Si:H TFT used in this work.

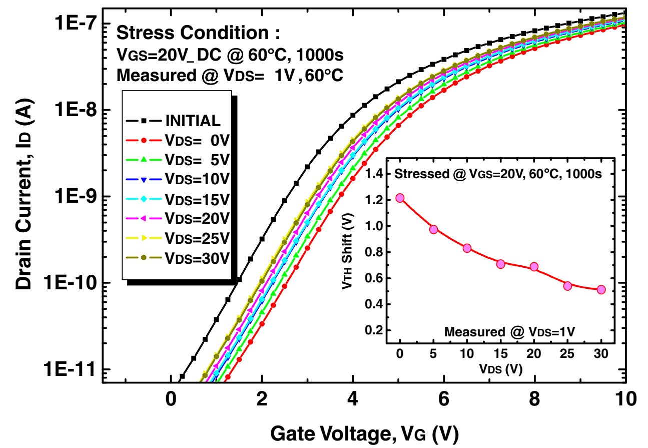


Fig. 2. (Color online) I_D–V_G behavior of the devices before and after ON region drain DC stress with different V_{DS} levels. The inset shows the V_{DS} dependence of V_{TH} shift for ON region drain DC stress.

5 µm and width (W) of 20 µm are used for instability test in this study.

In order to simulate the stress conditions of most advanced applications, various experiments for drain DC and AC stress with gate-bias are performed. The HP41501 pulse generator and HP4156 precise semiconductor parameter analyzer are used to perform stress on the devices and to extract the transfer characteristics of the devices after stress. The current transfer characteristics for the a-Si:H TFT used in this work is shown in Fig. 1. The threshold voltage and subthreshold swing of the fresh device are respectively 4.3 V and 1.08 V/decade. For enhancing the unapparent degradation, all the stress and measurement conditions are performed under 60 °C which is about the real operating environment temperature in most applications.

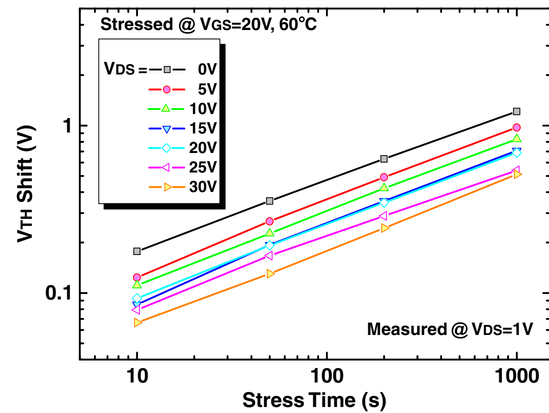


Fig. 3. (Color online) V_{TH} shift vs stress time for ON region drain DC stress.

3. Discussion

3.1 *Drain DC stress*

The experiment conditions of drain DC stress are separated into two groups. For ON region drain DC stress, the gate-bias voltage V_G is set to 20 V to keep the TFT channel formed in the a-Si:H layer. Then DC signals of different voltage level are applied on the drain electrode to investigate the effect of drain voltage levels. For OFF region drain DC stress, the gate voltage is set to 0 V (grounded) to keep the TFT operating in OFF region. Also, DC biases of different voltage level are applied on the drain electrode to investigate the degradation in OFF region operation. The stress time is 1000 s and the source electrode is grounded in all stress conditions.

For ON region drain DC stress, with the fixed 20 V gate bias, the drain voltage is modulated from 0 to 30 V with increasing step of 5 V to investigate the effect of drain voltage level. Figure 2 shows the current transfer behaviors for the device before and after ON region drain DC stress. It can be observed that the device after stress shows apparent threshold voltage (V_{TH}) shift and almost unchanged subthreshold swing behavior. The inset in Fig. 2 shows the V_{DS} dependence of V_{TH} shift for ON region drain DC stress. It is observed that threshold voltage shift seriously depends on the supplied drain voltage levels. The V_{TH} shift is about +1.2 V after 1000 s of +20 V gate stress without any drain bias. With the increasing of drain bias voltage, the V_{TH} shift declines to +0.5 V when the drain bias increases to +30 V. In this experiment, from Fig. 3, the obvious power-law time dependence of positive V_{TH} shift can be discovered. This phenomenon indicates that the defect states creation is the dominant instability mechanism of this ON region drain DC stress. From the theory of defect pool model, the rate of defect creation is a function of the barrier to defect formation, the number of carriers, and the density of the weak bond sites.[9] It has also been proven that the higher gate bias applied, the worse degradation a-Si:H TFTs would suffer.[5] In this experiment, when the drain bias increases, the relative V_{GD} is decreased while V_{GS} remains unchanged. And the carrier concentration in the channel near the drain terminal would be reduced by the descending V_{GD} which results in less defect creation. This can explain the drain voltage dependence of a-Si:H TFTs degradation under ON region drain DC stress. Karim *et al.* had reported similar results in their research.[10] Besides the linear region operation, they also reported that once the TFT is saturated, there is no significant change in the concentration of channel charge. As the TFT is further driven into saturation, the change in V_{TH} shift is negligible. This phenomenon is also found in our experiment that when V_{DS} is higher than 15 V (saturation region), the slope of V_{TH} shift curve would

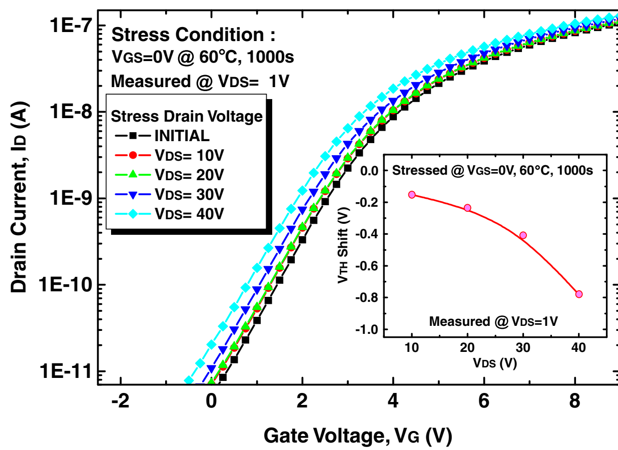


Fig. 4. (Color online) I_D–V_G behavior of the devices before and after OFF region drain DC stress with different V_{DS} levels. The inset gives the V_{DS} dependence of V_{TH} shift for OFF region drain DC stress.

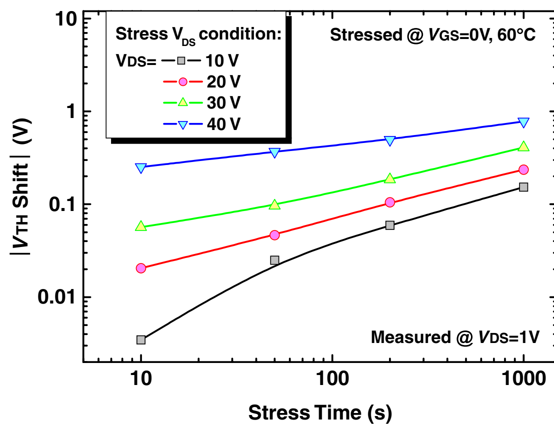


Fig. 5. (Color online) Absolute value of V_{TH} shift vs stress time for OFF region drain DC stress.

become smaller than that as V_{DS} is smaller than 15 V (linear region) as shown in the inset of Fig. 2.

For OFF region drain DC stress, the gate bias is removed and the drain voltage is modulated from 10 to 40 V with increasing step of 10 V. Figure 4 gives the current transfer curves for the device before and after OFF region drain DC stress. Only V_{TH} shift can be observed and changes in subthreshold swing are negligible. The inset in Fig. 4 shows the V_{DS} dependence of V_{TH} shift for OFF region drain DC stress. The V_{TH} shift is about -0.15 V after 1000 s of $+10$ V drain DC stress with gate grounded and becomes more negative to -0.8 V as the drain voltage is up to $+40$ V. Regardless of the polarity, Fig. 5 shows that the power-law time dependence also appears in the OFF region drain DC stress experiment. This should be the evidence of defect removal effect. With no bulk voltages should be taken into consideration, the OFF region drain DC stress is just like the stress condition of negative gate DC stress on the single side of the TFT. That is the reason why the *I*–*V* degradation behavior of OFF region drain DC stress is very similar to negative gate DC stress. As the drain bias increases, the relative V_{GD} becomes more negative and introduces worse degradation at the same time, which can fairly explain the drain voltage dependence in OFF region.

3.2 Drain AC stress

For the advanced circuit applications formed with a-Si:H TFTs, the devices act not only the switches but also the driving components, such that various circuit operation conditions would be applied to the devices in the driving circuit. This reveals that the reliability issue of the circuits under various AC operation conditions would be even more important as the a-Si:H TFTs are applied in the advanced circuits. In the following sections, the device reliability under different operation conditions would be discussed. Three groups of experiment conditions with different drain voltage peak level, frequency and duty ratio conditions are designed to investigate the device's reliability behavior under drain AC stress. For peak level dependent experiment, gate biases of 0 and 20 V are also introduced to keep the TFT operating respectively in OFF and ON region. The AC signals with different voltage peak levels are applied to the drain electrode to investigate the peak level dependence. The frequency here is set as 10 Hz with 50% duty ratio and the low level of the drain voltage is 0 V for these stress conditions.

For the experiment studying frequency dependence, three different experiment conditions are performed. In ON region linear mode, the gate bias is 20 V with drain high level voltage 5 V and low level voltage 0 V. In ON region saturation mode, the gate bias remained 20 V with drain high level voltage changed to 30 V and low level voltage fixed on 0 V. In OFF region experiment, the gate electrode is grounded to make sure the channel is not formed in the a-Si:H layer. The drain high level voltage is set on 40 V with 0 V low level voltage. With these chosen voltage levels, various frequencies of the drain AC signals are applied to investigate the frequency effect of drain AC stress with the duty ratio of 50%.

For duty ratio dependent experiment, it is deliberately set the same stress voltage levels as the frequency dependent experiment for the three operation modes and 10 Hz is picked as the test frequency. In this part of experiment for duty ratio examination, various duty ratios of drain AC signals are designed to investigate the effect of duty ratio of drain AC signal on device's reliability.

3.2.1 ON region operation

In order to investigate the effect of peak level in ON region drain AC stress, the peak level of drain AC signal is modulated from 5 to 30 V with increasing step of 5 V while the low level of drain signal is fixed at 0 V. The gate bias is kept at 20 V and the source is grounded. Figure 6 shows the current transfer behavior of the device before and after the ON region drain AC stress. Similar to the curves in ON region drain DC stress, only V_{TH} shift for the stressed devices can be observed and the subthreshold swing remains almost unchanged. The inset of Fig. 6 shows the V_{DS} dependence of V_{TH} shift for ON region drain AC stress. As can be seen, the degradation behavior of ON region drain AC stress is very similar to that under ON region drain DC stress mentioned in the previous section. The V_{TH} shift also decreases with the increasing drain peak level. In addition, a significant power-law time dependence of the positive V_{TH} shift is discovered in Fig. 7. This proves that defect state creation may also be the main degradation mechanism of ON region drain AC stress.

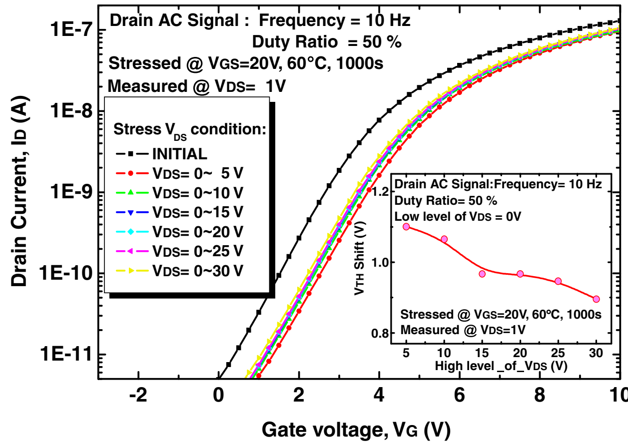


Fig. 6. (Color online) I_D–V_G behavior of the devices before and after ON region drain AC stress with different V_{DS} high-levels. The V_{DS} high-level dependence of V_{TH} shift for ON region drain AC stress is shown in the inset.

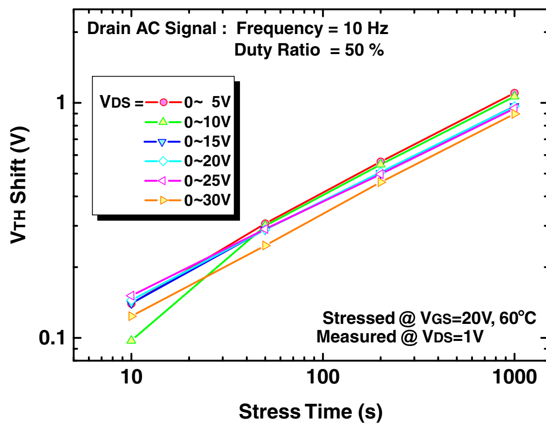


Fig. 7. (Color online) V_{TH} shift vs stress time for ON region drain AC stress.

Compare the data between the insets in Figs. 2 and 6, it can be found that the degradation is worse and the dependence on the drain applied voltage is clearer in DC stress than that in AC stress. It can be interpreted that the degradation near drain is less during the high-level period of drain AC signal than that during the low-level period. Taking the AC stress condition of $V_{DS} = 0$–20 V for example, during the low-level period of drain AC signal, the TFT suffers positive 20 V gate stress on both source and drain edges. But during the high-level period, the relative V_{GD} is zero and only the source edge is stressed by 20 V gate bias thus induces less degradation. In other words, for ON region drain AC stress with duty ratio 50%, only 50% of the stress time of the drain AC signal would result in degradation and thus in such AC stress conditions the positive V_{TH} shift can be effectively reduced.

For the ON region drain DC stress in section A, the V_{TH} shift under $V_{DS} = 0$ V with 20 V gate bias can be treated as pure gate induced degradation ΔV_{TH} (Gate_DC). The V_{TH} shift with non-zero drain DC voltage and 20 V gate bias can be expressed as ΔV_{TH} (Gate_DC + Drain_DC). The reduced V_{TH} shift induced by the drain DC stress can then be expressed as

$$\Delta V_{TH}\,(\text{Drain_DC}) = \Delta V_{TH}\,(\text{Gate_DC}) - \Delta V_{TH}\,(\text{Gate_DC + Drain_DC}). \tag{1}$$

From the illustration in last paragraph, the V_{TH} shift under ON region drain AC stress can thus be estimated as

$$\Delta V_{TH}\,(\text{Gate_DC + Drain_AC}) = \Delta V_{TH}\,(\text{Gate_DC}) - 1/2\Delta V_{TH}\,(\text{Drain_DC}), \tag{2}$$

where $1/2$ represents the 50% duty ratio.

It has been proposed that the V_{TH} shift caused by defect state creation under gate DC bias can be expressed as[7)]

$$\Delta V_{TH}\,(\text{Gate_DC}) = A(V_{GS} - V_T)t^{\beta}, \tag{3}$$

where A and β are temperature-dependent parameters and have been calculated as 3.72×10^{-3} and 0.42 respectively for the samples used in this work. Besides, V_{GS} represents the gate bias, V_{TH} the initial threshold voltage, and t the stress time.

Also, the V_{TH} shift under drain DC stress with gate DC bias has been proposed as[10)]

$$\Delta V_{TH}\,(\text{Gate_DC + Drain_DC}) = \left(\frac{Q_G}{Q_{G0}}\right)A(V_{GS} - V_T)t^{\beta}. \tag{4}$$

The Q_{G0} in eq. (4) is the channel charge under gate DC stress which can be expressed as[10)]

$$Q_{G0} = C_G \cdot W \cdot L(V_{GS} - V_T), \tag{5}$$

where C_G is the TFT gate capacitance per unit area, W is the transistor width, and L is the transistor length. And Q_G in eq. (4) is the channel charge under drain DC stress with gate DC bias and can be expressed as[10)]

$$Q_G = \frac{2}{3}C_G \cdot W \cdot L\frac{(V_{GS} - V_T)^3 - (V_{GD} - V_T)^3}{(V_{GS} - V_T)^2 - (V_{GD} - V_T)^2}, \tag{6}$$

where V_{GD} is the gate-to-drain voltage.

By using eqs. (3) and (4), eq. (1) can be transformed into a general form as

$$\Delta V_{TH}\,(\text{Drain_DC}) = \left(1 - \frac{Q_G}{Q_{G0}}\right)A(V_{GS} - V_T)t^{\beta}. \tag{7}$$

Thus, eq. (2) can be rewritten as

$$\Delta V_{TH}\,(\text{Gate_DC + Drain_AC}) = \left[1 - \frac{1}{2}\left(1 - \frac{Q_G}{Q_{G0}}\right)\right] \cdot A(V_{GS} - V_T)t^{\beta}. \tag{8}$$

The $1/2$ in this equation stands for the 50% duty ratio, which will be discussed later in the duty ratio experiment.

By using these simple equations, the approximate degradation of ON region drain AC stress can be predicted and the satisfactory agreement with the real measured data can be obtained as shown in Figs. 8 and 9. This result can also provide a significant proof that the degradation under ON region drain AC stress is mostly composed of the ON region drain DC stress in high-level period and low-level period of the drain AC signal.

For investigating the frequency effect of ON region drain AC stress, two sets of drain AC signal are chosen which respectively represents the operation in linear mode and saturation mode. Frequencies of drain AC signal progres-

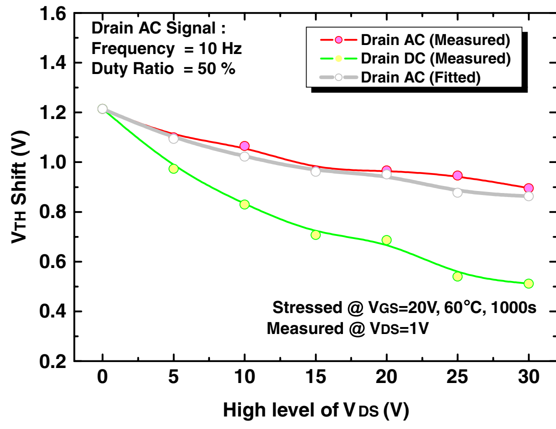


Fig. 8. (Color online) Comparison for V_{TH} shift of ON region drain AC and DC stress vs V_{DS} high-level with fitted result.

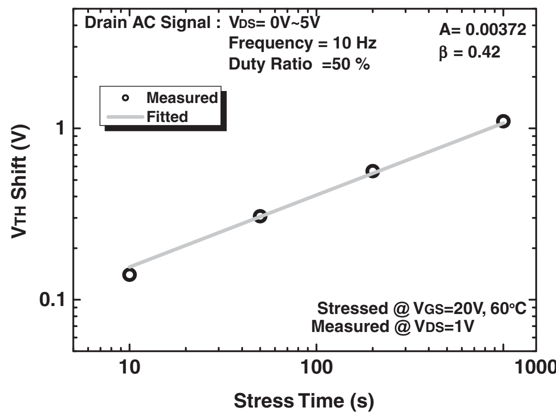
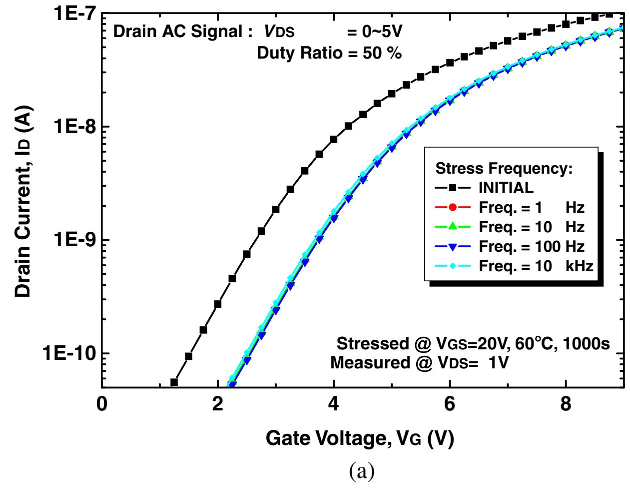
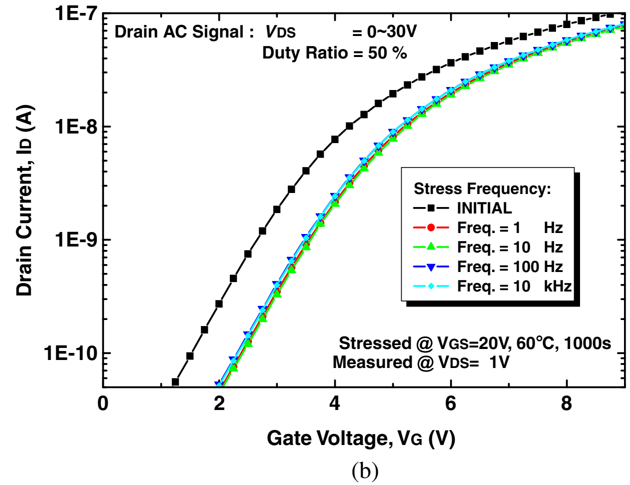


Fig. 9. Comparison between fitted result and measured data of eq. (8).

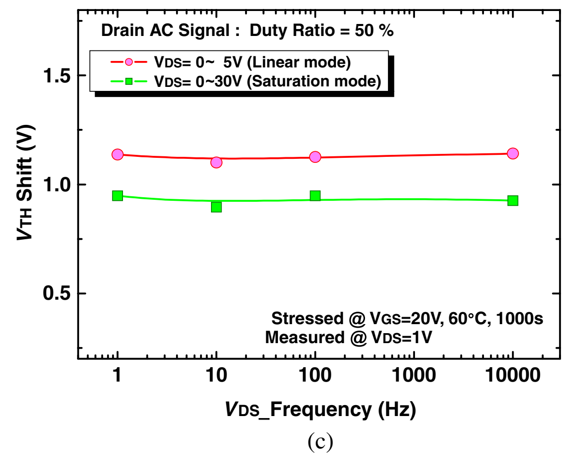
sively ranging from 1 to 10 kHz are designed to investigate the frequency effect. The duty ratio is set as 50%. Figure 10(a) shows the I_D–V_G transfer curves for the devices before and after stress of ON region drain AC stress with different frequency ranging from 1 to 10 kHz and drain AC signal 0–5 V, while Fig. 10(b) shows that with drain AC signal 0–30 V. Only V_{TH} shift is observed in the I_D–V_G curves for the stressed device and the amount of shift for different stress frequencies is very close. Figure 10(c) shows the threshold voltage shift versus drain signal frequencies for ON region drain AC stress. The V_{TH} shift is almost the same under drain AC stress with different frequencies for both linear and saturation mode. In other words, the degradation is not frequency-dependent under these stress conditions. The frequency independent phenomenon was reported in positive gate AC stress.[6,7] For the ON region drain AC stress experiment, the stress conditions can be treated as positive gate AC stress near drain with gate DC stress near source electrode. The RC time delay effect[8] can be introduced to explain the frequency independence. For the gate DC voltage 20 V and the AC signal applied to the drain electrode, the drain electrode essentially suffers from positive gate AC stress by the alternate V_{GD} from drain AC signal. For each low-level period of the drain pulse, due to positive gate bias, it can be inferred that the electrons would rapidly accumulate in the channel. In other words, the RC time constant is low enough to be neglected under this



(a)



(b)



(c)

Fig. 10. (Color online) (a) I_D–V_G behavior of the devices before and after ON region drain AC stress with different frequencies for the drain AC signal 0–5 V. (b) I_D–V_G behavior of the devices before and after ON region drain AC stress with different frequencies for the drain AC signal 0–30 V. (c) Frequency dependence of V_{TH} shift for ON region drain AC stress.

operation frequency. Due to fast electron accumulation, the drain AC signal can generate effective voltage change in the a-Si:H layer synchronously even if the AC frequency is up to 10 kHz. Consequently, the density of created states is almost equal for different stress frequencies. As a result, the degradation of ON region drain AC stress shows no frequency dependence. Furthermore, base on this conclusion, the frequency-independence reveals that eq. (8) would

be applicable in modeling for reliability in the operation conditions under any frequencies.

Besides frequency dependence, duty ratio is also a key to understand the degradation mechanism. Same as the last experiment, two sets of drain AC signal had been chosen for the duty ratio dependence experiment. Pulse width of drain AC signal ranges from 25 to 75 ms progressively with fixed pulse period of 100 ms is adopted to investigate the effect of duty ratio on device reliability. The I_D–V_G curves before and after drain AC stress with different duty ratio for the linear region stress are given in Fig. 11(a), while those for the saturation region stress are given in Fig. 11(b). The after-stress V_{TH} shift versus stress drain signal duty ratio is shown in Fig. 11(c). The V_{TH} shift obviously decreases with the increasing duty ratio for both linear and saturation mode operation. As referred to previous reports,[6,7] the degradation of a-Si:H TFTs under gate AC stress shows apparent duty ratio dependence because of the effective stress time of the gate AC stress. Back to the experiment in this work with ON region drain AC stress, based on the discussion above, the relative V_{GD} plays an important role of the degradation. In addition to the +20 V gate DC stress near source, the drain electrode also suffers +20 V gate stress during low-level period of the drain AC signal. Only the stress time of drain AC signal which operates in high-level period can effectively reduce the degradation. Thus, the degradation decreases with the increasing duty ratio and shows apparent duty ratio dependence. Base on this result, eq. (8) can be refined as:

$$\Delta V_{TH}\ (\text{Gate_DC} + \text{Drain_AC}) = \left[1 - Dc\left(1 - \frac{Q_G}{Q_{G0}}\right)\right] \cdot A(V_{GS} - V_T)t^{\beta}, \quad (9)$$

where 1/2 in eq. (8) is replaced with Dc representing duty ratio.

By using eq. (9), the approximate degradation of ON region drain AC stress with various duty ratios under any frequencies and stress time can be predicted. And the fitted result shows great agreement with the real measured data, as shown in Fig. 12. However, this equation is only used for evaluating approximate result. Some detailed factors such as the state relaxation during drain high-level and low-level periods which has not yet been quantified are neglected.

3.2.2 OFF region operation

For OFF region drain AC stress, the gate and source voltages are set to 0 V (grounded) to keep the TFT staying in OFF region. The stress conditions are that the high-level of drain AC signal ranges from 10 to 40 V with increasing step of 10 V while the drain low-level is fixed at 0 V. Figure 13 shows the I_D–V_G curves before and after OFF region drain AC stress with different values of high level of drain AC signal. Similar to the aforementioned ON region drain AC stress, only V_{TH} shifts are apparent and the subthreshold swing remains almost unchanged for the stressed device. The V_{DS} dependence of V_{TH} shift for OFF region drain AC stress is given in the inset of Fig. 13. It can be observed that the V_{TH} shift becomes more negative with the increasing drain high-level and shows the same trend as OFF region drain DC stress. Figure 14 shows the relationship between absolute value of V_{TH} shift and the stress time. It is obvious

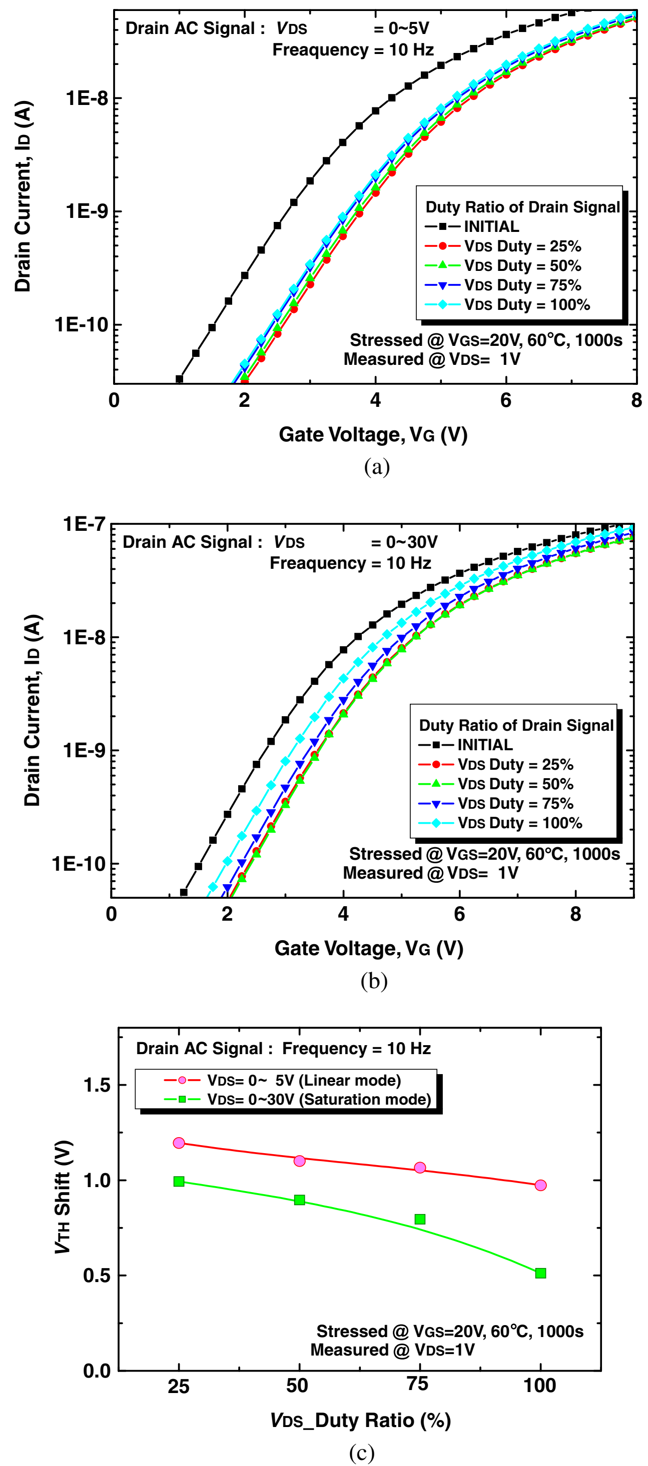


Fig. 11. (Color online) (a) I_D–V_G behavior of the devices before and after ON region drain AC stress with different duty ratios for the drain AC signal 0–5 V. (b) I_D–V_G behavior of the devices before and after ON region drain AC stress with different duty ratios for the drain AC signal 0–30 V. (c) Duty ratio dependence of V_{TH} shift for ON region drain AC stress.

that the power-law time dependence also appears in the OFF region drain AC stress. This means that the dominant mechanism of degradation, defect state removal, is the same as the case in OFF region drain DC stress.

For OFF region drain AC stress, during the low-level period of drain AC signal, all three terminals of a-Si:H TFT are grounded at the same time thus no degradation will occur in this period. But during the high-level period, the stress

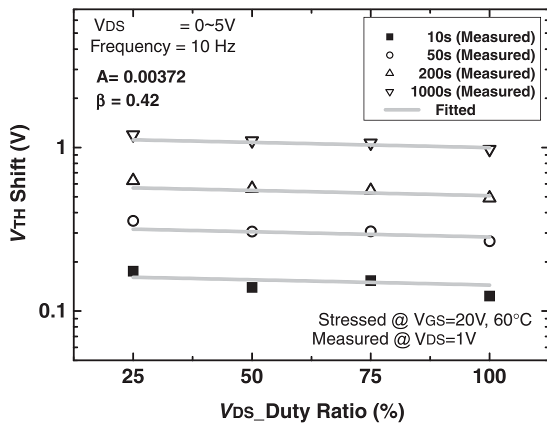


Fig. 12. Comparison between fitted result and measured data of eq. (9) for different duty ratios.

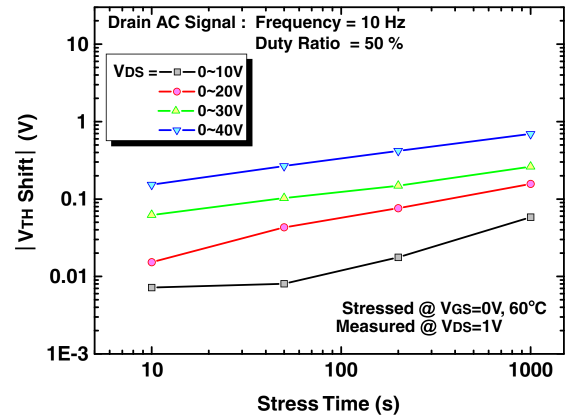


Fig. 14. (Color online) Absolute value of V_{TH} shift vs stress time for OFF region drain AC tress.

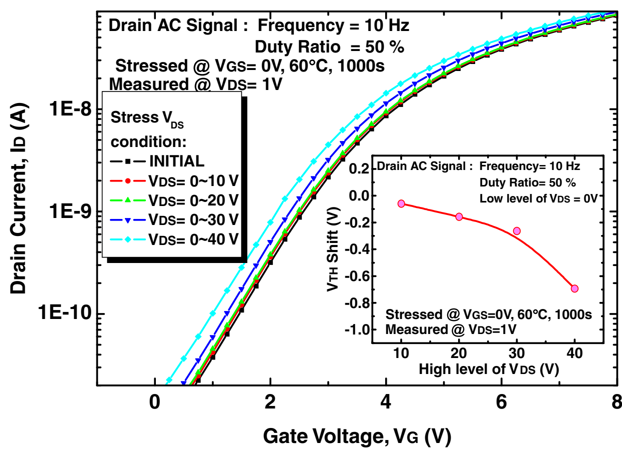


Fig. 13. (Color online) I_D–V_G behavior of the devices before and after OFF region drain AC stress with different high levels for the drain AC signal. The inset is the dependence between the high-level of V_{DS} and V_{TH} shift for OFF region drain AC stress.

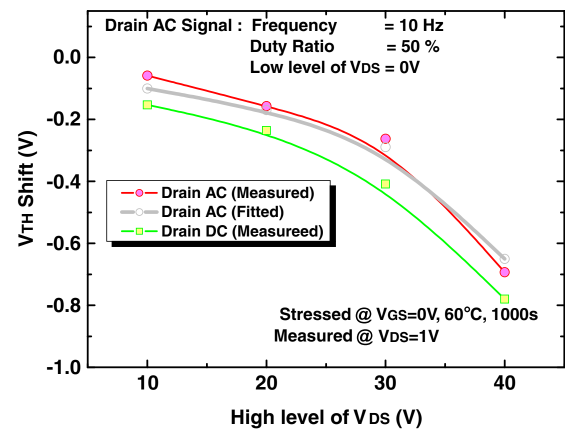


Fig. 15. (Color online) Comparison of measured V_{TH} shift of OFF region drain AC and DC stress with respect to the high-level of V_{DS} and the fitted result.

condition will be the same as the case in OFF region drain DC stress, which is just like negative gate DC stress on single side of the TFT. As the drain high-level increases, the relative V_{GD} becomes more negative and hence introduces more degradation. This can finely explain the dependence of the high-level value in OFF region drain AC stress.

The same as ON region drain AC stress, one may be able to estimate the degradation of OFF region drain AC stress from the measured data of drain DC stress. Since the V_{TH} shift of OFF region drain DC stress shows ideal power law time dependence in Fig. 5, one can easily evaluate the V_{TH} shift after 500 s drain DC stress by fitting these curves. Here, 500 s is the high-level period of 1000 s drain AC signal with 50% duty ratio. As shown in Fig. 15, the evaluated data shows good agreement with the real measured data as expected. This result can provide a significant proof that the degradation under OFF region drain AC stress might mostly be composed of OFF region drain DC stress, which shows apparent dependence on the effective stress time of the high-level period of the drain AC pulse.

Similar experiment is performed to investigate the frequency effect of OFF region drain AC stress on the device. The drain AC signal of 0–40 V which is supposed to have the most apparent result is chosen. The frequency of drain AC signal from 10 to 100 kHz progressively is used to investigate the effect of frequency on device reliability. Figure 16 shows I_D–V_G curves for the device before and after stress and the inset shows the result of OFF region drain AC stress with different stress frequencies. The value of V_{TH} shift becomes less as the drain frequency increases. In contrast to ON region drain AC stress, the degradation shows obvious frequency dependence for OFF region drain AC stress. The RC time delay effect mentioned in the ON region drain AC stress section could also be used to explain this phenomenon. During stress, the drain electrode suffers from relatively negative gate AC stress from the drain AC signal thus the major carriers are holes under such stress condition. Because of the block of n+ a-Si:H layers at the drain junction, the effective resistance for hole supply is very high for negative gate stress. Hence, the RC time constant will become very large that the RC time effect must be taken into account. As the frequency increases, the speed of holes accumulation will no longer able to catch the high frequency AC signal thus the drain AC signal cannot generate effective voltage change in the a-Si:H layer. Consequently, the density of created states will decrease with the increasing frequencies of drain AC signal and induce less degradation.[6,7]

To further study the degradation behavior of OFF region drain AC stress, the experiment conditions with different

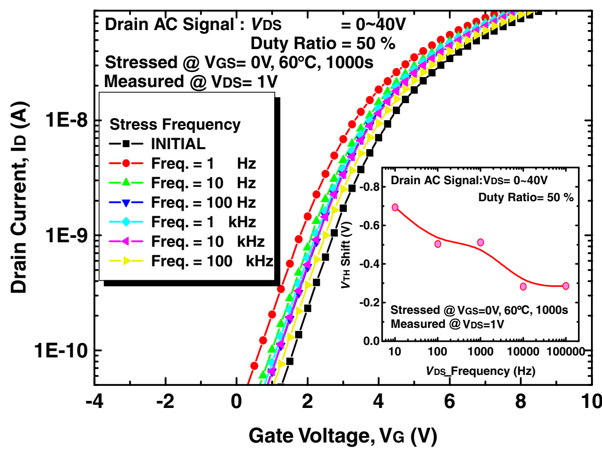
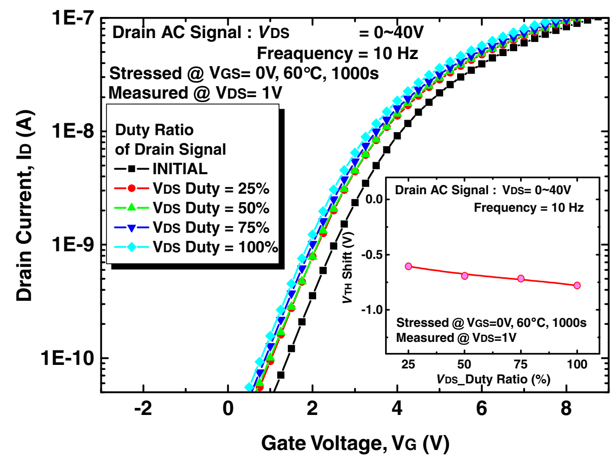


Fig. 16. (Color online) I_D–V_G behavior of the devices before and after OFF region drain AC stress with different drain AC frequencies. The inset shows the frequency dependence of V_{TH} shift for OFF region drain AC stress.

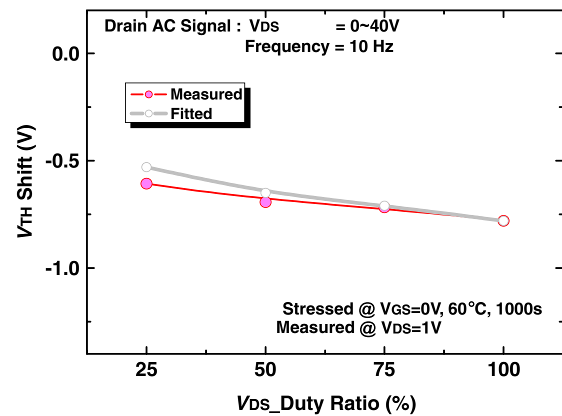
duty ratios had also been performed to verify the effect of effective stress time. Pulse width of drain AC signal from 25 to 75 ms progressively with fixed pulse period of 100 ms is used to investigate the duty ratio effect. Figure 17(a) gives the current transfer behavior for the device before and after stress and its inset shows the extracted V_{TH} shift for the device after stress. From the result shown in the inset, it can be observed that the degradation becomes worse with the increasing duty ratio. From the discussion in the last paragraph, the degradation of OFF region drain AC stress comes from the negative gate stress near drain during on the high-level period of the drain AC signal. In other words, only the stress time of high-level period can effectively generate the degradation of a-Si:H TFTs. As the duty ratio increases, the effective stress time also increases at the same time and the degradation becomes worse. Base on this conclusion, the V_{TH} shift after drain AC stress with duty ratio 25, 50, and 75% under low frequency of 10 Hz are fitted with 250, 500, and 750 s OFF region +40 V drain DC stress as shown in Fig. 17(b). As shown in this figure, the data can be fairly fitted, which indicates that the degradation is strongly affected by the effective stress time and this also reveals that the degradation under low frequency operation can be evaluated from the DC reliability behavior. This finding would be helpful in predicting and evaluating the device reliability behavior for the devices used as switches as well as for the a-Si:H TFT-integrated circuits.

4. Conclusions

The degradation behavior of a-Si:H TFTs under drain DC and AC stress had been thoroughly investigated in this paper. It is significantly shown that one can predict the degradation behavior by analyzing vertical electric field in source and drain electrode for the drain DC stress. The state creation and removal are found to still be the dominant mechanisms of ON region and OFF region drain DC stress, respectively. Furthermore, a linear combination model has been proposed to evaluate the V_{TH} shift of drain AC stress from the drain DC stress data and the good agreement with real measured data is discovered. This could be very useful for the design of advanced a-Si:H applications and the



(a)



(b)

Fig. 17. (Color online) (a) I_D–V_G behavior of the devices before and after OFF region drain AC stress with different duty ratios for the drain AC signal. The inset gives the duty ratio dependence of V_{TH} shift for OFF region drain AC stress. (b) The measured and fitted result for the duty ratio dependence of V_{TH} shift for OFF region drain AC stress.

reliability evaluation for both the devices and circuits of a-Si:H TFTs.

Acknowledgements

This work has been sponsored by the National Science Council, Republic of China (NSC 96-2221-E-009-096). The work is partially supported by Ministry of Economic Affair, Technology Development Program for Academia, The Republic of China, under contract 96-EC-17-A-07-S1-046.

1) M. J. Powell: Appl. Phys. Lett. **43** (1983) 597.
2) A. R. Hepburn, J. M. Marshall, C. Main, M. J. Powell, and C. van Berkel: Phys. Rev. Lett. **56** (1986) 2215.
3) C. van Berkel and M. J. Powell: Appl. Phys. Lett. **51** (1987) 1094.
4) M. J. Powell, S. C. Deane, and W. I. Milne: Appl. Phys. Lett. **60** (1992) 207.
5) J.-W. Tsai, C.-Y. Huang, Y.-H. Tai, H.-C. Cheng, F.-C. Su, F.-C. Luo, and H.-C. Tuan: Appl. Phys. Lett. **71** (1997) 1237.
6) C.-Y. Huang, T.-H. Teng, J.-W. Tsai, and H.-C. Cheng: Jpn. J. Appl. Phys. **39** (2000) 3867.
7) C.-S. Chiang, J. Kanicki, and K. Takechi: Jpn. J. Appl. Phys. **37** (1998) 4704.
8) F. R. Libsch and J. Kanichi: SID Int. Symp. Dig. Tech. Rap., 1993, p. 455.
9) M. J. Powell, C. van Berkel, A. R. Franklin, S. C. Deane, and W. I. Milne: Phys. Rev. B **45** (1992) 4160.
10) K. S. Karim, A. Nathan, M. Hack, and W. I. Milne: IEEE Electron Device Lett. **25** (2004) 188.