High Density and Low Leakage Current in TiO_2 MIM Capacitors Processed at 300 °C

C. H. Cheng, S. H. Lin, K. Y. Jhou, W. J. Chen, C. P. Chou, F. S. Yeh, J. Hu, M. Hwang, T. Arikado, S. P. McAlister, *Senior Member, IEEE*, and Albert Chin, *Senior Member, IEEE*

***Abstract*—We report Ir/TiO_2/TaN metal–insulator–metal capacitors processed at only 300 °C, which show a capacitance density of 28 fF/μm^2 and a leakage current of 3×10^{-8} (25 °C) or 6×10^{-7} (125 °C) A/cm^2 at −1 V. This performance is due to the combined effects of 300 °C nanocrystallized high-κ TiO_2, a high conduction band offset, and high work-function upper electrode. These devices show potential for integration in future very-large-scale-integration technologies.**

***Index Terms*—High κ, Ir, metal–insulator–metal (MIM), TiO_2.**

I. Introduction

THERE is a strong desire to decrease the processing temperature of metal–insulator–metal (MIM) capacitors [1]–[16] while maintaining a high capacitance density ($\varepsilon_0\kappa/t_\kappa$) and low leakage current. This requirement is due to the low-temperature processing associated with low-κ isolation dielectrics, such as poly-arylene. For very-large-scale-integration (VLSI) backend integration, temperatures down to 300 °C may be desirable [17]. Low-temperature-processed MIM capacitors would be useful in the integration of future-generation Ge-on-Insulator (GOI) [18], [19] and IIIV-on-Insulator (IIIVOI) [20] technologies, where the device performance can crucially be dependent on the thermal processing budget. Unfortunately, most high-κ dielectrics, as used for high-density MIM capacitors, require a high process temperature to improve their quality and increase the κ value by crystallization.

Here, we describe the performance of MIM capacitors processed at only 300 °C. A capacitance density of 28 fF/μm^2 was obtained with a leakage current of just 3×10^{-8} A/cm^2. Such capacitor performance compares well with that for devices incorporating 450 °C processed $SrTiO_3$ (STO) [14], [15] and is better than that for 400 °C processed TiTaO [11], [12], TiLaO [13], and STO [16] capacitors. This was achieved by using a high-κ TiO_2 dielectric that had a high κ value of 65 due to nanocrystal formation. This occurs at processing temperatures as low as 300 °C. These MIM capacitors have potential in analog, RF, and dynamic random access memory applications, and are vital for GOI [18], [19] and IIIVOI [20] technologies.

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C. H. Cheng and C. P. Chou are with the Department of Mechanical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: feldcheng@hotmail.com; cpchou@cc.nctu.edu.tw).

S. H. Lin and F. S. Yeh are with the Department of Electrical Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan, R.O.C. (e-mail: d9563815@oz.nthu.edu.tw; fsyeh@ee.nthu.edu.tw).

K. Y. Jhou is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: a9368b.ee95g@nctu.edu.tw).

W. J. Chen is with the Department of Mechanical Materials Engineering, National Yun-Lin Polytechnic Institute, Huwei 632, Taiwan, R.O.C. (e-mail: wjchen@npust.edu.tw).

J. Hu, M. Hwang, and T. Arikado are with Tokyo Electron Ltd., Tokyo 107-8481, Japan (e-mail: jim.hu@tel.com; ming.hwang@tel.com; tsunetoshi.arikado@tel.com).

S. P. McAlister is with the National Research Council of Canada, Ottawa, ON K1A 0R6, Canada (e-mail: Sean.McAlister@nrc-cnrc.gc.ca).

A. Chin is with the Department of Electrical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C., and also with the Nano-Electronics Consortium of Taiwan, Hsinchu 30013, Taiwan, R.O.C. (e-mail: albert_achin@hotmail.com).

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II. Experimental Procedure

The high-κ TiO_2 MIM capacitors were fabricated on standard Si wafers having a 2-μm-thick SiO_2 isolation layer on the Si substrates. Then, TaN (50 nm thick) was deposited on a 200-nm Ta layer and used as the lower capacitor electrode. The TaN surface was first given an NH_3 plasma treatment [13]–[16] and then exposed to an O_2 plasma—this being done to increase the oxidation resistance before the high-κ dielectric deposition and postdeposition anneal (PDA). Then, a 20-nm-thick TiO_2 dielectric was deposited at room temperature by electron-beam evaporation at a pressure of 2×10^{-6} torr followed by a 300 °C PDA for 10 min in an oxygen ambient of 1-atm pressure. Finally, a 20-nm Ir layer was deposited and patterned to form the top electrode. The capacitors were 180 μm × 180 μm in size, thus minimizing any complications from variations in dimensions arising from lithography. The fabricated devices were characterized by standard C–V and J–V measurements.

III. Results and Discussion

In Fig. 1(a) and (b), we show the C–V and J–V characteristics of Ir/TiO_2/TaN capacitors, respectively. A high capacitance density of 28 fF/μm^2 was measured along with a low leakage current of 3×10^{-8} A/cm^2 at −1 V. These results are compared with other MIM data in Table I. Our results are an improvement over those for a Ni/STO/TaN device, which had a slightly lower density of 25 fF/μm^2 and were processed at 400 °C [16]. Since the work function of the Ni electrode is only slightly lower than Ir, the better leakage in the Ir/TiO_2/TaN device, when compared with Ni/STO/TaN, is due to the larger conduction band offset (ΔE_C) of TiO_2 with respect to the STO [21], [22]. This is because the larger ΔE_C and the higher work-function electrode will form a higher Schottky barrier height to lower the leakage current by Schottky emission mechanism [15], [16]. A larger ΔE_C to the metal electrode is also important for the high-temperature leakage current at 125 °C. We found a 125 °C

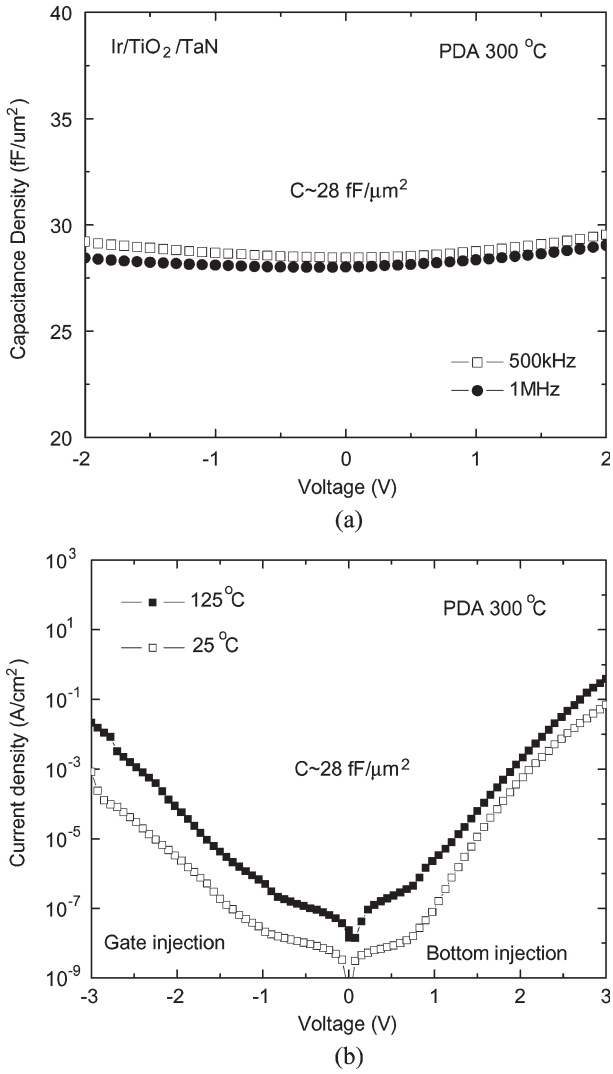

Fig. 1. (a) C–V and (b) J–V (measured at 25 °C and 125 °C) characteristics for Ir/TiO_2/TaN capacitors.

leakage current of 6×10^{-7} A/cm^2 measured at -1 V. This is, to the best of our knowledge, better than previous data and is at a high capacitance density of 28 fF/μm^2 [1]–[16]. In addition, a small loss tangent of 0.013 is obtained at such large 28 fF/μm^2 density using the advanced four-element model and two-frequency calculation [23], which can be decreased with decreasing capacitance density [24]. A quadratic voltage coefficient of capacitance (α) of 5010 ppm/V^2 was obtained at 500 kHz, which can also rapidly be improved with a decreased capacitance density [14] used for analog/RF application. A temperature coefficient of capacitance of 353 ppm/°C was measured even at a high 28 fF/μm^2 density.

To understand the performance improvements, we examined the 300 °C processed TiO_2 structure by cross-sectional TEM. As shown in Fig. 2, the nanocrystallization of TiO_2 is observable even at 300 °C. This nanocrystallization effect yields a high κ value of ~65 for the TiO_2 dielectric and explains why the leakage current is better than that for previous TiTaO [11], [12] and TiLaO [13] MIM capacitors, shown in Table I, which have a κ value of 45. The high κ value, in combination with ΔE_C and the high work-function Ir electrode, helps explain the

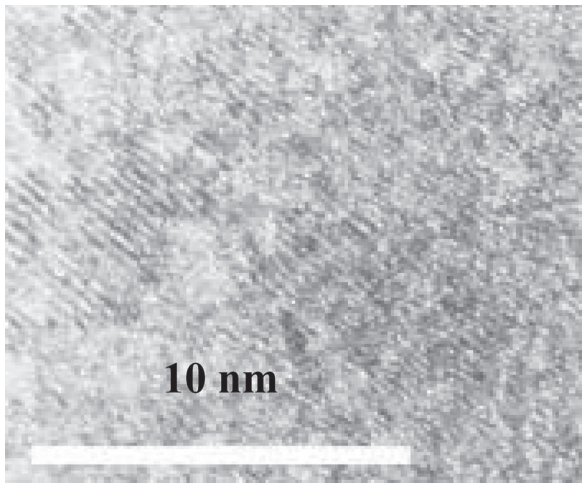

Fig. 2. Cross-sectional TEM image of a TiO_2 sample after 300 °C processing.

TABLE I
COMPARISON OF MIM CAPACITORS THAT HAVE VARIOUS DIELECTRICS AND METAL ELECTRODES

	HfO_2 [7]	Tb-HfO_2 [9]	Al_2O_3-HfO_2 [8]	TiTaO [11]-[12]	TiLaO [13]	STO [16]	STO [15]	**TiO_2 This work**
Process Temp. (°C)	400	400	400	400	400	400	450	300
Top Electrode	Ta	Ta	TaN	Ir	Ir	Ni	TaN	Ir
Work-function (eV)	4.2	4.2	4.6	5.27	5.27	5.1	4.6	5.27
Cap. Density (fF/μm^2)	13	13.3	12.8	23	24	25.2	28	28
Current Density (A/cm^2) @25°C	6×10^{-7} (1V)	1×10^{-7} (2V)	8×10^{-9} (2V)	2×10^{-6} (1V) 2×10^{-5} (2V)	1×10^{-7} (1V) 2.3×10^{-7} (2V)	2×10^{-7} (1V) 8×10^{-6} (2V)	3×10^{-8} (2V)	3×10^{-8} (1V)
Current Density (A/cm^2) @125°C	2×10^{-6} (1V)	2×10^{-7} (2V)	6×10^{-9} (1V) 5×10^{-8} (2V)	–	6.6×10^{-7} (1V) 6.7×10^{-6} (2V)	5×10^{-6} (1V)	–	6×10^{-7} (1V)

good 125 °C leakage current. This is because the larger ΔE_C value lowers the Schottky emission current, and the high κ value decreases the conducting electric field for both Schottky emission and Frenkel–Pool mechanism [15].

To study the thermal stability, we annealed an Ir/TiO_2/TaN capacitor at 350 °C for 20 min under an N_2 ambient. In Fig. 3(a) and (b), we display the C–V and J–V characteristics before and after this thermal treatment. Only a small degradation of the capacitance density and leakage current occurred, indicating the good thermal stability of both the top Ir electrode and the metal-electrodes-capped TiO_2. We also note that good thermal stability has been reported for Ir/HfAlON pMOS even at rapid thermal annealing temperatures of up to 900 °C [25].

IV. CONCLUSION

We have demonstrated Ir/TiO_2/TaN MIM capacitors with a capacitance density of 28 fF/μm^2 along with a leakage current of 3×10^{-8} A/cm^2 at -1 V. Since the device processing was performed at 300 °C, this would permit these capacitors to be integrated into a VLSI backend, along with advanced low-κ isolation dielectrics, or with future front-end GOI and IIIVOI technologies.

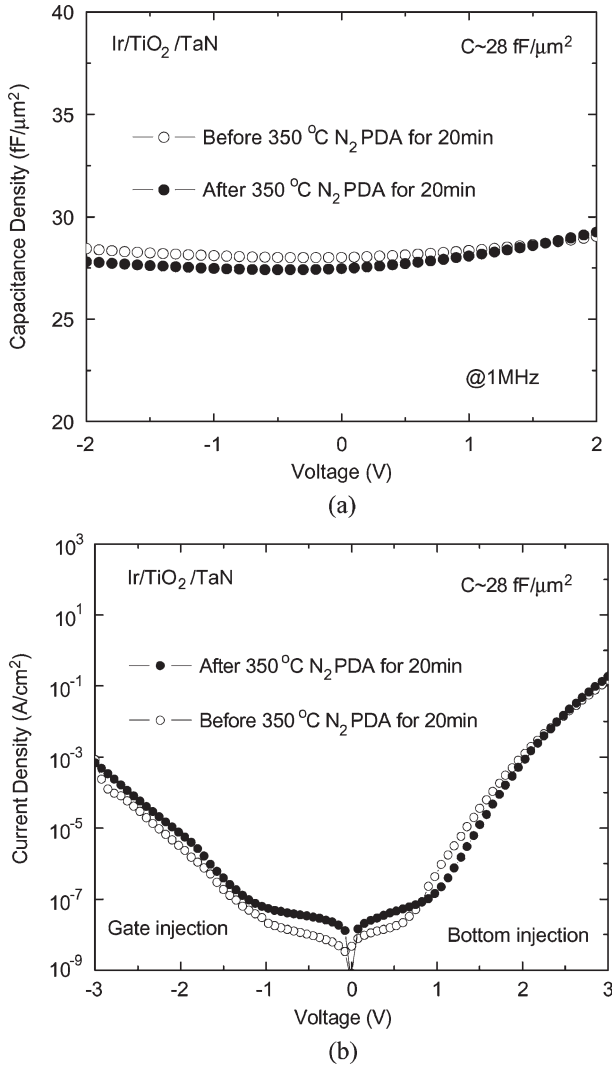

Fig. 3. Thermal stability behavior of a 300 °C formed $Ir/TiO_2/TaN$ capacitor after a 350 °C N_2 anneal for 20 min.

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