Novel Gate-All-Around Poly-Si TFTs With Multiple Nanowire Channels

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***Abstract*—The novel gate-all-around (GAA) poly-Si thin-film transistors (TFTs) with multiple nanowire channels (MNCs) have been, for the first time, fabricated using a simple process to demonstrate high-performance electrical characteristics and high immunity to short-channel effects (SCEs). The nanowire channel with high body-thickness-to-width ratio ($T_{\rm Fin}/W_{\rm Fin}$), which is approximately equal to one, was realized only with a sidewall-spacer formation. Moreover, the unique suspending MNCs were also achieved to build the GAA structure. The resultant GAA-MNC TFTs showed outstanding three-dimensional (3-D) gate controllability and excellent electrical characteristics, which revealed a high on/off current ratio ($> 10^8$), a low threshold voltage, a steep subthreshold swing, a near-free drain-induced barrier lowering, as well as an excellent SCE suppression. Therefore, such high-performance GAA-MNC TFTs are very suitable for applications in system-on-panel and 3-D circuits.**

***Index Terms*—Gate-all-around (GAA), nanowire, poly-Si, thin-film transistors (TFTs), three-dimensional (3-D) device.**

I. Introduction

POLY-Si thin-film transistors (TFTs) have been widely used as switching elements in active matrix displays. For further system-on-panel (SOP) and 3-D circuit applications with high versatile circuit and system integration, there is a need to scale down poly-Si TFTs' device geometries to achieve higher speeds and packing densities [1], [2]. Unfortunately, it has been shown that conventional planar (CP) short-channel poly-Si TFTs suffer from several undesirable short-channel effects (SCEs) in electrical characteristics, including threshold-voltage ($V_{\rm th}$) roll-off, poor subthreshold swing (SS), and large drain-induced barrier lowering (DIBL), which greatly retard their applications [3], [4]. Recently, for single-crystalline-Si MOSFETs, lots of efforts on nonplanar device structures have been developed for better gate electrostatic control of the channel potential, such as double gated, triple gated, Π gated, Ω gated, nanowire channel, and gate-all-around (GAA) [5]–[9]. Among those, GAA FETs, together with the nanowire channel, have been reported to be the best structure for extreme geometry scaling [7]–[9]. It is well known that poly-Si TFTs serve more pronounced SCEs than single-crystalline-Si MOSFETs due to the rich defects in poly-Si thin films [3], [4]. However, few works demonstrated such structures on poly-Si TFTs [10]–[12]. In this letter, we first apply a simple process to achieve the combined GAA and multiple-nanowire-channel (MNC) structures on poly-Si TFTs to improve the device performance and suppress the SCEs.

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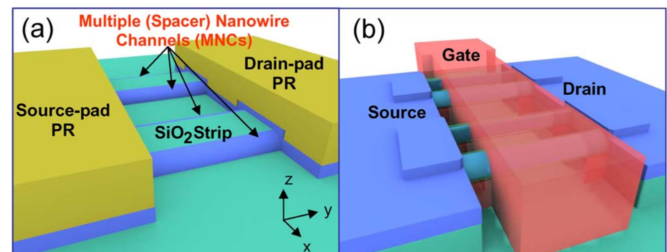

Fig. 1. Schematic diagrams of the key fabrication steps for GAA-MNC TFTs. (a) Formation of the MNCs and S/D pads. (b) Three-dimensional GAA formation.

II. Device Fabrication

The key fabrication steps of the GAA-MNC poly-Si TFTs are schematically shown in Fig. 1. At first, a 50-nm-thick SiN and a 300-nm-thick tetraethyl orthosilicate (TEOS) SiO_2 were sequentially deposited by low-pressure chemical vapor deposition (LPCVD) system at 780 °C and 700 °C on oxidized silicon wafer as a selectively etch-stop and a sacrificial layer, respectively. The sacrificial SiO_2 layer was then patterned with several dummy strips and anisotropically etched only at 100-nm depth to form the step profiles. After a 100-nm-thick a-Si conformal deposition by LPCVD at 550 °C, only the photoresists (PRs) for the source/drain (S/D) pads were patterned to overlap on the two edges of those dummy strips by standard g-line lithography. Subsequently, a reactive ion etch (RIE) (with a transformer-coupled RF power of 250 W and a standard capacitively coupled RF bias power of 150 W) was used to remove the a-Si; meanwhile, a couple of spacer nanowire channels were *in situ* resided in a self-aligned manner against the sidewall of each dummy strip and naturally connected to the S/D pads [Fig. 1(a)]. It should be noted that the nanoscale dimension of the nanowire channels can be defined only by controlling the RIE time without any advanced lithography [11]–[13], and the

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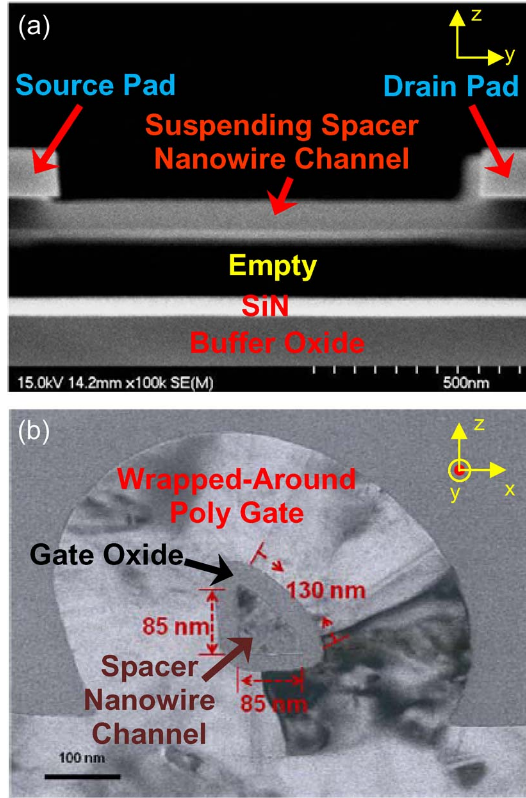

Fig. 2. (a) SEM image of the suspending spacer nanowire channel braced by S/D pads. (b) Cross-sectional TEM image of each channel of GAA-MNCs.

MNCs can be designed with patterning several dummy strips. After the release of S/D-pad PRs, a solid-phase crystallization at 600 °C in N_2 ambient for 24 h was performed to transform the a-Si into poly-Si. Then, the unique suspending MNCs were constructed after the dummy SiO_2 strips were etched away (down to the SiN etch-stop layer) by an HF etchant. Then, the 25-nm-thick TEOS SiO_2 and 200 nm of phosphorous *in situ* doped poly-Si (with a doping level of 5×10^{19} cm^{-3}) were conformally deposited by the LPCVD system at 700 °C and 550 °C as gate insulator and gate electrode, respectively. After gate patterning, a self-aligned phosphorous S/D implantation was performed (at 30 keV to a dose of 5×10^{15} cm^{-2}) [Fig. 1(b)], and a 300-nm-thick passivation oxide layer was deposited, followed by an S/D activation at 600 °C in N_2 ambient for 10 h. Contact opening formation, metallization, and 1-h NH_3 plasma passivation at 300 °C was carried out [14]. For the purpose of comparison, the CP poly-Si TFTs were also fabricated with the same process run.

III. Results and Discussion

Fig. 2(a) shows the scanning electron microscopy (SEM) image of the suspending spacer nanowire channel braced by S/D pads after the removal of dummy strips, and the empty space between the suspending nanowire channel and the etch-stop SiN layer is clearly observed. Fig. 2(b) shows the cross-sectional transmission electron microscopy (TEM) image of each GAA-MNC. The good step coverage is observed on the GAA structure both for the TEOS gate oxide and the phosphorous *in situ* doped poly gate, and the vertical sidewall

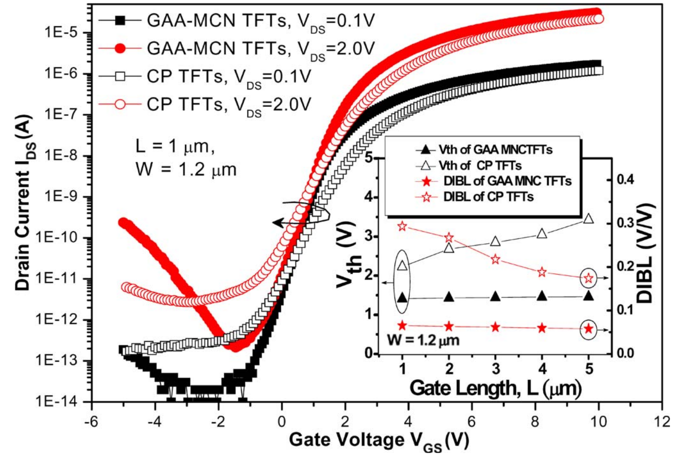

Fig. 3. Transfer characteristics of GAA-MNC and CP TFTs. The inset shows the comparisons of (left) $V_{\rm th}$ and (right) DIBL between GAA-MNC and CP TFTs for different gate lengths.

thickness ($T_{\rm Fin}$), the horizontal width ($W_{\rm Fin}$), and the bevel length of each nanowire channel are about 85, 85, and 130 nm, respectively. Thus, the total surrounding width of each nanowire channel is 300 nm. The aspect ratio $T_{\rm Fin}/W_{\rm Fin}$ of each nanowire channel in the GAA-MNC TFT (approximately equal to one) is much larger than that in the CP TFT and thus features like a fin structure [6], [14].

Transfer characteristics of GAA-MNC and CP TFTs are compared in Fig. 3. Those devices have a gate length (L) of 1 μm and a channel width (W) of 1.2 μm, where the W of GAA-MNC TFTs are defined by four nanowires with two-dummy-strip structure (2 strips $\times$ 2 wires/strip $\times$ 300 nm/wire $=$ 1.2 μm). $V_{\rm th}$ was defined as the gate voltage that is required to obtain a normalized drain current of $I_{\rm DS} = (W/L) \times 10^{-8}$ A at $V_{\rm DS} = 0.1$ V. SS was extracted at $V_{\rm DS} = 0.1$ V, and the maximum on current ($I_{\rm on}$), the minimum off current ($I_{\rm off}$), and the maximum on/off current ratio ($I_{\rm on}/I_{\rm off}$) were defined at $V_{\rm DS} = 2.0$ V. The field-effect mobility (μ) was extracted from the peak linear transconductance at $V_{\rm DS} = 0.1$ V. DIBL was defined as $\Delta V_{\rm GS}/\Delta V_{\rm DS}$ at $I_{\rm DS} = 10^{-10}$ A. Due to the inherently larger surface-to-volume ratio and the smaller volume of nanowire in the GAA-MNC TFT, fewer grain-boundary defects exist in the nanowire channels, leading to the lower minimum $I_{\rm off}$, higher maximum $I_{\rm on}$, lower $V_{\rm th}$, higher μ, and better SS [10]–[12], [16]. Moreover, the MNC scheme can also provide a more efficient NH_3 plasma passivation to reduce the defects and further improve the minimum $I_{\rm off}$, maximum $I_{\rm on}$, $V_{\rm th}$, μ, and SS characteristics [10], [14]. In addition, the 3-D fully surrounding gate (GAA) and the three sharp corners of the spacer profile in GAA-MNC TFTs effectively increase the gate controllability, resulting in higher performance on $I_{\rm on}$, $V_{\rm th}$, SS, μ, and DIBL as well [5], [17], [18]. Therefore, obvious improvement in device characteristics is achieved for the GAA-MNC TFT as compared with the CP TFT. $V_{\rm th}$ decreases from 2.23 to 1.41 V, SS decreases from 0.66 to 0.36 V/dec, minimum $I_{\rm off}$ decreases from 2.72×10^{-12} to 2.14×10^{-13} A, maximum $I_{\rm on}$ increases from 2.21×10^{-5} to 3.12×10^{-5} A, $I_{\rm on}/I_{\rm off}$ increases from 8.12×10^{6} to 1.46×10^{8}, μ increases from 18.8 to 25.5 $cm^2/V \cdot s$, and DIBL

decreases from 0.3 to 0.06 V/V. In addition, the trap densities (N_t) were extracted from the slope of $\ln(I_{\rm DS}/V_{\rm GS})$ versus $(1/V_{\rm GS})$ according to the grain-boundary trap model [19]. It can be found that the GAA-MNC TFT exhibited a lower N_t (1.1×10^{12} cm^{-2}) than the CP TFT (1.5×10^{12} cm^{-2}). This result further confirms the defect reduction in the GAA-MNC TFT. However, the OFF-state leakage current of the GAA-MNC TFT increases more rapidly than that of the CP TFT as the gate voltage decreases continuously, which is also explained by the higher electric field near the drain junction enhanced from these three sharp corners. It could be further improved by using the lightly doped drain or the T-shaped gate structures [20]–[22].

In addition, the inset of Fig. 3 shows the comparisons of $V_{\rm th}$ (left) and DIBL (right) between GAA-MNC and CP TFTs for different gate lengths. GAA-MNC TFTs exhibit negligible $V_{\rm th}$ and DIBL shifts as compared with those of CP TFTs, which is also attributed to the stronger gate controllability from both the 3-D GAA structure and the three sharp corners of the spacer nanowire that weakens the electric field penetration from the drain to the channel to efficiently suppress SCEs.

IV. Conclusion

The novel GAA-MNC TFTs have been demonstrated by using a simple process sequence. The MNCs were performed only with a sidewall-spacer formation. Furthermore, the unique suspending MNCs were also achieved to build the GAA structure. Owing to the nanoscale dimension and the three sharp corners of the spacer nanowire, the 3-D GAA structure, together with the more effective plasma passivation of such an MNC scheme, the GAA-MNC TFTs reveal high-performance characteristics and excellent SCE immunity. Therefore, such TFTs are highly promising for applications in SOP and 3-D circuits.

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