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Formation of thin-film transistors with a polycrystalline hetero-structure channel layer

Miin-Horng Juang[1], I-Shen Tsai[1], S-L Jang[1] and H C Cheng[2]

[1] Department of Electronic Engineering, National Taiwan University of Science and Technology, Kee-Lung Rd, 106 Taipei, Taiwan, Republic of China
[2] Department of Electronic Engineering, National Chiao-Tung University, 300 Hsin-Chu, Taiwan, Republic of China

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Abstract
A thin-film transistor (TFT) with a polycrystalline Si/SiC hetero-structure channel layer has been proposed. For the conventional polycrystalline silicon (poly-Si) channel layer, the leakage current would be considerably increased with increase of the negative gate bias voltage. However, when a polycrystalline Si/SiC stacked channel layer is employed, the leakage current exhibits just a slight increase with increase of the negative gate bias voltage. As a result, the leakage current can be largely suppressed to a low level without degrading the on-state current. Moreover, when the channel length is further scaled down to 1 μm and the gate oxide is reduced to 60 nm thickness, the conventional poly-Si TFT device shows even more obvious deterioration of the leakage current. Instead, for the TFT device with a polycrystalline Si/SiC channel layer, no considerable degradation of the leakage characteristics is caused.

1. Introduction

In recent years, polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have been actively studied for their potential use in the static random-access memory (SRAM) [1] and as the integrating peripheral driving circuits in high-resolution active matrix liquid crystal displays (AMLCDs) due to their large mobility [2]. However, due to the presence of defects in the poly-Si TFT, some issues have to be resolved in comparison with the single crystalline transistors. Leakage current is increased with the increase of gate and drain voltages due to the field emission via trap states (defects) in the depletion region near the drain. This is one of the bias-dependent issues caused by defects in the poly-Si TFT, which cause poor switching characteristics such as a low on/off current ratio [3–6]. TFTs with the lower on/off current ratio used as pixel switching in the AMLCD represent a limiting factor for operation and can degrade the performance of the display.

It has been reported that various drain structures can decrease the leakage current in the polysilicon TFTs due to reduction of electric field intensity near the drain region [7–11]. On the other hand, channel engineering has been employed to improve device characteristics including short-channel effect in ultra-large-scale-integrated circuits. Hence, the TFT device characteristics may also be improved via proper channel engineering. In this study, a TFT structure with a polycrystalline hetero-structure channel layer has been proposed to implement high-performance poly-Si TFTs in the micrometre regime.

2. Device scheme

A typical poly-Si TFT device fabrication process flow is first described below. A 100 nm thick amorphous silicon (a-Si) film was first deposited on a standard glass substrate by low-pressure chemical vapour deposition (LPCVD) at 580 °C. Then, the a-Si thin film was crystallized by 308 nm XeCl excimer laser annealing. After defining the active device layer, an 80 nm thick tetraethyloxysilane (TEOS) gate oxide layer, as a gate dielectric, was deposited by plasma-enhanced chemical vapour deposition (PECVD) at 400 °C. A poly-Si film of 300 nm thickness was then deposited, and delineated as gate electrodes of 1 and 5 μm channel length. The samples were directly implanted with phosphorous

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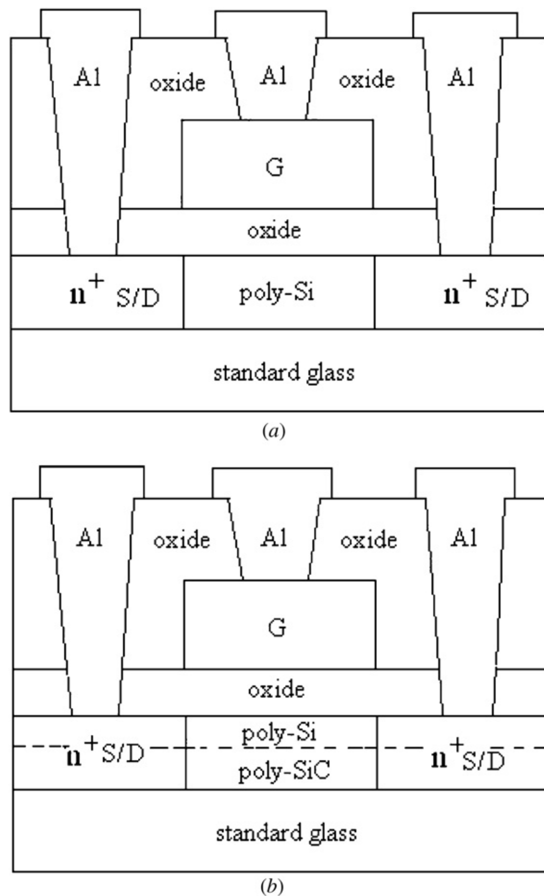

Figure 1. The schematic structure of (*a*) the TFT device with the poly-Si channel and (*b*) the hetero-structure poly-Si/poly-SiC channel.

100 keV to a dose of 4×10^{15} cm^{-2}. The implanted doping impurities were activated by furnace annealing at 600 °C for 90 min. Then, an 800 nm thick TEOS oxide was deposited by PECVD as a passivation layer. By using a photo-mask process for the definition of the gate/source/drain (G/S/D) contact holes and then etching through the oxide layer, the G/S/D contact holes were formed. A 1200 nm thick Al film was subsequently deposited and patterned. Finally, all the samples were sintered at 300 °C for 45 min in a forming gas ambient. Figure 1(*a*) shows the schematic structure of the conventional poly-Si TFT.

In addition, the poly-SiC TFT device was also prepared. A 100 nm thick amorphous SiC (a-SiC) film was first deposited on a standard glass substrate by plasma-enhanced chemical vapour deposition (PECVD) at 400 °C. Then, the a-SiC thin film was crystallized by 308 nm XeCl excimer laser annealing. Similarly, the samples were subsequently treated by the above device fabrication process. As a result, the poly-SiC TFT device was formed.

On the other hand, the TFT device with a hetero-structure channel layer was formed by first depositing a wide-bandgap a-SiC layer on a standard glass substrate by plasma-enhanced chemical vapour deposition at 400 °C and then the a-Si layer was deposited by LPCVD at 580 °C onto the a-SiC layer. Then, the a-Si/a-SiC stacked film was crystallized by 308 nm

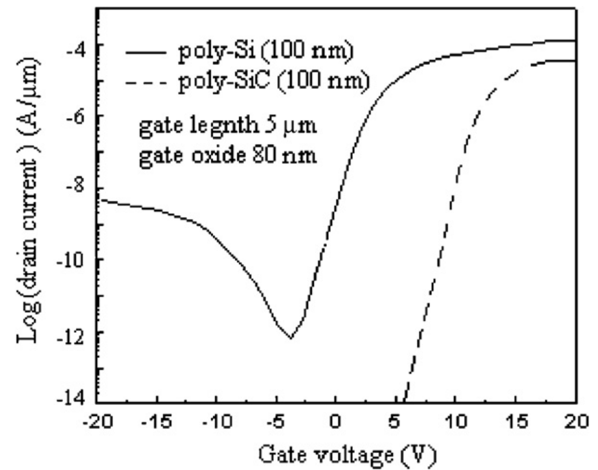

Figure 2. The I_{DS}–V_{GS} characteristic at a V_{DS} of 5 V for the TFT device with a poly-Si and a poly-SiC channel layer.

XeCl excimer laser annealing. Similarly, the samples were subsequently treated by the above device fabrication process. Thereby, the TFT device with a hetero-structure channel layer (poly-Si/poly-SiC stacked layer) was implemented. Figure 1(*b*) shows the schematic structure of the TFT with a poly-Si/poly-SiC stacked channel layer.

3. Results and discussion

The TFT leakage current may be largely reduced by using a poly-SiC channel layer, attributable to the wide-bandgap property of the SiC material. Figure 2 shows the I_{DS}–V_{GS} characteristic at a V_{DS} of 5 V for the TFT device with a poly-Si and a poly-SiC channel layer, respectively. The poly-SiC device shows a much smaller leakage current than the poly-Si device. Since the SiC is with a large bandgap, the carrier field emission via trap states may be considerably suppressed due to a larger energy gap between the trap state and the carrier conduction band. However, the poly-SiC device would exhibit a much lower on-state driving current, due to a lower carrier mobility and a smaller amount of induced inversion charges.

On the other hand, as the poly-Si TFT is scaled down to the micrometre regime, a large leakage current is generated. Figure 3 shows the I_{DS}–V_{GS} characteristic at a V_{DS} of 5 V for the poly-Si TFT device with a channel lengths of 1 and 5 μm. The leakage current is increased to be about two to three orders larger, while the TFT channel length is reduced from 5 μm to 1 μm. According to the basic device physics, when the channel length of the TFT device is scaled down to 1 μm, the channel region would endure more serious source/drain bulk punch-through caused by the short-channel effect. More serious source/drain bulk punch-through within the channel region would obviously result in a significantly larger lateral electric field within the channel region below the surface channel. For a long-channel device, however, a large lateral electric field can only be found near the drain region, but not within the channel region. Accordingly, for the shorter channel poly-Si TFT device, carrier field emission and/or

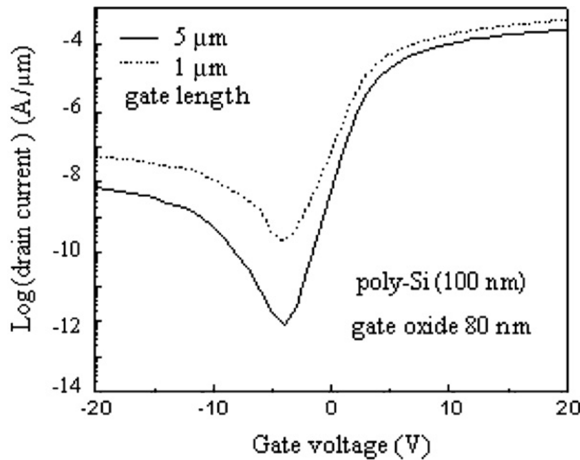

Figure 3. The I_{DS}–V_{GS} characteristic at a V_{DS} of 5 V for the poly-Si TFT device with a channel length of 1 and 5 μm.

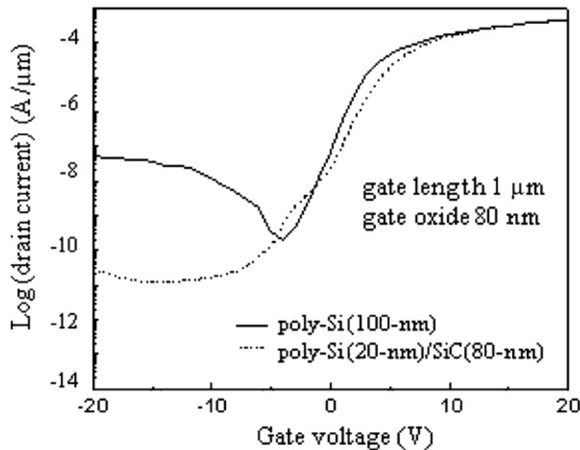

Figure 4. The I_{DS}–V_{GS} characteristic at a V_{DS} of 5 V for the TFT devices with a poly-Si and a poly-Si/poly-SiC channel layer, with a channel length of 1 μm and a gate oxide of 80 nm thickness.

carrier tunnelling via the traps [12] within the channel region would be further enhanced. In addition, the source/drain bulk punch-through would shorten the bulk leakage path, also degrading the leakage characteristics. As a result, a much larger leakage current is caused.

Though the poly-SiC channel layer can greatly suppress the leakage, the on-state current is largely degraded. Hence, a poly-Si layer is stacked atop a poly-SiC layer to form a poly-Si/poly-SiC stacked channel layer for retaining the on-state current. In addition, by this scheme, the source/drain bulk punch-through would mainly occur within the SiC channel region. Therefore, the leakage current due to the carrier field emission via trap states may be greatly suppressed due to the wide bandgap of SiC. Accordingly, when a poly-Si/poly-SiC stacked channel layer is employed in the polycrystalline TFT device, the leakage current may be suppressed without degrading the on-state current. As a result, while the poly-Si channel layer (100 nm) is replaced by a stacked poly-Si/poly-SiC channel layer (20 nm poly-Si/80 nm poly-SiC), the leakage current is significantly suppressed. Figure 4 shows

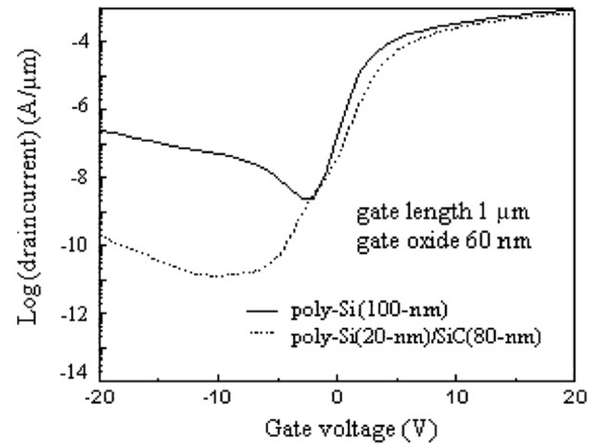

Figure 5. The I_{DS}–V_{GS} characteristic at a V_{DS} of 5 V for the TFT devices with a poly-Si and a poly-Si/poly-SiC channel layer with a channel length of 1 μm and a gate oxide of 60 nm thickness.

the I_{DS}–V_{GS} characteristic at a V_{DS} of 5 V for the TFT devices with a single poly-Si and a hetero-structure poly-Si/poly-SiC channel layer, with a channel length of 1 μm and a gate oxide of 80 nm thickness. The TFT device with a poly-Si/poly-SiC channel layer shows just a slight decrease of the on-state current. Moreover, the leakage current is significantly suppressed to a low level at the negative gate bias, even to 20 V. However, for the TFT device with a poly-Si channel layer, the leakage current is obviously increased with increase of the negative gate bias voltage.

Similarly, even though the gate oxide thickness is reduced to increase the on-state current, the leakage current of the TFT device with a poly-Si/poly-SiC stacked channel layer is still kept at a low current level. Figure 5 shows the I_{DS}–V_{GS} characteristic at a V_{DS} of 5 V for the TFT devices with a poly-Si and a poly-Si/poly-SiC channel layer, respectively, of a channel length of 1 μm and a gate oxide of 60 nm thickness. In terms of the TFT device with a poly-Si/poly-SiC channel layer, even for a gate oxide of 60 nm thickness, the leakage current only shows slight degradation with increase of the negative gate bias voltage. However, the TFT device with a poly-Si channel layer would exhibit an obviously large leakage current.

Since a thinner gate oxide would result in the increase of the resultant electric field in the channel region, a larger leakage is inevitably generated for the channel layer with trap states. Figure 6 also shows the I_{DS}–V_{GS} characteristic at a V_{DS} of 5 V for the poly-Si TFT devices with gate oxides of 60 and 80 nm thickness and a channel length of 1 μm. The result can reflect the resultantly enhanced electric field due to the thinner gate oxide. On the other hand, however, when a poly-Si/poly-SiC hetero-structure channel layer is employed, the leakage current is still low, even for a 60 nm gate oxide. Figure 7 also shows the I_{DS}–V_{GS} characteristic at a V_{DS} of 5 V for the poly-Si/poly-SiC TFT devices with gate oxides of 60 and 80 nm thickness and a channel length of 1 μm. This result may reflect the largely suppressed carrier

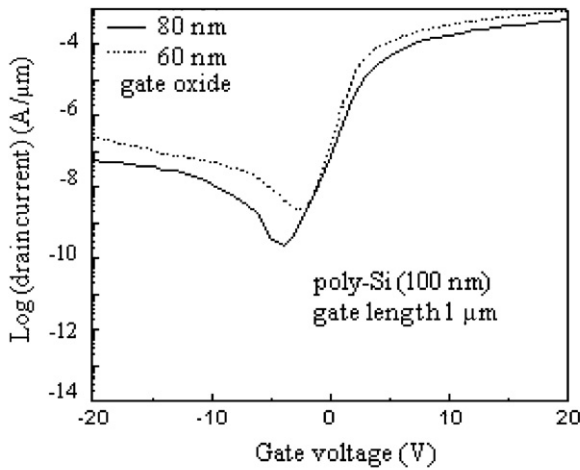

Figure 6. The I_{DS}–V_{GS} characteristic at a V_{DS} of 5 V for the poly-Si TFT devices with gate oxides of 60 and 80 nm thickness for a channel length of 1 μm.

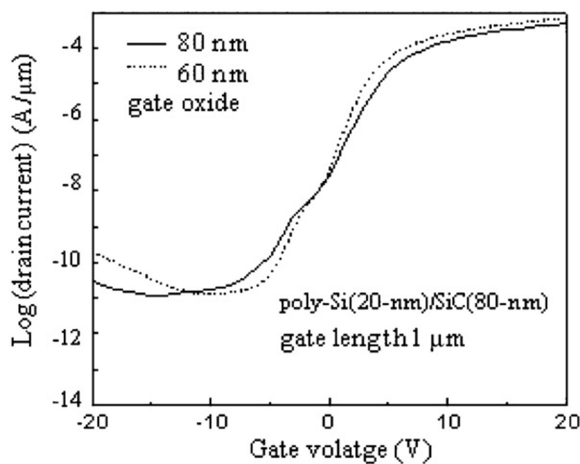

Figure 7. The I_{DS}–V_{GS} characteristic at a V_{DS} of 5 V for the poly-Si/poly-SiC TFT devices with gate oxides of 60 and 80 nm thickness for a channel length of 1 μm.

field emission via trap states due to the wide bandgap of SiC.

4. Conclusions

Formation of thin-film transistors with a polycrystalline Si/SiC hetero-structure channel layer has been studied. For the conventional poly-Si channel layer, the leakage current would be considerably increased with increase of the negative gate bias voltage. The poly-SiC channel layer can greatly suppress the leakage, due to the wide-bandgap property of the SiC. However, the on-state current is largely degraded because of low mobility. Accordingly, when a poly-Si/poly-SiC stacked channel layer is employed, the leakage current can be largely suppressed to a low level, without degrading the on-state current. By this scheme, in addition, the leakage current exhibits just a slight increase with increase of the negative gate bias voltage. On the other hand, when the channel length is further scaled down to 1 μm and the gate oxide is reduced to 60 nm thickness, the conventional poly-Si TFT device shows even more obvious deterioration of the leakage current. Instead, for the TFT device with a poly-Si/poly-SiC channel layer, no considerable degradation of the leakage characteristics is caused. The source/drain bulk punch-through and thus the considerably induced lateral electric field would mainly occur within the SiC region. Therefore, the carrier field emission via the trap state within the channel region would be greatly suppressed due to the wide bandgap of SiC.

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