## SOLID-STATE SCIENCE AND TECHNOLOGY

# A New Tungsten Gate Metal Oxide Semiconductor Capacitor Using a Chemical Vapor Deposition Process

**Wen-Kuan Yeh, Yeu-Cherng Shiau, and Mao-Chieh Chen***

*Department of Electronics Engineering, National Chiao Tung University and National Nano Device Laboratory, Hsinchu, Taiwan*

ABSTRACT

A new process for tungsten gate metal oxide semiconductor (MOS) capacitors has been developed using chemical vapor deposition (CVD) of tungsten on a thin poly-Si layer of appropriate thickness. The poly-Si acts as a sacrificial layer and is consumed during the CVD of tungsten (W). This process yields a nearly pure W metal gate after $SiH_4$ reduction of $WF_6$ at 300°C. Compared with sputtered tungsten films, the CVD tungsten film has lower resistivity and lower intrinsic film stress. In addition, the CVD tungsten metal gate MOS capacitor has a lower interface state density ($D_{it}$) and a higher charge-to-breakdown ($Q_{bd}$), than sputter-deposited tungsten gate MOS capacitors.

## Introduction

As device dimensions continue to decrease for higher density and improved performance in integrated circuits, there is a growing demand for more highly conductive gate and interconnection materials. The poly-Si now used for this purpose in conventional processing has certain limitations, due mainly to limited conductivity. In addition, it is well known that the use of $p^+$-polygates has become indispensable for p-channel metal oxide semiconductor field effect transistors (MOSFETs) in the deep submicron regime. However, the penetration of boron impurities results in a shift of the threshold voltage, an increase in subthreshold swing and leakage current, and degradation of the gate oxide reliability.[1-3] Metal silicides[4-6] have been considered because their conductivities are higher than that of poly-Si by one order of magnitude. Furthermore, it is expected that materials with conductivities higher than those of silicides will be required in the future for very high density integrated circuits. Tungsten is considered a very promising gate material candidate because it makes gate implantation unnecessary. Furthermore, tungsten also provides low resistivity and near midgap work function.[7] Tungsten gates have conventionally been prepared by sputtering,[8] plasma- or laser-enhanced chemical vapor deposition (CVD).[9,10] However, conventional CVD of tungsten using silane or hydrogen reduction of $WF_6$ cannot deposit W on oxides at temperatures below 400°C.[11] Although tungsten can be forced directly onto $SiO_2$ surfaces at temperatures above 400°C, the resulting films possess β-type structures with high resistivity[12] and tend to peel off because of poor adhesion to the $SiO_2$. In this study, we developed a new process, in which CVD of tungsten was employed to deposit W on a thin sacrificial poly-Si layer deposited on a gate oxide prior to CVD of the W itself. The natural self-limiting Si consumption property of the chemical vapor deposition of tungsten,[13] the so-called Si reduction reaction, will cause the thin sacrificial poly-Si layer to be consumed, so that a nearly pure W metal-gate MOS capacitor will result at the low deposition temperature of 300°C. We introduce the first tungsten metal gate (the poly-Si layer is completely consumed) MOS capacitor with the tungsten-gate formed by CVD process; this differs from conventional tungsten-polycide gates[14] and tungsten/poly-Si gate MOS capacitors.[15] Our MOS capacitors are superior to sputter-deposited W gate capacitors with respect to MOS device applications.

## Experimental

Samples were fabricated on (100) oriented p-type Si wafers. After initial RCA cleaning, 10 nm gate oxides were thermally grown in dry oxygen ambient at 925°C, followed by deposition of poly-Si layers of different thicknesses. Tungsten films of 200 nm thickness were then deposited using a CVD process via silane reduction of $WF_6$ under the following conditions: substrate temperature 300°C, total gas pressure 100 mTorr, $WF_6$ flow rate 20 sccm, $SiH_4$ flow rate 10 sccm, and $H_2$ carrier-gas flow rate 1000 sccm. For comparison purposes, sputtered-W-gate capacitors and conventional $n^+$-poly-Si-gate capacitors were also fabricated. For the sputtered-W-gate capacitors, the W gate was deposited directly on the gate oxide using dc magnetron sputtering in Ar ambient at a pressure of 8 mTorr and a deposition rate of 3 nm/min. For the conventional $n^+$-poly-Si-gate capacitors, the poly-Si gate was 300 nm thick and was doped with $POCl_3$ at 950°C for 35 min. The completed W-gate and polygate capacitors were treated with 60 s rapid thermal annealing (RTA) in $N_2$ ambient at temperatures ranging from 600 to 1000°C. The poly-Si consumption thickness of the tungsten CVD process was measured using cross-sectional transmission electron microscopy (TEM). The electrical characteristics of the MOS capacitors were evaluated by C-V and I-V measurements. Stress in the W film was measured using a Tencor FLX-2320 thin-film stress measurement device.

## Results and Discussion

Figure 1 shows the proposed process flow. The chemical vapor deposited tungsten film is easily deposited on the poly-Si surface at 300°C. Figure 2 shows cross-sectional TEM photographs of W gates with poly-Si layers of different thicknesses prior to CVD of tungsten: the polysilicon layer thickness is 45 nm (a) and 25 nm (b). The poly-Si was

* Electrochemical Society Active Member.

 © The Electrochemical Society, Inc.

Downloaded on 2014-04-28 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

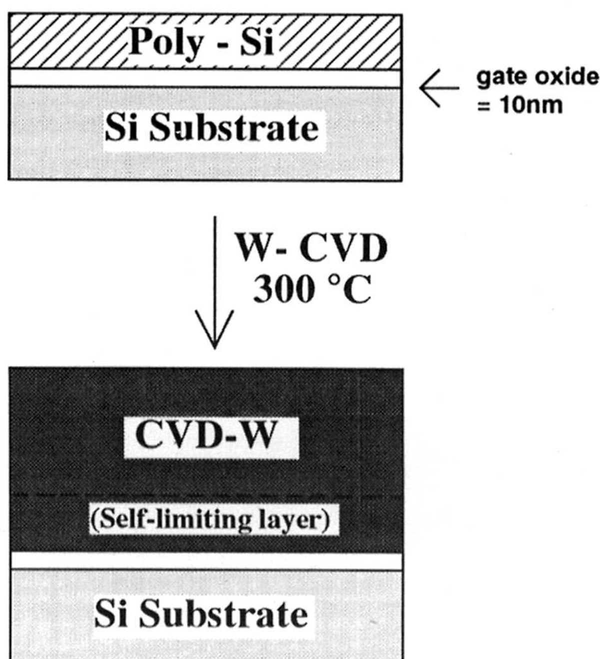


Fig. 1. Proposed process flow for CVD-W-gate MOS capacitor using a sacrificial poly-Si layer.

consumed at the initial stage by the tungsten CVD process and the amount of consumption remained constant for given a deposition condition irrespective of the deposited W film thickness. In this study, the sacrificial poly-Si layer was approximately 25 nm thick; thus, it nearly disappeared from samples upon which 25 nm poly-Si was deposited prior to the tungsten deposition.

Figure 3 shows the capacitance-voltage (C-V) characteristics of the CVD tungsten gate MOS capacitors with different sacrificial poly-Si layer thicknesses. MOS capacitors with 45 nm thick sacrificial layer of poly-Si yielded a clear discrepancy between high frequency and quasi-static C-V curves in accumulation mode, as shown in Fig. 3a; this discrepancy is attributable to the high-resistivity undoped poly-Si layer remaining after CVD. MOS capacitors started with 25 nm thick poly-Si sacrificial layers had a negligible discrepancy between their high frequency and quasi-static C-V curves in accumulation mode due to residual poly-Si, as shown in Fig. 3b. Furthermore, any residual poly-Si was later consumed by $WSi_x$ formation during the subsequent thermal annealing.

Figure 4 shows the sheet resistance ($R_s$) *vs.* annealing temperature for the W/poly-Si/$SiO_2$/Si samples with different initial poly-Si thicknesses. Samples with 45 or 30 nm thick initial poly-Si layers showed increased $R_s$ after annealing at 600°C, presumbly due to transformation of W into the $WSi_x$ phase ($1 < x < 2$). The $WSi_x$ phase formed at temperatures up to 600°C has a hexagonal structure; however, this changes to a lower resistivity tetragonal structure at temperatures above 600°C. [16] Thus, the sheet resistance of the samples decreased after annealing at temperatures above 600°C. Since samples with 45 nm thick initial poly-Si layers presumably consumed more tungsten during $WSi_x$ formation than those with 30 nm thick initial poly-Si layers, the samples with 45 nm thick poly-Si layers showed higher $R_s$ values. Samples with initial poly-Si layer 25 nm thick had no poly-Si remaining after CVD of tungsten and pure tungsten gate MOS structures were obtained. Annealing of these samples therefore

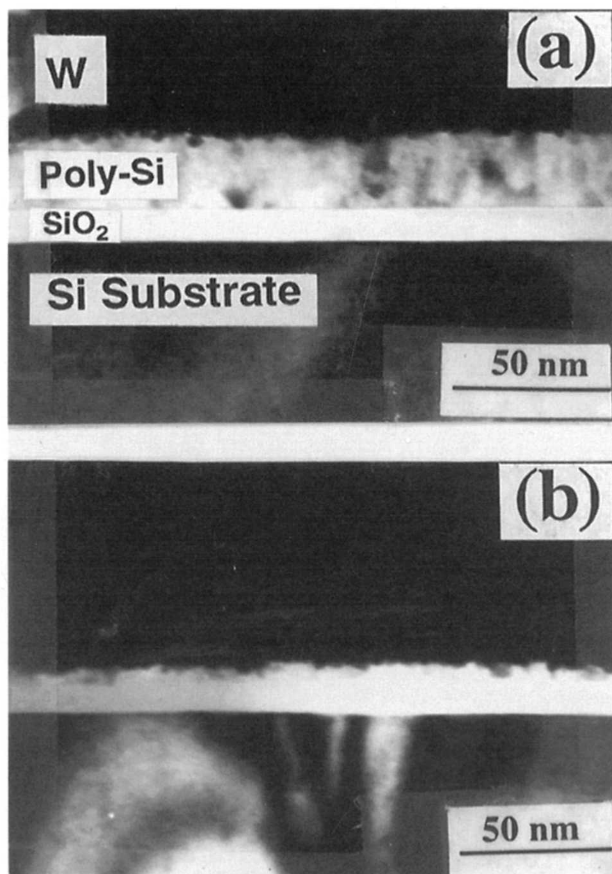


Fig. 2. Cross-sectional TEM photographs of CVD-W films deposited on (a) 45 nm poly-Si/10 nm $SiO_2$/Si and (b) 25 nm poly-Si/10 nm $SiO_2$/Si substrates.

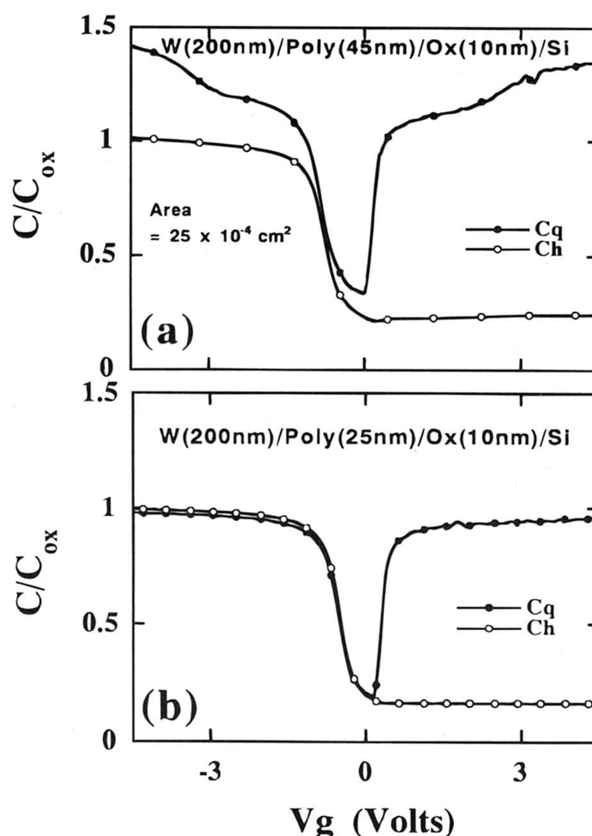


Fig. 3. Capacitance-voltage characteristics of the CVD-W-gate MOS capacitors with initial poly-Si sacrificial layer of (a) 45 and (b) 25 nm thickness prior to CVD of W.

Downloaded on 2014-04-28 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

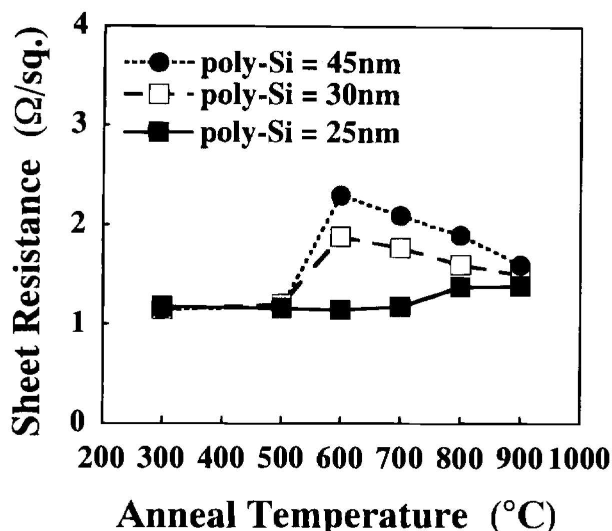


Fig. 4. Sheet resistance *vs.* annealing temperature for W/(poly-Si)/$SiO_2$/Si samples with various initial poly-Si thicknesses.

involved no W silicide formation, and the sheet resistance correlation to the annealing temperature differed from samples that had thicker initial poly-Si layers. The x-ray diffraction (XRD) spectra of these samples after RTA annealing at 600, 700, and 800°C are shown in Fig. 5. The (110) and (200) W signals indicate that the samples were low resistivity α-W phase and remained unchanged even after annealing at the temperature of 800°C. No $WSi_x$ signal was detected for these samples.

Dielectric strength of the W gate MOS capacitors was also investigated. Figure 6 shows the distribution of the dielectric breakdown fields for the CVD tungsten-gate and the sputtered-tungsten-gate MOS capacitors, as well as the $n^+$-poly-Si-gate capacitors. It can be seen that the average breakdown field of the CVD-tungsten-gate MOS capacitors is comparable with those of the sputtered-W-gate and $n^+$-poly-Si gate MOS capacitors. Charge-to-breakdown ($Q_{bd}$) was measured using constant-current stress on the 100 × 100 μm capacitors at a current density of 10 mA/$cm^2$. Figure 7 shows the Weibull plots of charge-

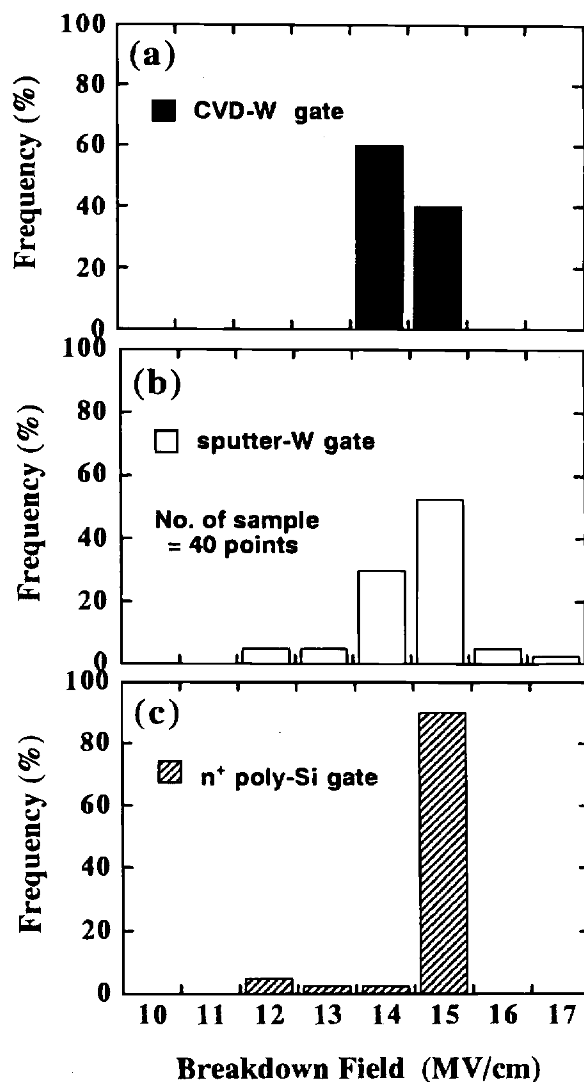


Fig. 6. Dielectric breakdown field distribution for the MOS capacitors with CVD-W, sputtered-W, and $n^+$-poly-Si electrodes; gate oxide thickness is 10 nm.

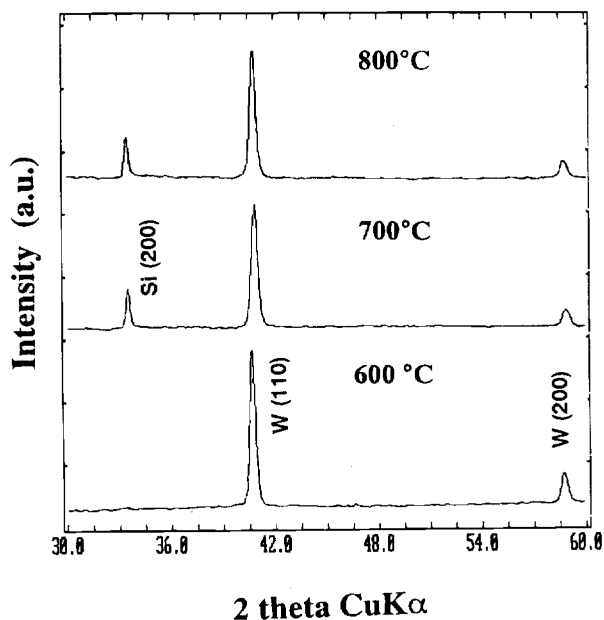


Fig. 5. XRD spectra of the RTA annealed CVD-W-gate MOS capacitors.

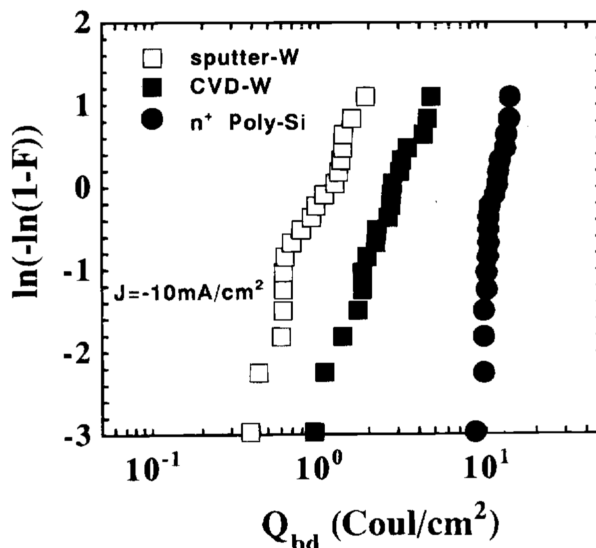


Fig. 7. Weibull plots of charge-to-breakdown ($Q_{bd}$) for the MOS capacitors with CVD-W, sputtered-W, and $n^+$-poly-Si electrodes; gate oxide thickness is 10 nm.

Downloaded on 2014-04-28 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

to-breakdown ($Q_{bd}$) for the CVD-tungsten-, sputtered-tungsten-, and n$^+$-poly-Si-gate MOS capacitors. Although the $Q_{bd}$ of the CVD-tungsten-gate capacitor is lower than that of the conventional n$^+$-poly-Si-gate capacitors, it is much larger than that of the sputtered-tungsten gate capacitors. This is presumably due to the large film stress of the sputtered-W-gate, which was found to be $1 \times 10^{10}$ dyn/cm$^2$. Large stress tends to induce a high interface state charge density ($Q_{it}$) and fixed-oxide charge density ($Q_f$).[17] Thus, in order to maintain a constant current injection, the gate voltage must be increased,which leads to earlier breakdown of the oxide dielectric.

Figure 8 shows the flatband voltage ($V_{FB}$) plotted against annealing temperature for the CVD-tungsten-, sputtered-tungsten-, and n$^+$-poly-Si-gate MOS capacitors. The $V_{FB}$ of the CVD-tungsten-gate capacitor was $-0.32$ V (after post-metallization sintering at 400°C), and only a slight change of 0.12 V in $V_{FB}$ occurred over a wide range of annealing temperatures up to 1000°C. The slight difference in flatband voltage ($V_{FB}$) between the CVD-tungsten-gate and sputtered-tungsten-gate MOS capacitors was presumably due to the discrepancy of work function between the CVD and sputtered tungsten. Table I gives a comparison of characteristics between the CVD-tungsten-gate and sputtered-tungsten-gate MOS capacitors. The CVD-tungsten films showed an α-type structure, as revealed by x-ray diffraction analysis, and had a low resistivity of 12.5 μΩ cm, compared with a resistivity of more than 46 μΩ cm for the sputtered-tungsten films. The initial stress of the CVD-tungsten film was tensile, and lower than that of the sputtered-tungsten film, which was compressively stressed. The midgap interface state density ($D_{it}$) of the CVD-tungsten-gate MOS capacitor was found to be about $10^{10}$ eV$^{-1}$ cm$^{-2}$, which was lower than that of the sputtered-tungsten-gate MOS by one order of magnitude. The large film stress of the sputtered-tungsten-gate capacitor apparently induced a large number of interface trap states. Flatband voltage variations of the CVD-tungsten-gate capacitors and the sputtered-tungsten-gate capacitors are comparable over a wide range of annealing temperatures up to 1000°C.

## Conclusion

A new CVD-tungsten-gate MOS process has been proposed. After an appropriate thickness of sacrificial poly-Si layer has been deposited on the gate oxide, W film can easily be deposited using the CVD process at low temperatures. The chemical vapor deposition of tungsten results in complete consumption of the sacrifical poly-Si layer, leading to a nearly pure tungsten-gate MOS. Compared with sputtered-tungsten-gate MOS capacitors, the proposed MOS capacitor has a lower resistivity gate, lower intrinsic tungsten film stress, lower interface state density ($D_{it}$), and higher charge-to-breakdown ($Q_{bd}$). These basic characteristics indicate that the proposed MOS capacitors show great promise for future VLSI application.

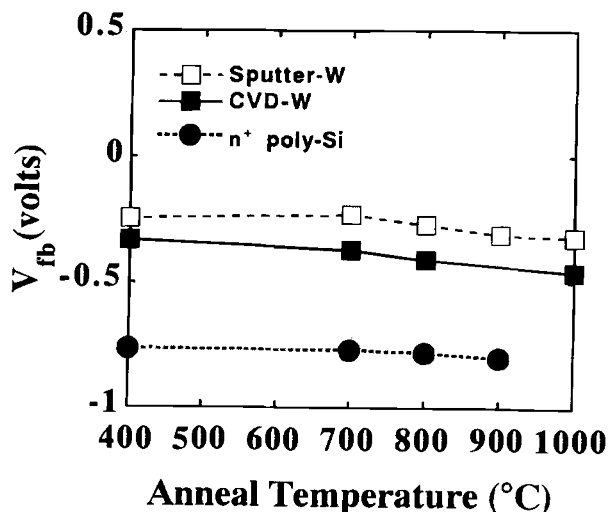


**Fig. 8. Flatband voltage vs. annealing temperature for the MOS capacitors with CVD-W, sputtered-W, and n$^+$-poly Si electrodes; gate oxide thickness is 10 nm.**

**Table I. Characteristics of MOS capacitors with chemical-vapor deposited-W and sputtered-W electrodes; gate oxide thickness is 10 nm.**

| | CVD-W-gate MOS | Sputtered-W-gate MOS |
|---|---|---|
| W film resistivity (μΩ cm) | 12.5 | 46.7 |
| W film stress (dyne/cm$^2$) | $5.4 \times 10^9$ (tensile) | $\sim 1 \times 10^{10}$ (compressive) |
| $D_{it}$ (eV cm$^2$)$^{-1}$ | $\sim 1.0 \times 10^{10}$ | $2 \times 10^{11}$ |
| $\Delta V_{FB}$ (V) | 0.12 | 0.09 |

Gate oxide = 10 nm.
$D_{it}$: interface state density.
$\Delta V_{FB}$: flatband voltage variation after anneal at temperatures up to 1000°C.

## Acknowledgments

This work was supported by National Science Council (ROC) under Contract No. NSC84-2622-E009-007-1.

Manuscript submitted Nov. 1, 1995; revised manuscript received Sept. 14, 1996.

*National Chiao Tung University assisted in meeting the publcation costs of this article.*

REFERENCE

1. G. J. Hu and R. H. Bruce, *IEEE Trans. Electron Devices*, **ED-32**, 584 (1985).
2. J. Y.-C. Sun, C. Wong, Y. Taur, and C.-H. Hsu, in *Digest of Technical Papers, 1989 Symposium* on VLSI Technology, p. 17, Japan Society of Applied Physics, Kyoto, Japan (1989).
3. J. R. Pfiester, F. K. Baker, T. C. Mele, H.-H. Tseng, P. J. Tobin, J. D. Hayden, J. M. Miller, C. D. Gunderson, and L. C. Parrillo, *IEEE Trans. Electron Devices*, **ED-37**, 2312 (1990).
4. M. Ishihara, T. Matsumoto, S. Shimizu, K. Mitsusada, and K. Shimohigashi, in *Digest of Technical Papers, 1982 IEEE International Solid-State Circuits Conference*, p. 74, IEEE, Piscataway, NJ (1982).
5. F. Mohammadi and K. C. Saraswat, *IEEE Electron Device Lett.*, **EDL-2**, 24 (1981).
6. T. Mochizuki, T. Tsumimaru, M. Kashiwagi, and Y. Nishi, *IEEE Trans. Electron Devices*, **ED-27**, 1431 (1980).
7. N. Yamamoto, H. Kume, S. Iwata, K. Yagi, N. Kobayashi, N. Mori, and H. Miyazaki, *This Journal*, **133**, 401 (1986).
8. N. Kobayashi, S. Iwata, N. Yamamoto, and N. Hara, in *Workshop on Tungsten and Other Refractory Metals for VLSI Application*, p. 159, MRS, Pittsburgh, PA (1987).
9. J. S. Hong, Y. T. Kim, and S. K. Min, *J. Appl. Phys.*, **70**, 2366 (1991).
10. H. Matsuhashi, S. Nishikawa, and S. Ohno, *Jpn. J. Appl. Phys.*, **27**, L2161 (1988).
11. M. L. Green and R. V. Levy, *This Journal*, **132**, 1243 (1985).
12. T. I. Kamins, D. R. Broadbury, T. R. Cass, S. S. Laderman, and G. A. Reid, *ibid.*, **133**, 2555 (1986).
13. E. K. Broadbent and C. L. Ramiller, *ibid.*, **131**, 1427 (1984).
14. B. L. Crowder, in *Workshop on Tungsten and Other Refractory Metals for VLSI Application*, p. 3, MRS, Pittsburgh, PA (1988).
15. J. G. Black, D. J. Ehrlish, J. H. C. Sedlacek, A. D. Feinerman, and H. H. Busta, *IEEE Electron Device Lett.*, **EDL-7**, 422 (1986).
16. F. M. d'Heurle, F. K. LeGoues, R. Joshi, and I. Suni, *Appl. Phys. Lett.*, **48**, 332 (1986).
17. H. Matsuhashi, S. Nishikawa, and S. Ohno, *Jpn. J. Appl. Phys.*, **28**, L2309 (1989).

Downloaded on 2014-04-28 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).