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Characterization of poly-Si TFT variation using interdigitated method

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ABSTRACT

In this paper, the device variation characteristic of poly-Si TFTs is statistically investigated. First the variation of devices is examined with respect to different device distance. It is found that the device variation would exhibit similar behavior for different device distance. Then, in order to study the method to suppress device variation, the interdigitated layout is adopted. It is found that though the variation behavior of the poly-Si TFTs is much more serious and complicated than MOSFETs, the law of area can still be utilized to describe the variation behavior in the interdigitated layout. The fitting parameters in law of area can provide insights for understanding the intrinsic variation behavior for poly-Si TFTs and the discussion about the variation for the device with various channel width is provided. The variation behavior of poly-Si TFTs is then compared with amorphous silicon TFTs and single crystal silicon MOSFETs. The impacts of poly-Si TFT variation on circuit design and performance is also discussed.

1. Introduction

Low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs), owing to its better crystallinity, have higher device mobility than amorphous silicon TFTs [1–2]. Its higher driving ability enables the capability of forming both the in-pixel switches and the peripheral circuits for the display system all with the poly-silicon technology [3]. This would be much beneficial to cut the cost to integrate the peripheral circuits onto the panel with poly-Si TFTs in fabricating the advanced display, while the reliability and module weight can be relieved at the same time. Since the device mobility can be as high as 100 cm^2/V s, several value-added functions, such as touch panel and sensor circuit, are also expected to be realized with the poly-Si TFTs [4–6].

However, poly-Si TFTs are found to suffer from serious variation effect, which could come from the diverse grain structure in the poly-Si film. Devices from predominant process condition still exhibit electrical behavior variation. Though the device structure is similar to metal–oxide–silicon field effect transistors (MOSFETs), the variation behaviors of TFTs are much worse than those of MOSFETs. Though these years several novel recrystallization techniques have been proposed for poly-Si film, the variation of device behavior still exists and there are very few papers discussing this issue [7–10]. Nevertheless, in real applications the variation of the device parameter will establish extra difficulties for designers. For example, for the display applications, as the poly-Si TFTs are mostly applied in, the device variation would lead to the varying circuit performance and non-uniformity of display image. Therefore, in order to correctly evaluate the performance of poly-Si TFTs in real applications, the variation behavior of the devices should be studied in detail. In previous work, we had characterized the variation behavior of poly-Si TFTs using the proposed layout [11]. It is discovered that the variation behavior can be decoupled as "long-range variation" and "micro variation," which respectively correspond to the process control issue and the behavior of poly-Si film quality. In this work, the behavior of micro variation is further examined with respect to different device distance. Then, in order to suppress the micro variation behavior, the interdigitated layout is adopted and the parameter variation for different fingers in interdigitated layout is investigated. The law of area is then used to describe the standard deviation of the devices in different finger numbers of the interdigitated arrangement. The variation behavior with respect to different device width is also discussed. Finally, the device variation for the devices with different crystallinity is discussed using the interdigitated layout. The impact of micro variation of poly-Si TFTs on circuit design and performance would also be discussed.

2. Experimental

The process flow of TFTs is described below. Top gate poly-Si TFTs with width/length dimension of 20 μm/5 μm were fabricated using low temperature process. Firstly, the buffer oxide and a-Si:H

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films with thickness of 50 nm were deposited on glass substrates with PECVD. The samples were then put in the oven for dehydrogenation. The XeCl excimer laser of wavelength 308 nm and energy density of 400 mJ/cm^2 was applied. The laser scanned the a-Si:H film with the beam width of 4 mm and 98% overlap to recrystallize the a-Si:H film to poly-Si. The average grain size is about 0.4 um. The poly-Si film is then channel-implanted with BF_3 with low energy and low dosage for V_{TH} adjustment. After poly-Si active area definition, 100 nm SiO_2 was deposited with PECVD as the gate insulator. Next, the metal gate was formed by sputter and then defined. For n-type devices, the lightly doped drain (LDD) region and the n^+ source/drain doping were formed by PH_3 implantation with dosage 2×10^{13} cm^{-2} and 2×10^{15} cm^{-2} of PH_3, respectively. The LDD implantation was self-aligned and the n^+ regions were defined with a separate mask. The LDD structure was not used on p-type devices. The p^+ source/drain doping was done by B_2H_6 self-align implantation with a dosage of 2×10^{15} cm^{-2}. Then, the interlayer of SiN_x was deposited. Subsequently, the rapid thermal annealing was conducted to activate the dopants. Meanwhile, the poly-Si film was hydrogenated. Finally, the contact hole formation and metallization were performed to complete the fabrication work.

In this work the threshold voltage is determined from the commonly-adopted constant current method, which extracts threshold voltage V_{TH} from the gate voltage at the normalized drain current $I_D = 10$ nA for $V_D = 0.1$ V. The method to extract the field effect mobility is to find the maximum value of the transconductance at $V_D = 0.1$ V and divide it with the normalized channel width, length and gate insulator capacitance.

3. Results and discussion

3.1. Micro variation for poly-Si TFTs

For MOSFETs, the device variation can be characterized by the correlation distance, which is defined as the distance how the process disturbance or fabrication fluctuations affect the device performance [12]. For example, if the correlation distance of the factor is larger than the smallest device distance, such as the film thickness fluctuation across the wafer surface, the factor would affect all the devices over a specific region. In this case, the devices located at longer distance could be more affected by this long-range variation than the devices placed close to each other. On the other hand, if this distance of the factor is around the distance between the nearest devices, such as the charge trapped in the gate oxide layer, the effect of the disturbance would vary from device to device. In previous work, similar classification technique is followed and the variation for poly-Si TFTs is found to be able to be classified as "long-range variation" and "micro variation" and the way to decouple them is by finding the parameter difference between the nearest devices, as shown in Fig. 1 [11]. The possible factors forming the long-range and micro variation are given in Table 1. One additional factor that the poly-Si TFTs have besides MOSFETs is that there are grains in the active region and these grains are recrystallized with laser pulse, which is much different from the method of the active layer formation of MOSFETs. During the poly-Si film preparation, there could be laser energy fluctuation and recrystallization site variations, making the grains have varying size and electrical behavior. Since there are around hundreds of grains in the channel region, the grain-to-grain electrical performance variation could then lead to device-to-device variation and thus this could be attributed to the micro variation, which is yet unclear for poly-Si TFTs.

While the long-range variation could be mainly attributed to the process control issue, the micro variation is believed to be closely related to the intrinsic film quality of poly-Si film. In other words, with the improving process control technique, the micro variation could still exist and might gradually become the main variation source. In that sense the study for the micro variation behavior from point to point would be of practical interest. Fig. 2 shows the standard deviation for the threshold voltage (V_{TH}) and mobility (Mu) difference between two devices for different device distance. Around 500 devices using the "crosstie layout" are measured and their parameters are extracted [11]. Their initial device parameters are shown in Table 2. As referred to Fig. 2, it is discovered that the standard variation values for V_{TH} difference for both n-type and p-type devices are all around 20–30 mV and show no apparent dependence on device distance. Similar behavior can be found for Mu difference for both n-type and p-type devices and for different device distances. The standard deviation values for Mu are all around 2 cm^2/V s for different device distance. This reveals that the micro variation is imposing similar effects for device performance for different positions on the film, which can be attributed to the uniform grain distribution in the poly-Si film. This finding also gives the information that with the aforementioned method for decoupling the variation, the variation behavior may be feasibly modeled on different sites and the amounts for micro variation are around 30 mV in V_{TH} and 2 cm^2/V s in mobility.

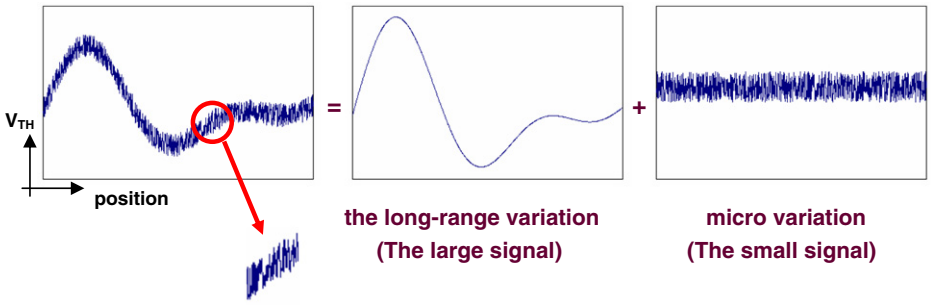

Fig. 1. The figure illustrating the superposition of long-range variation and micro variation.

Table 1
Possible factors to long-range variation and micro variation

	Long-range variation	Micro variation
Effect on device parameters	Common trend over a range	Random fluctuation among devices
Possible factors	Film thickness, ion implantation dosage, channel length, LDD length	Defect sites, defect density, activation efficiency, grain size variation

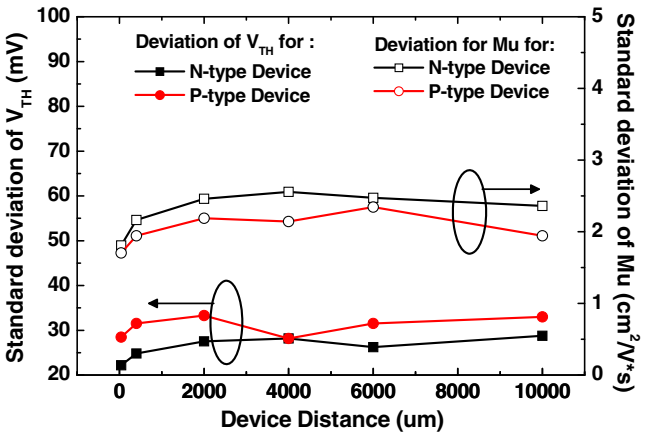

Fig. 2. The V_{TH} and mobility variation for the devices with different device distances.

Table 2
The mean value and the standard deviation of the measured device parameter

N-type	V_{TH} (V)	Mu (cm^2/V s)
Average	1.64	66.33
Standard deviation	0.019	1.7
P-type	V_{TH} (V)	Mu (cm^2/V s)
Average	−2.39	79.08
Standard deviation	0.023	1.608

3.2. Variation behavior in the interdigitated arrangement

Typically, the dimension of the transistors in analog circuits is larger than that in digital circuits. On the other hand, signal in the analog circuits may require higher precision than that in the digital circuits since the latter may only need to distinguish the high or low signal of the applied voltage. In certain analog circuit, a very high matching behavior between devices is desired. In addition to the simplest structure, the interdigitated layout, several layout techniques with the more complicated structure are proposed to reach the high matching behavior between the devices, such as common centroid layout technique, and the dummy device technique [13,14]. In the following section, therefore, only the variation behavior of poly-Si TFTs in the interdigitated layout method is discussed. Fig. 3 shows the idea of interdigitated layout. The idea is that the devices are placed in a cross-over form and the finger number represents how many devices are connected to each other. For example, two-finger interdigitated layout means that the number N_{TH} and $(N+2)_{TH}$ devices are electrically connected, and the same for the $(N+1)_{TH}$ and $(N+3)_{TH}$ devices.

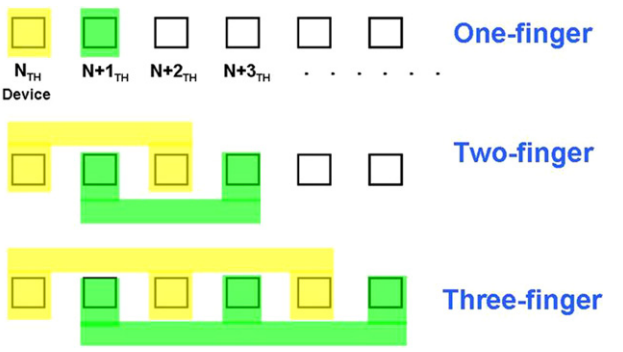

Fig. 3. The interdigitated connection discussed in this work with different finger numbers.

The V_{TH} variation behaviors between the interdigitated devices with different fingers for n-type devices are shown in Fig. 4, while those behaviors of the p-type devices are shown in Fig. 5. On the other hand, the mobility variation behaviors of the n-type and p-type devices for different fingers of interdigit are, respectively shown in Figs. 6 and 7. The values of the standard deviation for these distributions with different interdigit finger numbers are given in Table 3. It can be observed that, for both V_{TH} and mobility and for both n-type and p-type devices, the distribution is becoming more centralized and the profile becomes narrower as the finger number increases, which reveals that the variation of these parameters decreases with interdigit finger number. Besides, the center of these distributions move closer to zero as the finger number increases. Gaussian distribution is used to fit the profile of the parameter variation in the interdigitated layout and the coefficient of determination, as shown for each parameter in the Figs. 4–7, increases with finger number. This reveals that though the true profile of micro variation is not clarified yet, the parameter variation of the poly-Si TFTs is essentially approaching Gaussian distribution in the interdigitated layout method as the finger number increases.

3.3. Modeling the variation behavior in the interdigitated layout

Fig. 8a shows the standard deviation value of V_{TH} with different interdigit finger numbers, while Fig. 8b shows that of mobility. It

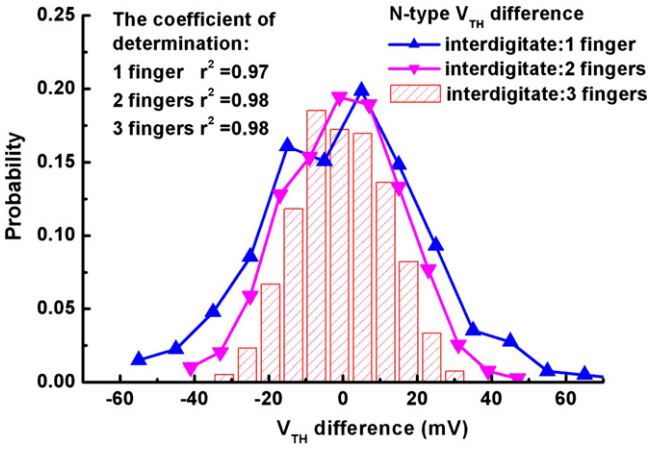

Fig. 4. The threshold voltage difference distribution of n-type devices with the interdigitated method with different finger numbers.

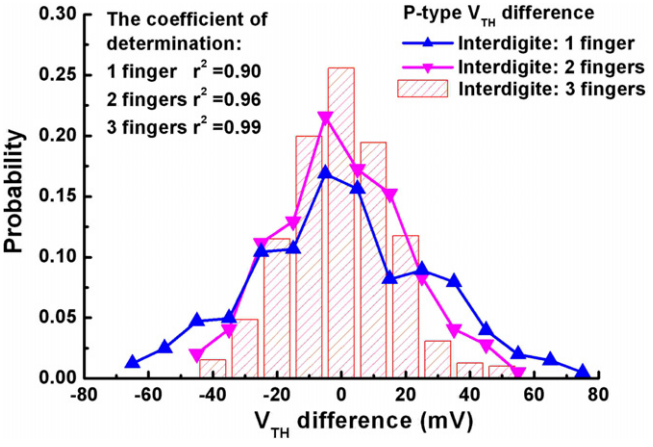

Fig. 5. The threshold voltage difference distribution of p-type devices with the interdigitated method with different finger numbers.

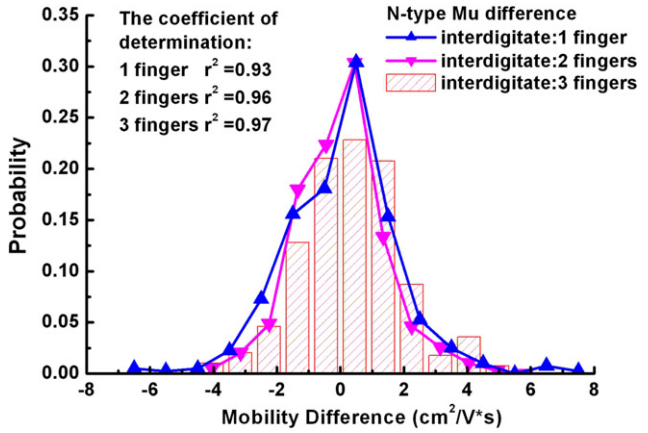

Fig. 6. The mobility difference distribution of n-type devices with the interdigitated method with different finger numbers.

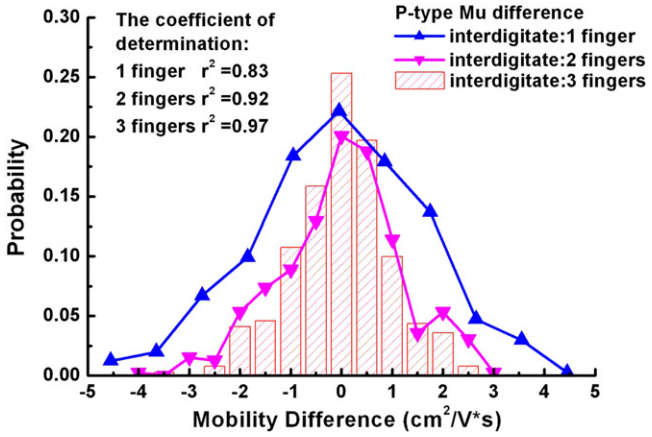

Fig. 7. The mobility difference distribution of p-type devices with the interdigitated method with different finger numbers.

can be observed that both for n-type and p-type curves follow the same trend and the difference between the n-type and p-type devices is kept a constant gap. Besides, it is discovered that the micro variation of V_{TH} of p-type device is larger than that of n-type devices in the interdigitated arrangement, which can be attributed to the BF_3 channel implant for V_{TH} adjustment. These implanted boron atoms could form the shallow state near the valence band in the poly-Si bandgap and may then turn out to be a variation factor for the p-type devices [15]. Besides, it is also found that the mobility variation of n-type device is larger than that of p-type, which can be attributed to the activation and uniformity of the LDD region for the n-type devices.

Table 3
The standard deviation value for V_{TH} and mobility with different interdigit finger number

Device type standard deviation	N-type		P-type	
	V_{TH} (mV)	Mu (cm^2/V s)	V_{TH} (mV)	Mu (cm^2/V s)
Finger number				
One-finger	22.2	1.8108	28.49	1.7043
Two-finger	15.4	1.3619	20.33	1.1776
Three-finger	12.2	1.1585	16.21	0.9579
Four-finger	10.6	1.0312	15.23	0.8344
Five-finger	8.7	0.9765	13.56	0.7055
Six-finger	8.2	0.9482	12.44	0.6465

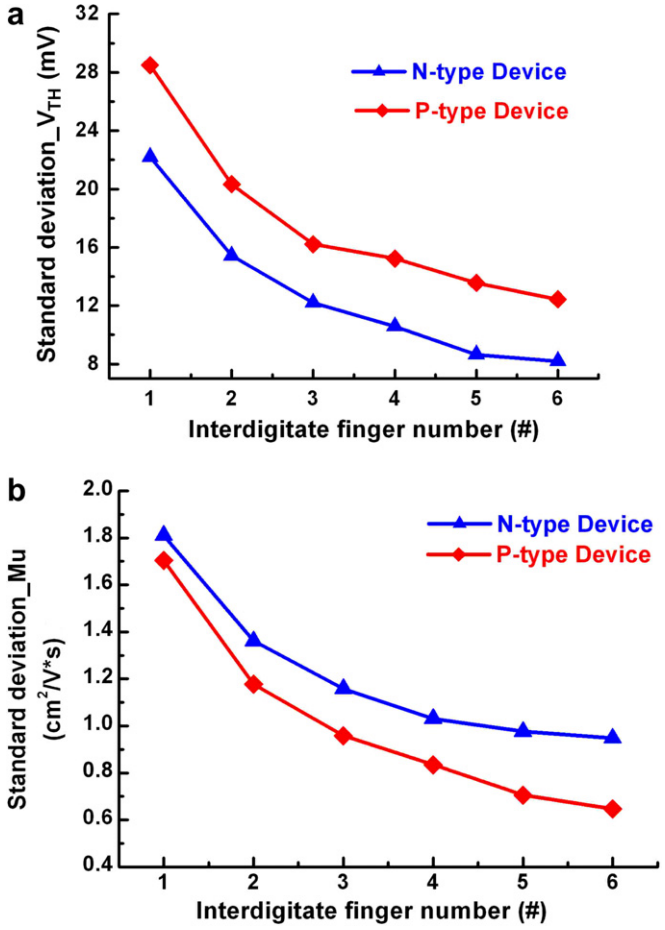

Fig. 8. The standard deviation of the device parameter with interdigit finger number for (a) V_{TH} and (b) mobility.

The interdigitated layout is essentially extending the device width and therefore the well-known "law of area" may be used to model the variation behavior. The "law of area" states that the device parameter mismatch is inversely proportional to the root of the channel area [16]. This indicates that the larger device dimension is, the less variation these devices would suffer. This also means that the variation behavior would be worse in the small dimension devices than that in the large dimension devices. Owing to the randomly-distributed grains in the poly-Si film, the parameter variation of poly-Si TFTs could show a different behavior than MOSFETs. Fig. 9a shows the V_{TH} variation for different finger numbers and the fitting curve, while Fig. 9b shows that of mobility variation. The "law of area" equation used in this work is given as:

$y = a + \frac{b}{\sqrt{x}}$, where a and b are the fitting parameters.

The fitting parameters and the coefficients of determination (r^2) are given in Table 4. Referred to Fig. 9, it can be found that for both device parameters the law of area can well fit the curves with very high accuracy, where the coefficients of determination are all above 0.99. This indicates that though with the presence of worse micro variation behavior as compared with MOSFETs, the variation behavior of the interdigitated poly-Si TFTs can still be well described with law of area.

Referred to Table 4, the fitting parameter a and b, respectively represent how the variation would be as the device width is very large and how the variation would worsen as the device width shrinks. For V_{TH}, it is discovered that parameter a is the same for both n-type and p-type devices, meaning that the variation of the large width device would show similar V_{TH} variation behavior for n-type and p-type devices. However, the fitting parameter b for

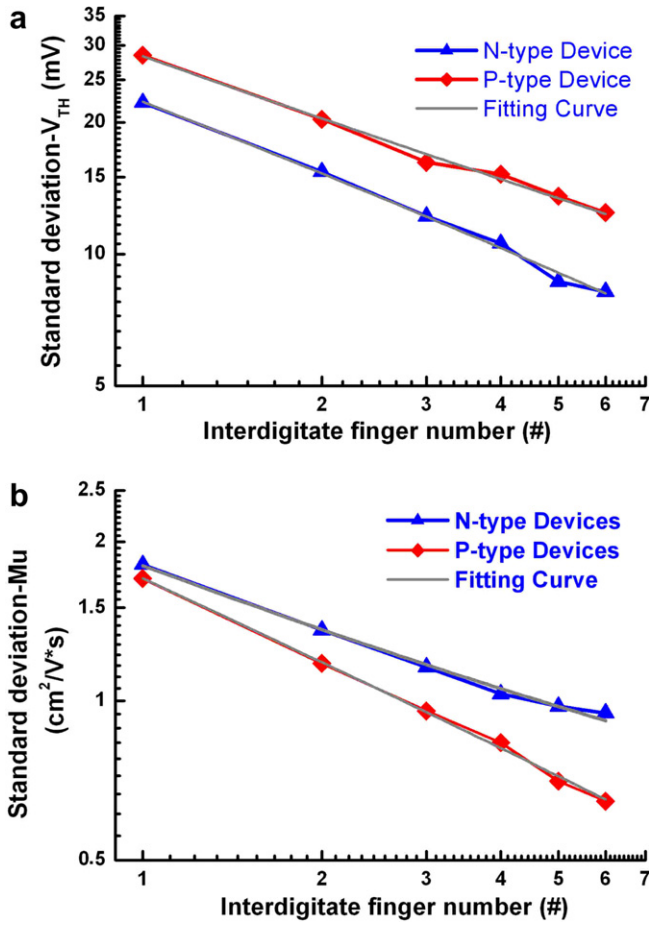

Fig. 9. The log-scale standard deviation of the device parameter with interdigit finger number and the fitting curve for (a) V_{TH} and (b) mobility.

Table 4
The fitting parameters and the coefficient of determination (r^2) for fitting the standard deviation of interdigitated layout of poly-Si TFTs

Device	Fitness (r^2)	Fitting parameter "a"	Fitting parameter "b"
V_{TH} variation			
N-type	0.9981	1.7 (mV)	23.9
P-type	0.9959	1.7 (mV)	26.9
Mu variation			
N-type	0.9968	0.3081	1.4939
P-type	0.9991	0.0765	1.7817

p-type device is slightly larger than that for n-type device, meaning that the aforementioned channel doping effect could gradually become dominant as the device width decreases. On the other hand, for mobility, it is found that the parameter *a* for n-type device is much larger than that for p-type device. This reveals that, as the device width increases, the grain number and electrical behavior variation in the channel region may be gradually averaged and thus the LDD variation may be the main factor responsible for the larger mobility variation, making the mobility variation in n-type devices larger than that in p-type devices. However, as the device width becomes smaller, the number of grains in the channel could greatly differ from each other and thus the value of mobility variation for both n-type and p-type devices would slowly become similar and the effect of LDD variation may be less important. This finding of device variation behavior with respect to different device width could be of great help in realizing and modeling of device variation and can also assist designers to properly evaluate the device parameter variation for poly-Si TFTs with different dimensions.

3.4. Comparing the variation behavior in the interdigitated layout for different crystallinity behavior

In previous section, the variation behavior of poly-Si TFTs is discussed using the interdigitated layout. For further studying the variation behavior, it would be of practical interest to study the variation behavior of the silicon-based devices with different crystallinity behavior. Fig. 10 shows the standard deviation for V_{TH} for different type of devices. More than 400 crosstie devices of amorphous silicon TFTs are measured and statistically summarized. The amorphous silicon TFT is of the conventional inverted stagger structure. The data of the single crystal silicon is referenced from Chee Lin Yum in Bachelor's thesis on Electrical Engineering [17]. The fitting parameters and the corresponding coefficients of determination (r^2) are given in Table 5.

Referred to Table 5, it is shown that the coefficients of determination are all above 0.7, indicating that the law of area can be used for describing the variation for the devices with different grain structures. For fitting parameter a, it is discovered that the parameter for single crystal silicon MOSFETs is very small, meaning that the variation would be eliminated for the very large width devices. In addition, the parameter a for amorphous silicon TFT is around four times larger than that of poly-Si TFTs. This reveals that the micro variation behavior of amorphous TFT may be worse than that in poly-Si TFTs, which may result from the micro structure and film thickness fluctuation of the amorphous silicon film.

For the fitting parameter *b*, it is found that the variation of n-type poly-Si TFTs is ten times larger than n-type single crystal silicon MOSFETs. Furthermore, the parameter *b* of amorphous silicon TFTs is three times larger than that of n-type poly-Si TFTs. For p-type devices, the parameter *b* of poly-Si TFTs is one hundred times larger than that of single crystal silicon MOSFETs. Since parameter *b* can be viewed as the increase rate for device variation as the device width shrinks, it can be inferred that the variation of amorphous silicon TFT would be worse than that of poly-Si TFTs and the single crystal MOSFETs would exhibit slow increase of device variation as the device width decreases. This can be attributed to the micro structure and grain behavior of the silicon layer for the devices. The preparation of the single crystal silicon film takes long time in the high temperature environment (around 1000 °C). Silicon atoms may get enough energy and time to form the good bonding and crystallinity, therefore the structure of the silicon film

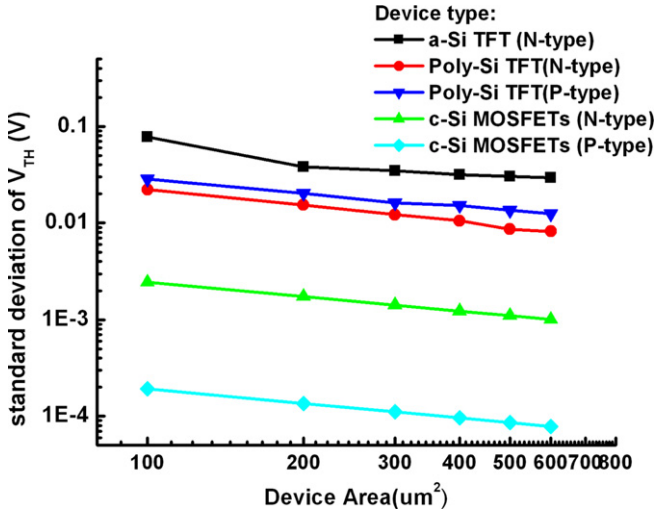

Fig. 10. The standard deviation of V_{TH} for different types of devices and for both n-type and p-type devices.

Table 5
The fitting parameters and the coefficient of determination (r^2) for fitting the standard deviation of interdigitated layout of various kinds of devices

Device type	Coefficient of determination (r^2)	Fitting parameter "a"	Fitting parameter "b"
a-Si TFT (N-type)	0.8913	7.9	796.1
Poly-Si TFT (N-type)	0.9981	1.7	239.4
Poly-Si TFT (P-type)	0.9959	1.7	269.6
c-Si MOSFET (N-type)	1	2.7E−4	24.6
c-Si MOSFET (P-type)	1	−9.0E−8	1.9

would be of good quality and uniformity. However, the film preparation for poly-Si film in this work is by using the excimer laser to recrystallize the deposited amorphous film and therefore the film structure may not be as good as that of the single crystal silicon film in MOSFETs. On the other hand, the preparation for amorphous film is just by PECVD deposition and there may be very small grains in the silicon film. Besides, in this work the amorphous silicon TFT is of the conventional bottom gate structure and film thickness variation of the amorphous silicon film may also results in device variation.

3.5. Impact of the variation behavior on circuit design and performance prediction

Owing to the higher device mobility, poly-Si TFTs are expected to replace bond ICs and form the circuits for some specific applications. From the viewpoint of circuit design, higher driving current of the poly-Si devices is desired. From the simple current equation, it means that the ratio of device width over length (W/L) should be higher to obtain the higher driving current without changing the process method. For poly-Si TFTs, it is reported that reducing the device length to around 2 μm will introduce serious short channel effect and that could result in the inaccuracy between the circuit design and the real device performance [18]. Another way to increase driving current is to enlarge the device width. An additional point for increasing the device width is that the larger channel width means that there are more grains in the channel region and the device variation behavior may be relieved. Therefore, in order to have higher driving current and lower variation issue, one option is to increase the width of poly-Si TFTs. However, from the above discussion, it is shown that even for the devices with large width, variation between devices can still exist and the amount is around 1.7 mV in V_{TH} and 0.3 cm^2/V s in device mobility. Though the variation can not be fully eliminated, for some applications, such as the pixel design in active matrix liquid crystal display (AMLCD), such variation behavior for large width device might still pass the 8 mV criteria in the grey level voltage definition of the 8-bit panel specification. However, for some circuits requiring high signal precision, such variation in device performance should be taken into consideration. Furthermore, for the pixel design in active matrix organic light emitting diode (AMOLED) driven with poly-Si TFTs, panel designers should design for such variation and the compensation methods may still be necessary for the high performance panels. The impact of this work is to provide the behavior of device variation for different device width and furthermore to give the amount of variation when the device width is very large. This would be helpful for circuit and panel designers in evaluating the variation behavior of poly-Si TFTs and designing for variation if necessary.

4. Conclusion

This work focuses on the characterization of variation behaviors of poly-Si TFTs. The micro variation of device parameters is found to exhibit similar behavior for different device distances. The interdigit method is then utilized to examine the micro variation behavior of the devices in different sets of arrangement. It is discovered that the parameter variation gradually resembles Gaussian distribution as the interdigit finger number increases. The law of area is adopted to describe the variation behavior and it is found that with the presence of larger micro variation the law of area can still fit the curve with a very high accuracy. Based on the fitting parameters of law of area, it is found that poly-Si devices will still suffer variation and the amount of variation is about 1.7 mV and 0.3 cm^2/V s in mobility. The law of area is also adopted to describe the variation behavior of amorphous silicon TFT and single crystal silicon MOSFTEs and it is found that the micro variation of amorphous silicon TFTs may be larger than that of poly-Si TFTs. The modeling would be helpful for the variation evaluation of the poly-Si TFTs with various device dimensions in the pixel design and analog circuit design in display electronics with poly-Si TFTs.

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