Design of low-voltage CMOS low-noise amplifier with image-rejection function

L.-S. Wei, H.-I. Wu and C.F. Jou

A new design is presented that combines a low-noise amplifier (LNA) with an on-chip filter instead of external filter to eliminate image signal based on TSMC 0.18 μm CMOS technology. The fully integrated 5.9 GHz LNA exhibits 15.2 dB gain, 3.2 dB noise figure, better than −15 dB input and output return loss, and −27 dB image rejection. The circuit operates at a supply voltage of 1 V and consumes only 6.1 mW power.

Introduction: For radio-frequency (RF) integrated circuit wireless receivers, the need for low-power and low-cost systems demands the use of CMOS technology to arrive at a single-chip solution. However, the image problem requires an off-chip filter. The image-rejection (IR) filter usually is an external component, such as a surface-acoustic wave filter. This kind of filter is often expensive and large, which increases power consumption and costs, and is thus not suitable for integration. For this purpose, research into LNA with IR technique has developed [1–3] and improved RF level of integration. In [1], the active notch filter, which provides the lowest dip of input impedance at image frequency, is implemented in the signal path of a cascode LNA circuit; thus the image signal will be connected to ground. However, the active filter will contribute extra power and noise, and in addition a stack of three stages needs higher supply voltage (3 V). In this Letter, we present a new design that employs the current-reuse technique with an LC tank at inter-stage to achieve simultaneously an IR function and a lower power dissipation than in [1–3]. From measured results, it successfully provides −27 dB IR while exhibiting comparable performance to the traditional current-reuse amplifiers.

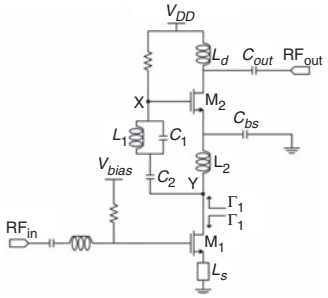

Fig. 1 *Circuit schematic of proposed LNA*

Circuit design: The schematic diagram of the proposed LNA is shown in Fig. 1. The supply voltage (V_{DD}) is 1 V and the bias voltage (V_{bias}) is 0.7 V. The circuit topology exploits the current-reuse technique, M_1 and M_2 transistors are a stack and use the same bias current and therefore the total power consumption is minimised. To achieve input impedance matching, only a small L_s value is required. This L_s value is done by layout of a small transmission line at M_1 source connected to ground, instead of using a spiral inductor component, so that area and cost can be saved. A simple LC network (L_d, C_{out}) is used to match the 50 Ω output impedance for measurement requirements. The passive IR filter is implemented at inter-stage and consumes no additional power compared with the active filter. The LC tank (L_1, C_1) is added and designed to resonate at image frequency so as to provide high impedance to reject the image. In the signal path as shown in Fig. 2*a*, the voltage ratio of node X to node Y, A_v, can be derived as

$$A_v \simeq \frac{1/sC_{in2}}{1/sC_{in2} + (1/sC_1//sL_1)} = \frac{s^2 + 1/L_1C_1}{s^2 + 1/L_1C_1(1 + C_{in2}/C_1)} \quad (1)$$

where C_{in2} is gate parasitic capacitance of M_2, which has small value (7 fF in this design) compared to the DC blocking capacitor C_2, thus C_2 is negligible in the analysis. From (1), the image and RF frequencies are located at zero and pole, respectively:

$$f_{image} = \frac{1}{2\pi\sqrt{L_1C_1}}$$

and

$$f_{RF} = \frac{1}{2\pi\sqrt{L_1C_1(1 + C_{in2}/C_1)}} \quad (2)$$

The RF signal is enhanced and the image signal is filtered out from node Y to node X. With design for small C_{in2}/C_1, the image signal can be set to close to the RF signal. In general, the quality factor Q of the on-chip integrated inductor is worse. To overcome this problem, the Q enhancement technique is proposed in this design. As shown in Fig. 2*b*, the input impedance of M_2 at high frequency can be expressed as

$$Z_{\text{in}} = r_{g2} - \frac{g_{m2}}{\omega^2 C_{gs2} C_{bs}} + \frac{1}{j\omega}\left(\frac{1}{C_{gs2}} + \frac{1}{C_{bs}}\right) \quad (3)$$

where C_{gs2} is the gate-to-source parasitic capacitance, and r_{g2} is the series gate parasitic resistance. Note that L_2 serving as an RF choke can be ignored at high frequency for simplicity. In (3) the second term on the right-hand side is negative resistance proportional to g_{m2}, and by adjusting the size of M_2, sufficient negative resistance can be generated to cancel out r_{g2} and the parasitic resistance of the on-chip inductor L_1. To verify the IR ability of the filter, the simulation result of A_v is shown in Fig. 3*a*. We can observe that the RF signal at 5.9 GHz passes through the filter and the image signal at 7.3 GHz is filtered out. In addition to rejecting the image signal, the filter is also used as the inter-stage matching. Fig. 3*b* shows that, at node Y, the simulated reflection coefficients Γ_1 and Γ_2 are approximately complex conjugate matching to achieve maximum power transformation.

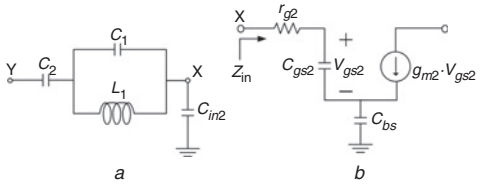

Fig. 2 *IR filter and small-signal equivalent circuit looking into gate of M_2*

a IR filter
b Equivalent circuit

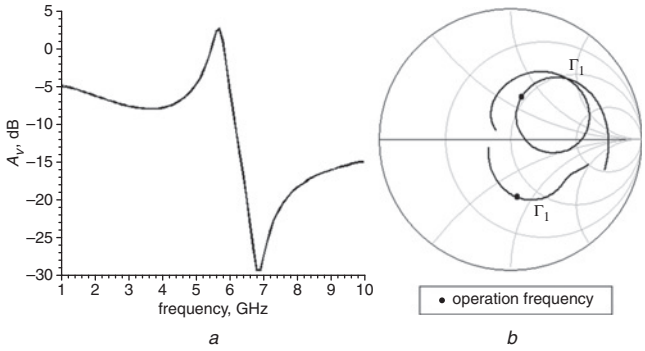

Fig. 3 *Simulation of $A_v = X/Y$ and inter-stage matching*

a $A_v = X/Y$
b Inter-stage maching

Measured results: The proposed LNA with IR function for wireless local area network (WLAN) receivers has been fabricated based on TSMC 0.18 μm CMOS 1P6M technology. It operates at 5.9 GHz, and image frequency is at 7.3 GHz. The chip photo of the proposed LNA is shown in Fig. 4, and the total chip size is 0.69 mm^2 including the probing pads. The pads use bottom ground metal as shielding. The total power consumption is 6.1 mW from a 1 V supply voltage. The measured input and output return loss are −16.4 and −15 dB at 5.9 GHz, respectively, as shown in Fig. 5. The lowest dip of S_{22} shifts 0.1 GHz owing to process variation. Fig. 6 shows gain (S_{21}) and noise figure. The measured gain achieves a maximum of 15.2 dB at 5.9 GHz and IR of −27 dB at 7.3 GHz. The measured noise figure is 3.2 dB and input-referred third-order intercept point (IIP3) is −9 dBm.

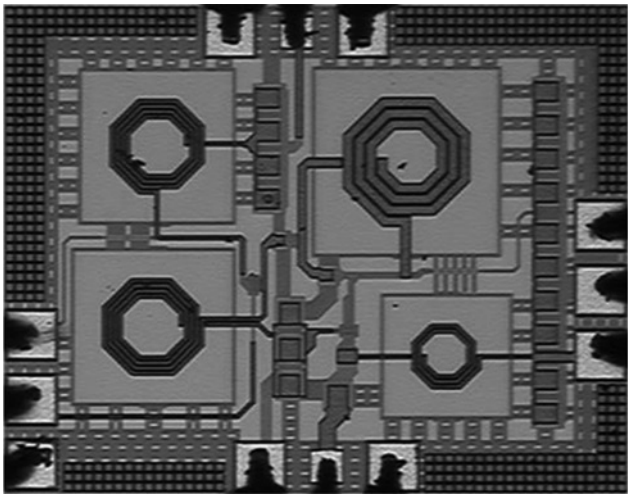

Fig. 4 *Photograph of proposed LNA*

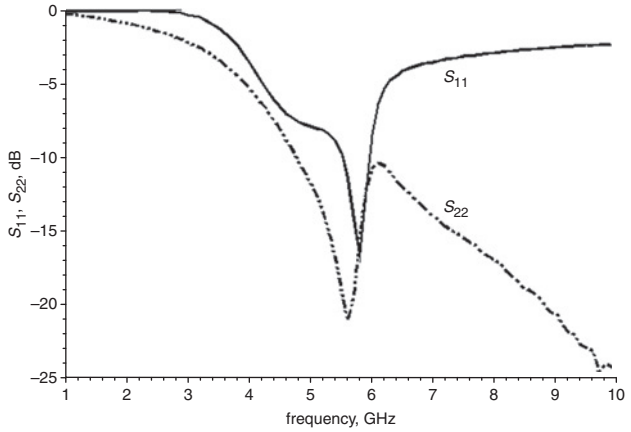

Fig. 5 *Measured results of input and output return loss*

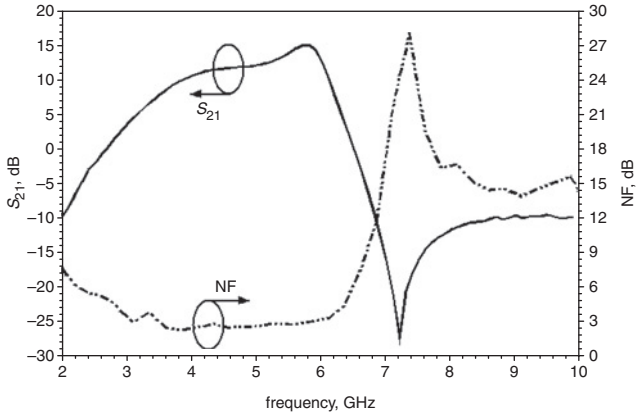

Fig. 6 *Measured results of gain and noise figure*

Conclusions: A fully integrated low-voltage IR LNA using Q enhancement technique for WLAN is proposed, based on current-reuse configuration for low-power operation, not cascode as in major traditional IR LNA. The IR filter is composed of passive components in order to allow less noise and less power consumption compared to an active filter. The experimental results show that this circuit provides better IR ability and lower power than [1]. The performance of the proposed LNA satisfies the system specification and chip size is comparatively small.

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