Appl. Phys., **77**, 3710 (1995). 10. S. M. Hu, Appl. Phys. Lett., **36**, 561 (1980). 11. J. Furukawa, N. Iwaoka, and H. Furuya, *Mater. Sci.* Forum, **196-201**, 1725 (1995). 12. W. Wijaranakula and H. D. Chiou, Appl. Phys. Lett., **64**, 1030 (1994).

The Influence of Precleaning Process on the Gate Oxide Film Fabricated by Electron Cyclotron Resonance Plasma Oxidation

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ABSTRACT

The influence of the precleaning process on the characteristics of SiO_2 film grown by using electron cyclotron resonance (ECR) plasma oxidation at room temperature is presented in this work. We find that the growth rate, electrical properties, and reliability of the ECR plasma grown oxide is improved by this precleaning step. Two growth mechanisms are found which determine the electrical properties of the plasma grown oxide. The plasma damage is also discussed. We find that plasma oxidation produces little plasma damage in our experiments. Excellent ECR plasma grown silicon dioxide with good electrical properties and reliability characteristics are obtained by this precleaning technique.

Introduction

The formation of low temperature silicon dioxide is needed in some device structures such as thin film transistors (TFTs) for displays, SiGe metal oxide semiconductor field effect transistors (MOSFETs) etc. For this requirement, the plasma enhanced chemical vapor deposition (PECVD) oxide1 or liquid phase deposited (LPD) oxide2 are used to meet the low temperature issues. However, the growth rate and electrical properties of these methods are not easily controlled. On the other hand, the fabrication of a thin SiO₂ dielectric by plasma oxidation has been studied.³⁻⁷ It has been shown that the interface between the deposited SiO2 film and Si substrate can be improved by applying plasma oxidation just before film deposition. The minimum interface states density was as low as 4 imes10¹⁰ cm⁻² eV⁻¹. Besides, the electrical characteristics (e.g. mobility, D_{it} , etc.) are better than those of chemical vapor deposition (CVD) SiO₂ 4 as they are applied to fabricate the gate oxide of TFT devices. In addition, good electrical properties of gate oxide with plasma N₂O annealing has been obtained.3 The purpose of using N2O is to add some nitrogen atoms into SiO₂ film which improves the reliability of this thin film.8,9

It is also well known that the surface condition before oxidation determines the quality of the as-grown silicon dioxide. However, in previous studies, there are rarely reports about the influence of plasma precleaning on the quality of SiO₂ films grown by plasma oxidation. Plasma N₂O has been used to grow an oxynitride film before remote PECVD SiO₂;^{1,10,11} however, the key concept is that growing a plasma oxide yields a better interface between CVD SiO₂ and Si. Also, the electrical/reliability properties of the plasma grown SiO₂ film are rarely discussed. Therefore, in this work, we study plasma grown SiO₂ at room temperature with and without precleaning steps. Their growth rates, interface quality, and electrical reliability are discussed.

Experimental

The ECR plasma system used in our experiment is shown in Fig. 1. The coils surrounding the plasma chamber will generate an 875 gauss magnetic field density in the plasma chamber and 2.45 GHz microwaves are fed from the top of the plasma chamber. The substrate holder is approximately 18 cm below the plasma extraction port and is maintained at room temperature in our experiments. The substrate holder is not biased. The gas is injected into the plasma chamber and will be excited to become plasma by the magnetic field and the microwaves.

p-Type (100) 15 to 25 Ω cm Si wafers are used as the oxidation substrate. The process pressure is fixed at 1 mTorr. After initial cleaning, a wafer is transferred into the reaction chamber. The base pressure of our ECR system is about 1×10^{-6} Torr. The oxide thickness is measured by ellipsometer with fixed refractive index 1.462. For the study of electrical properties and the effective oxide thickness determination, poly silicon MOS capacitors are fabricated on the same silicon wafer. After plasma oxidation, 300 nm poly-Si is deposited at 620°C by a low pressure chemical vapor deposition (LPCVD) system and then followed by 850°C POCl₃ doped for 30 min. A 500 nm thick aluminum film is then deposited and patterned. The sample back side is also deposited with a 500 nm aluminum film as contact. Postmetallization annealing (PMA) is done at 400°C for 30 min in N_2 ambient. The capacitor areas are 3×10^{-4} and 6.28×10^{-5} cm² with circular shapes.

Except for those specifically mentioned, the flow rates of the gases used in our experiments are fixed at 50 sccm and the precleaning time is fixed at 10 min. The microwave power is 220 W for the precleaning step and 250 W for the plasma oxidation. During electrical measurement,

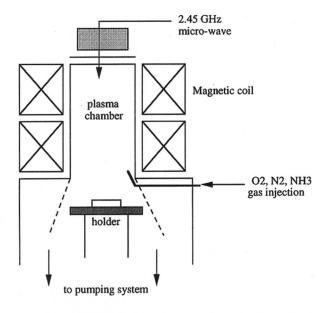


Fig. 1. Schematic diagram of the ECR plasma system.

the capacitors are tested at accumulation (negative gate biased). The interface states are determined by quasi-static and high frequency (1 MHz) current-voltage (C-V) measurement. For the measurement of cumulative distribution of the oxide reliability, 50 MOS capacitors are measured for each sample.

Results and Discussion

The influence of precleaning on oxide thickness.—Figure 2 shows the silicon dioxide thickness with different plasma precleaning conditions. After precleaning, plasma oxidation is performed to grow silicon dioxide. The thickness is determined by an ellipsometer with a fixed refractive index of 1.462. It is easily seen that the thickness is greater for the SiO_2 with the precleaning process than that without the precleaning step. When NH_3 gas is used to perform the precleaning process, the highest growth rate is obtained.

In order to investigate the precleaning effect, all of the samples have the same growth conditions except that some will undergo the precleaning step and others are not exposed to this process. Apparently, different oxide thicknesses are obtained. This means that the initial surface condition before plasma oxidation determines the growth kinetics. We think that although a standard RCA initial cleaning is performed before the sample is transferred into the ECR system, the native oxide on the silicon surface still existed. After the O_2 plasma is initiated, the initial oxygen plasma will "see" the surface of native SiO_2 (not the bare Si atoms in the substrate). The oxygen species diffuse through this native oxide film and then oxidize the silicon atoms. Thus, the oxidation is retarded, which lowers the oxidation rate. On the other hand, with the precleaning process in the vacuum chamber before plasma oxidation, the native oxide is removed and the silicon surface dangling bonds are activated. This leads to the higher growth mechanism because of direct reactions with this cleaned/activated silicon surface atoms and thus the higher growth rate. In other words, the oxidation reaction is continuous and the initial surface condition determines the growth mechanism. If the initial growth condition is determined, then the oxidation mechanism is decided. These two different growth mechanisms will affect the electrical properties of the plasma grown oxide.

Electrical properties.—The breakdown characteristics of the ECR plasma grown oxide mentioned above are determined by two methods: the time-zero dielectric breakdown experiment and constant current stress under Fowler-Nordheim (F-N) tunneling. The effective oxide thickness was measured by the C-V method. The break-

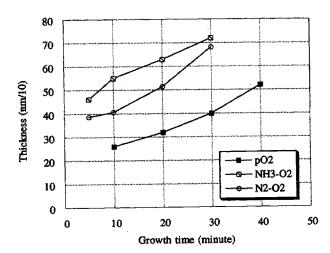


Fig. 2. The oxide thickness with different growth time. The curve of pO₂ is the sample without precleaning, the curve of NH₃-O₂ uses NH₃ plasma precleaning for 10 min, and the curve of N₂-O₂ uses N₂ plasma precleaning for 10 min.

down field (BF) distributions of different samples are shown in Fig. 3. The capacitor area is 3 \times 10 $^{-4}$ cm². Because the growth rate is too low for the oxygen only plasma used without pretreatment, we added some N_2 gas into O_2 plasma to improve the growth rate. The gas ratio is $N_2/O_2=9$ (sccm)/50 (sccm) and the growth pressure is also at 1 mTorr. This sample (WO) is used for the case without precleaning for electrical measurement, and its BF distribution is shown in Fig. 3. The oxide thickness of WO is 7 nm. In Fig. 3, the curve of WP- N_2 is the SiO $_2$ with 7 nm thickness precleaned by N_2 plasma and the curve of WP- N_3 is the SiO $_2$ with 7.2 nm thickness precleaned by N_4 plasma.

The BF distributions of ECR oxide with and without pretreatment (WO, WP-N2, and WP-NH3) are all tightly distributed in the higher breakdown field (-12 \sim -13 MV/cm) region and very small B-mode breakdown¹² distributions exist. Note that the dielectric breakdown fields are categorized into three modes: A, B, and C modes. The A mode can be attributed to the pinhole of the gate oxide which causes nearly zero breakdown field (< 1 MV/cm). The B mode is caused by a weak spot of oxide with intermediate breakdown field (1 MV/cm ~ 8 MV/cm). The C mode is due to the defect-free oxide breakdown (intrinsic dielectric breakdown). The results in Fig. 3 reveal that there is a small number of defects (such as pinholes, weak spots, etc.) in our samples, which result in lower dielectric breakdown field. From this figure, the lower value breakdown field distribution of samples of WP-N2 and WO are smaller than that of WP-NH₃. This means that with the N₂ plasma precleaning step, the BF characteristics of SiO2 were not influenced; however, if the NH3 plasma precleaning is used the BF characteristics are slightly degraded. However, for the charge-to-breakdown (Q_{bd}) distributions, the samples with the precleaning steps are better than those without the precleaning processes. This can be seen in Fig. 4. The $Q_{\rm bd}$ was measured by applying a constant -200 mA/cm² F-N tunneling current density on the MOS capacitor with an area of $6.28 imes 10^{-5}$ cm². It can be seen that the Q_{bd} of all the ECR plasma oxidized oxide can be achieved -9 C/cm² under the -200 mA/cm² stressing. From this figure, we found that samples of WO exhibit significant distributions for cumulative failure less than 60%. However, samples of WP-N2 and WP-NH3 do not exhibit the phenomenon of WO. From the results of Fig. 3 and 4, we conclude that with the N2 plasma precleaning step, the breakdown field and reliability characteristics of gate oxide grown by ECR plasma oxidation can be

The interface states of samples WO, WP- N_2 , and WP- NH_3 are shown in Fig. 5. The initial midbandgap interface

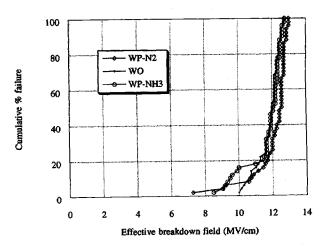


Fig. 3. The cumulative failure distribution of effective breakdown field. WO denotes without precleaning, WP- N_2 is with N_2 precleaning, and WP- N_3 denotes N_3 precleaning.

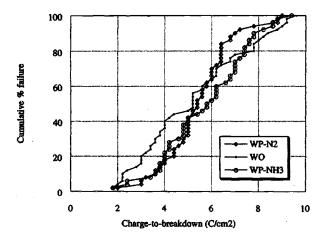


Fig. 4. The cumulative failure distribution of $Q_{\rm bd}$.

states are 6.5×10^{10} , 8×10^{10} , and 2.4×10^{11} cm⁻² eV⁻¹ for WO, WP-N₂, and WP-NH₃, respectively. It can be seen that the initial D_{it} of WO is lower than those of the other two, and sample WP-NH $_3$ has the highest D_{it} . If the nitrogen is in the SiO_2 , the reliability characteristics (such as $\Delta g_{\rm m}$, $\Delta V_{
m T}, \Delta D_{
m it}, \, Q_{
m bd}$, etc.) are improved. $^{
m s}$ Furthermore, if nitridation is performed with NH₃ gas, higher interface states generation may be formed. ^{13,14} The precleaning gases used in our experiments contain the nitrogen "N" species; this pretreatment step will have some nitridation effect, and the D_{it} of those with the precleaning step will be slightly higher. The worst case is found in the NH₃ precleaned sample (WP-NH₃). However, the $Q_{\rm bd}$ distributions are better for samples with the "N" related precleaning step due to the "N" incorporation during the precleaning which can be seen from the results of Fig. 4. Although the sample WO (grown by mixed N2/O2 plasma) may incorporate some nitrogen atoms into oxide, the improvement of Q_{bd} is smaller than for the other two samples.

In order to study the interface quality of the plasma grown oxide, changes of the midgap interface states (ΔD_{it}) after constant $-10~\text{mA/cm}^2$ current density stressing for 10~s for samples of WO, WP-N2, and WP-NH3 are investigated. The ΔD_{it} of WO, WP-N2, and WP-NH3 are about $2.3\times10^{11}, 2.3\times10^{11}, 4\times10^{11}~\text{cm}^{-2}~\text{eV}^{-1}$. It can be found that ΔD_{it} of WP-N2 and WO are about the same, but ΔD_{it} of WP-NH3 was found to be higher than the other two samples. This may be attributed to a weaker NH3 precleaning/nitridation effect, and more precleaning/nitridation should be

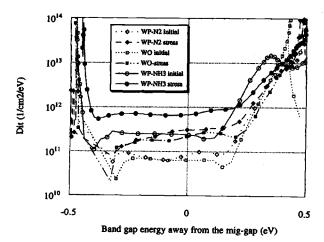


Fig. 5. The interface states evaluation of the samples of WO, WP- N_2 , and WP- N_3 . The solid symbols mean the $D_{\rm ft}$ after constant -10 mA/cm² current density stressing for 10 s.

used. ^{13,14} Although using N_2 precleaning will result in better $Q_{\rm bd}$ performance, the resistance of $\Delta D_{\rm it}$ was not significantly improved.

The gate voltage shift during -200 mA/cm² constant current density stress is investigated in Fig. 6. It is interesting to note that no negative charge trapping phenomenon exists in the oxide of WO and WP-N2. However, the oxide of WP-NH3 shows the trend of negative charge trapping. This may be attributed to some hydrogen atoms in the NH₃ gas which incorporate into SiO₂ and these H atoms are the sources of electron trapping which cause negative gate voltage shift. 15,16 Thus, a slightly negative charge trapping effect is seen in WP-NH3. It should be noted that positive charge trapping dominated for all of the samples. This phenomenon is different from the results of our previous study,17 in which the negative charge trapping dominated, and no positive charge trapping was observed. The different trapping effect existing in silicon dioxide grown by the same method was still observed in another study18 even in the thermal grown oxide. This phenomenon is still not clear presently.

The effect of plasma damage.—An important consideration of using plasma oxidation is that the film growth in the plasma ambient will be damaged by the plasma. In order to identify this damage, we transferred an oxide grown by dry O2 at 900°C in a conventional furnace with 5.6 nm thickness into our ECR system, then we excited the O2 plasma to grow oxide. The final effective oxide thickness is 7 nm. The poly-Si gate MOS capacitor was fabricated for electrical measurement, while the processes of MOS capacitor fabrication are the same as described in the Experimental section. Ramped I-V curves of this damaged oxide (DO) are shown in Fig. 7. It is clearly seen that the plasma-induced leakage current is higher due to the plasma damage. However, our ECR plasma grown SiO2 (WP- N_2) does not have this higher plasma-induced leakage. Even in the sample of WP-NH₃, which has a higher pretunneling leakage current due to the NH3 precleaning step, it does not have this larger plasma-induced leakage current. This indicates that very low plasma damage was done in our ECR plasma oxidized SiO₂ film with precleaning step.

Above, we find that there are two different growth mechanisms, that is, the oxidation with "initial" oxide existing on the Si surface and the oxidation with cleaned/activated Si surface. Besides, these different growth mechanisms will determine the quality of oxide. Before growing sample DO, a 5.6 nm SiO₂ has been on the Si surface and the growth mechanism is different from that of sample WP-N₂ with a cleaned surface. The possible explanation may be that the worst plasma damage will build in the initial stage of plasma oxidation but not in the plasma turn-off stage. Thus, the sample with "initial"

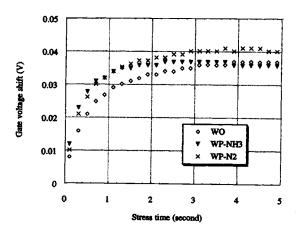


Fig. 6. The gate voltage shifts during constant -200 mA/cm² current density stressing.

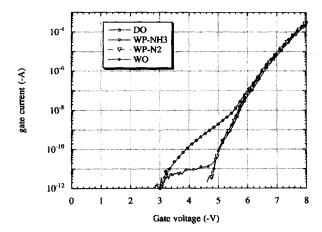


Fig. 7. The I-V curves of SiO₂ with different plasma treatment conditions. The curve of DO represents the growth with an initial 5.6 nm thermal oxide to about 7 nm by plasma O_2 oxidation.

insulator of silicon dioxide will build negative charges on the insulator surface to maintain the plasma condition which in turn will cause damage. However, the sample of WO with native oxide before plasma oxidation does not have this plasma-induced leakage current. This is due to the fact that native oxide is very thin (about 0.3 nm) and hence the plasma damage is very small. For thicker "initial" oxide on Si surface, the charges which are built up in the initial oxidation stage are larger in the thicker SiO₂ film, and hence higher plasma damage induced leakage current will be seen. However, for the cleaned surface, negative charges are built up in the Si (not in the insulator), and lower or even no plasma damage is expected. It should be mentioned that if the plasma oxidation pressure is reduced, the oxide will be damaged by the higher energetic ion bombardment even with the precleaning step. However, the plasma-induced leakage current is still not significant (not shown here).

Conclusion

Excellent gate oxides grown by ECR plasma oxidation have been obtained. The $E_{\rm bd}$ is about -13 MV/cm and the $Q_{\rm bd}$ can reach $-9~{\rm C/cm^2~under}~-200~{\rm mA/cm^2}$ constant current density stressing. In addition, the quality of the plasma grown SiO₂ can be improved with N₂ plasma precleaning step. There are different growth mechanisms for the samples with and without the precleaning processes. Without the precleaning step, plasma damage is higher. Besides, the plasma damage may build at the initial stage of the plasma oxidation.

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REFERENCES

- 1. T. Fuydi, T. Oka, and H. Matsunami, Jpn. J. Appl. Phys., 33, 440 (1994). C. F. Yeh, S. S. Lin, C. L. Chen, and Y. C. Yang, IEEE
- Electron Device Lett., **EDL-14**, 403 (1993)
- 3. P. C. Chen, Klaus, Y. J. Hsu, H. L. Hwang, and J. Y. Lin,
- J. Appl. Phys., 76, 5508 (1994).
 P. W. Li, E. S. Yang, Y. F. Yang, J. O. Chu, and B. S. Meyerson, IEEE Electron Device Lett., EDL-15, 402 (1994)
- 5. J. Y. Lee, C. H. Han, and C. K. Kim, ibid., EDL-15, 301 (1994)
- 6. D. W. Hess, Mater. Res. Soc. Symp. Proc., 236, 191 (1992).
- D. A. Carl, D. W. Hess, M. A. Lieberman, T. D. Nguyen, and R. Gronsky, *J. Appl. Phys.*, **70**, 3301 (1991).
 H. Hwang, W. Ting, D. L. Kwong, and J. Lee, *IEDM*,
- 421 (1990).
- 9. C. G. Sodini and K. S. Krish, *ibid.*, 617 (1992). 10. T. Yasuda, Y. Ma, S. HaBermehl, and G. Lucovsky, Appl. Phys. Lett., **60**, (1992). 11. D. R. Lee, C. G. Parker, J. Hauser, and G. Lucovsky, J.
- Vac. Sci. Technol, **B13**, 1788 (1995). 12. K. Yamabe and K. Taniguchi, *IEEE Trans. Electron*
- Device, 32, 423 (1985).
- 13. W. Yang, R. Jayaraman, and C. G. Sodini, ibid., ED-35, 935 (1988).
- 14. T. Hori, H. Iwasake, and K. Tsuji, ibid., ED-35, 904 (1988)
- H. S. Momose, T. Morimoto, Y. Ozawa, M. Tsuchiaki, M. Ono, K. Yamabe, and H. Iwai, IEDM Tech. Dig., 359 (1991).
- 16. T. Hori, H. Iwasaki, Y. Naito, and H. Esaki, IEEE Tran. Electron Device, ED-34, 2238 (1987).
- 17. K. M. Chang, C. H. Li, F. J. Fahn, J. Y. Tsai, T. S. Yeh, and W. S. Wang, To be published.
- 18. H. Fukuda, T. Arakawa, and S. Ohno, Jpn. J. Appl. Phys., 29, L2333 (1990).