Low-Power Programmable Pseudorandom Word Generator and Clock Multiplier Unit for High-Speed SerDes Applications

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***Abstract*—This paper presents the design of a low-power programmable pseudorandom word generator (PRWG) and a low-noise clock multiplier unit (CMU) for high-speed SerDes applications. The PRWG is capable of producing test patterns with sequence length of $2^7 - 1$, $2^{10} - 1$, $2^{15} - 1$, $2^{23} - 1$, and $2^{31} - 1$ b according to CCITT recommendations, and the random word is 16-bit wide. High-speed and low-power operations of the PRWG are achieved by parallel feedback techniques. The measured jitter of the CMU is only 3.56 ps_{rms}, and the data jitter at the PRWG output is mainly determined by the CMU. Implemented in an 0.18-μm CMOS process, the power dissipation for the PRWG is only 10.8 mW, and the CMU consumes about 87 mW from a 1.8-V supply. This PRWG can be used as a low-cost substitute for external parallel test pattern generators.**

***Index Terms*—Clock multiplier unit (CMU), parallel feedback shift register (PFSR), psuedorandom word generator (PRWG), SerDes.**

I. Introduction

The rapid development of high-speed serial link technologies, such as HDMI, PCI Express, Serial ATA, SONET, and GbE, have driven the data rate beyond the multi-GHz range. They create strong demands for low-cost, reliable, and automatic testing methodologies of these high-speed transceivers. Pseudorandom bit sequences (PRBS) provide a convenient way of testing these devices and have been widely used for eye diagram, bit error rate (BER), and jitter measurements. To facilitate built-in self test (BIST) of these components, a low-cost PRBS generator and a BER tester (BERT) can be integrated with the transceiver as substitutes for expensive, external testers and equipments.

Fig. 1 depicts the architecture of a serial link transceiver with BIST circuit. During the loop-back self-test mode, the test pattern is generated from a PRBS generator in the BIST circuit, traveling through the serializer, driver, an emulated channel (such as a jitter injection filter to stress the received eye diagram), and then received by the receiver for BER measurement.

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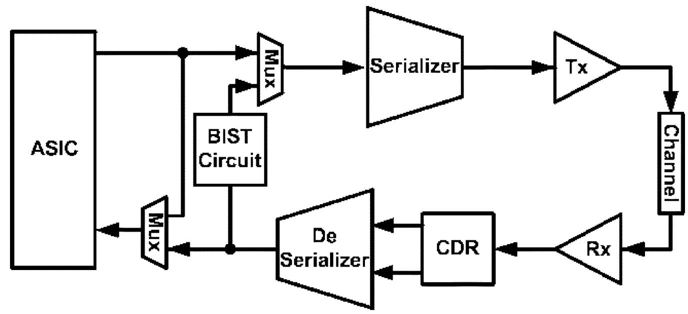


Fig. 1. Serial-link transceiver with BIST for loop-back test.

The response of the device under test (DUT) for different length of PRBS patterns can reveal essential hints about the device's performance, such as driving capability, bandwidth, and jitter generation. For example, a clock and data recovery unit in general generates higher jitter when a longer length test pattern is fed in. Thus, it is more flexible to build in a pattern generator with selectable sequence length [1]–[5]. Moreover, to facilitate the BER measurement of a high-speed serializer and deserializer (SerDes), i.e., to take the impacts of the MUX and DEMUX (DUT) on the jitter performance into accounts, a pseudorandom word generator (PRWG) complying with the word length of the MUX and DEMUX is desirable for loop-back test [5].

This paper presents a generic architecture of a parallel-feedback multipattern PRWG with selectable mark densities [5]. A low-cost, low-power, 16-bit-wide PRWG for high-speed SerDes applications is demonstrated by the proposed technique. In addition, an 8-phase, 1.25-GHz clock multiplier unit (CMU) is also integrated on the chip as a clock source for the 10-Gb/s transceiver.

This paper is organized as follows. Section II describes the proposed parallel feedback shift-register-based PRWG. Conventional PRBS generators are based on a linear feedback shift-register (LFSR) architecture, which are operated at a full rate [1], [6], a half rate [2]–[4], [7], [8], [11], [12], or a quarter rate [9], [10] incorporating with multiplexers and demultiplexers. In contrast to the prior state-of-the-art, the proposed architecture, which can generate parallel random words at a relatively lower symbol rate, is more feasible to comply with the SerDes BIST, is capable of high-speed operation, occupies a smaller chip area, and consumes much less power. In addition, the mark density and the sequence length are also selectable. Section III describes a multiphase CMU for the SerDes applications. Low-noise, low-power, and high-speed operations are achieved by

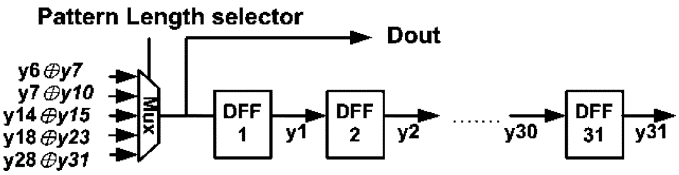


Fig. 2. Conventional programmable PRBS generator.

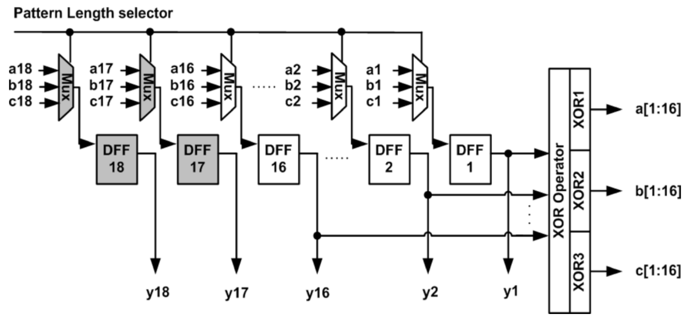


Fig. 3. PFSR-based PRW generator (for $n < 16$).

utilizing a ring-type voltage-controlled oscillator (VCO) with negative skew delay compensation [13]. The experimental results of both the PFSR-based PRW generator and CMU are presented in Section IV. Finally, a conclusion is drawn in Section V.

II. Pseudorandom Word Generator

To facilitate the characterization of a high-speed SerDes (including MUX and DEMUX on the transceiving path), a programmable, multi-pattern, PRWG generator complying with the word length of the MUX and DEMUX is desirable for BIST. According to CCITT recommendations [14], the following polynomials are implemented to generate pseudorandom words with sequence lengths of $2^{31}-1$ (f_{31}), $2^{23}-1$ (f_{23}), $2^{15}-1$ (f_{15}), $2^{10}-1$ (f_{10}), and $2^{7}-1$ (f_{7}), where

$$f_{31}(x) = 1 + x^{28} + x^{31} \quad (1)$$
$$f_{23}(x) = 1 + x^{18} + x^{23} \quad (2)$$
$$f_{15}(x) = 1 + x^{14} + x^{15} \quad (3)$$
$$f_{10}(x) = 1 + x^{7} + x^{10} \quad (4)$$
$$f_{7}(x) = 1 + x^{6} + x^{7}. \quad (5)$$

Fig. 2 shows a conventional programmable PRBS generator architecture [1], which is composed of an LFSR chain. To generate the above polynomials, the outputs of five XORs of various operations are fed back to the input of the finite state machine through a 5:1 MUX. The pattern length is chosen by a 3-b pattern length select signal. Once the loop is configured with a designated feedback, the pattern length of "Dout" can be determined accordingly.

Along with the increasing of the data rate, the clock frequency should be increased as well to trigger out the random bit streams. This imposes severe speed requirements of the LFSR digital logic circuits and consumes drastic power. Therefore, conventional BERT and PRBS generators are designed with silicon bipolar, SiGe BiCMOS, [1]–[4], [7]–[10], InP [11], or GaAs [12] technology, and the power dissipation is approximately several watts. Besides, standard PRB sequences have a mark density ratio, which is defined as the average ratio of number of zeros to ones in a sequence, of about 1/2 [2]–[4], [6]–[12]. To simulate the test vehicle of a dc unbalanced code, mark densities other than half, such as 1/4 or 1/8 are preferable [1], [5].

In order to facilitate parallel BER measurement and reduce the speed requirements of the logic circuitries, a PFSR-based PRWG with selectable mark densities of (1/2, 1/4, and 1/8) is proposed [5]. As a 16-bit-wide PRWG example, it is mainly comprised of 18 parallel feedback shift registers along with combinational logic. The extra two path (bits) extensions are utilized to incorporate with mark density control for up to 1/8, which will be explained later. To investigate the operating principles of the PFSR-based PRWG in detail, the architectures for generating sequence length of $2^n - 1$, where $n \leq 16$ and $n > 16$, are discussed separately.

A. Case I : 16-bit-Wide 2^{n-1} PRW Generator (for $n \leqq 16$)

Fig. 3 shows the circuit schematic of a 2^{n-1} PRWG with $n \leqq 16$, and the random word is 16-bit wide. The circuits shaded in gray are utilized for mark density control.

Let $a[1:16]$, $b[1:16]$, and $c[1:16]$ represent the succeeding random word ($y[17:32]$) that corresponds to different sequence lengths. According to CCITT recommendations, the following holds:

$$\text{if } n=7,\ a_i \equiv y_{i+16} = y_{i+9} \oplus y_{i+10}, \qquad i=[1\ldots 16] \quad (6)$$
$$\text{if } n=10,\ b_i \equiv y_{i+16} = y_{i+6} \oplus y_{i+9}, \qquad i=[1\ldots 16] \quad (7)$$
$$\text{if } n=15,\ c_i \equiv y_{i+16} = y_{i+1} \oplus y_{i+2}, \qquad i=[1\ldots 16]. \quad (8)$$

In the three cases, the succeeding random words can be derived from its previous word ($y[1:16]$) and part of itself ($y[17:32]$) through the XOR operations described in (6)–(8), which are implemented in XOR operators (XOR1-XOR3). For example, to generate a pseudorandom word of sequence length of 2^7-1, part of the next word $[y_{17},\ldots,y_{22}]$ can be derived from its previous word $[y_{10},\ldots,y_{16}]$, while the other part $[y_{23},\ldots,y_{32}]$ is derived from $[y_{16},\ldots,y_{26}]$, where $[y_{17},\ldots,y_{26}]$ are also generated in the current word. On the other hand, to generate a pseudorandom word with sequence length of $2^{10}-1$, part of the next word $[y_{17},\ldots,y_{23}]$ can be derived from its previous word $[y_{7},\ldots,y_{16}]$, and the other part $[y_{24},\ldots,y_{32}]$ is derived from $[y_{14},\ldots,y_{25}]$, where $[y_{17},\ldots,y_{25}]$ are also generated in the current word. The succeeding words ($a[1:16]$, $b[1:16]$, or $c[1:16]$) are then fed back to the input of PFSR through 3:1 multiplexers, and the sequence length is selected by the multiplexers.

B. Case II: 16-bit-Wide $2^n - 1$ PRW Generator (for $32 > n > 16$)

Also, let $d[1:16]$ and $e[1:16]$ represent the succeeding random word ($y[33:48]$) that corresponds to different sequence length. According to CCITT recommendations, the following holds:

$$\text{if } n=23,\ d_i \equiv y_{i+32} = y_{i+9} \oplus y_{i+14} \qquad i=[1\ldots 16] \quad (9)$$
$$\text{if } n=31,\ e_i \equiv y_{i+32} = y_{i+1} \oplus y_{i+4}, \qquad i=[1\ldots 16]. \quad (10)$$

In this case, the succeeding pseudorandom word comes out with the XOR operations of data in the previous two words. For

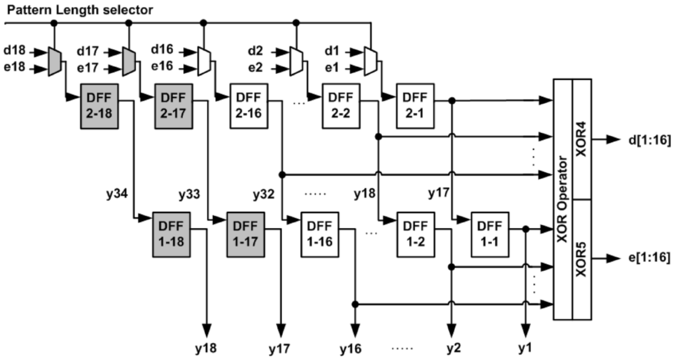


Fig. 4. PFSR-based PRW generator (for $32 > n > 16$).

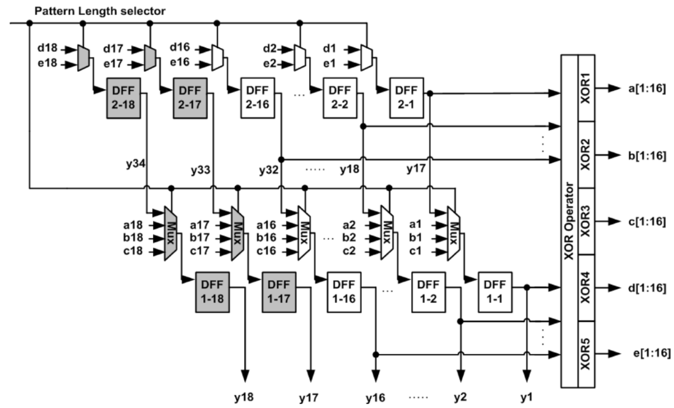


Fig. 5. Programmable 16-bit-wide, 5-pattern PRW generator ($n < 32$).

example, to generate a pseudorandom word with a sequence length of $2^{23} - 1$, the next two succeeding random words, $[y_{33}, \ldots, y_{48}]$, are derived from $[y_{10}, \ldots, y_{30}]$. On the other hand, to generate a pseudorandom word with sequence length of $2^{31} - 1$, the next two succeeding random words, $[y_{33}, \ldots, y_{48}]$, are derived from $[y_2, \ldots, y_{20}]$. Thus, this requires two register arrays (36 flip-flops) to store the previous two words. Fig. 4 shows the detailed circuit schematic. Here, $d[1 : 16]$ and $e[1 : 16]$ that correspond to different pattern lengths are fed back to the input of the PFSR through 2:1 multiplexers, and the XOR operators (XOR4 and XOR5) are utilized to implement (9) and (10). The sequence length of $2^{23} - 1$ or $2^{31} - 1$ is then selected by the 2:1 multiplexers .

C. *Case III: A 16-bit-Wide Multipattern-Length PRW Generator (for $n < 32$)*

In combination with cases I and II, a $2^n - 1$ ($n < 32$), 5-pattern, 16-bit-wide programmable PRWG is illustrated in Fig. 5. The PRWG is mainly composed of an 18×2 register array, 18 4:1 multiplexers, 18 2:1 multiplexers, and five XOR operators to implement the pattern generation polynomials. Here, DFF (1–1) to DFF (1–18) store the previous word of the PRWG outputs, and DFF (2–1) to DFF (2–18) store the current word. The two register arrays are connected in parallel feedback configuration. For $\mathrm{n} > 16$ ($n = 23, 31$), the PRWG is configured as a two-stage PFSR, and the top multiplexers select one of the pattern lengths. Thus, the successive random words can be stored in the FIFO to derive the next pseudorandom word. As $n < 16$ ($\mathrm{n} = 7, 10, 15$), the generator is reduced to a single-row PFSR, where the output sequence is selected by the bottom 4:1 multiplexers.

The critical path of the XOR operators is encountered for the generation of $2^7 - 1$ pseudorandom word. As is described in Case I, since the random word at the output is 16-bit wide while the feedback path is 7-bit deep, the derivation of the succeeding random word relies on part of itself. Thus, it takes more operations to fulfill the generation of a random word whose word length is longer than its feedback depth. Fig. 6(a) illustrates the detailed circuit schematic of the XOR operator for $n = 7$ (XOR1). It takes about three gate delays in the critical path. To shorten the delay time, the Boolean variables of the pattern-generation polynomials are substituted in a recursive form, which is described as follows.

To generate a PRW with a sequence length of $2^M - 1$, the mth bit of a random word y_m can be derived as

$$y_m = y_{m-M} \oplus y_{m-M+a} \tag{11}$$

where a corresponds to different word lengths ($a < M$).

We have

$$\begin{aligned} y_m &= y_{m-2M} \oplus y_{m-2M+a} \oplus y_{m-2M+a} \oplus y_{m-2M+2a} \\ &= y_{m-2M} \oplus y_{m-2M+2a}. \end{aligned} \tag{12}$$

Thus, y_m can be derived from y_{m-2M} and $y_{m-2M+2a}$ instead of y_{m-M} and y_{m-M+a}. Fig. 6(b) illustrates the circuit schematic of the modified XOR operator after recursive substitution according to (12), where the critical path in the XOR operator is reduced to a two-gate delay.

To sum up, the critical path delay time ($\mathrm{T_{delay}}$) of a $2^7 - 1$ PRWG can be described as

$$T_{\text{delay}} = t_{\text{dffs}} + t_{\text{dffp}} + 2t_{\text{xor}} + t_{\text{mux}}. \tag{13}$$

Here, t_{dffs} and t_{dffp} represent the setup time and the CK-to-Q delay of the flip-flop, and t_{xor} and t_{mux} denote the propagation delay of the XOR gate and the multiplexer. The t_{xor} is a critical term ($\sim$ 160 ps) in T_{delay}. By means of the proposed recursive Boolean variable substitution, the symbol rate for random words generation can be increased by about 30%.

The 16-bit-wide random word is fed into a mark density controller to alter its mark density. When two adjacent bits of the PRB sequence are "and"ed together, a "1" appears at the output only when both of the bits are 1 and the probability of appearing "1" becomes 1/4. It stands to reason that a PRBS with a mark density of 1/8 can be achieved by "and"ing the adjacent 3 bits. Thus, for a mark-density control up to $1/2^k$, extra $k - 1$ bits (paths) extension are needed to store the adjacent bits. The architecture of the mark density controller (MDC) is shown in Fig. 7(a), which is composed of 16 subcells (MDC1–16). The subcell of the MDC is illustrated in Fig. 7(b), which consists of an AND gate and two OR gates. The mark density of 1/2, 1/4, or 1/8 is then determined by the two-bits select signal (S1, S2).

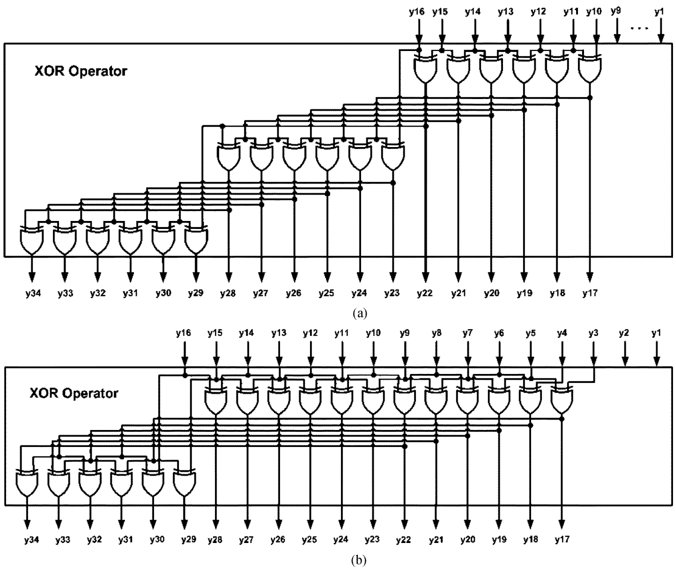


Fig. 6. (a) XOR operator. (b) Modified XOR operator (for $n = 7$).

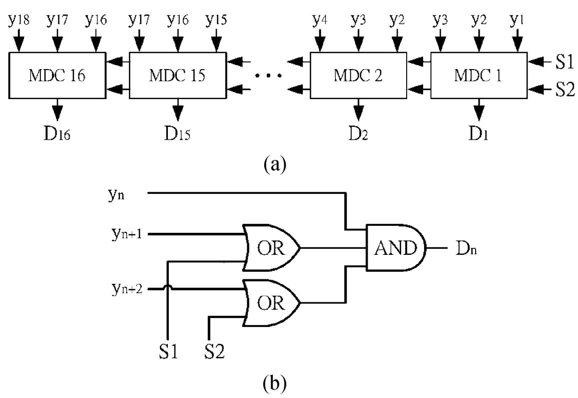


Fig. 7. MDC. (a) Schematic of the MDC. (b) MDC cell.

TABLE I
TRUTH TABLE OF THE MDC

S1	S2	$D_n(y)$	Mark density
0	0	$y_n \cdot y_{n+1} \cdot y_{n+2}$	$\frac{1}{8}\times\frac{2^{n-1}-1}{2^{n-1}}$
0	1	$y_n \cdot y_{n+1}$	$\frac{1}{4}\times\frac{2^{n-1}-1}{2^{n-1}}$
1	0	$y_n \cdot y_{n+2}$	$\frac{1}{4}\times\frac{2^{n-1}-1}{2^{n-1}}$
1	1	y_n	$\frac{1}{2}\times\frac{2^{n-1}-1}{2^{n-1}}$

The corresponding truth table for the MDC is summarized in Table I.

In summary, the proposed architecture can be extended to a generic PFSR-based PRW generator with selectable mark density. For a M-bit-wide PRWG with sequence length up to 2^L-1, i patterns, and mark density up to $1/2^k$, the PRWG can be configured as an $(M+k-1)\times N$ register array, where

$$N = \left\lceil \frac{L}{M} \right\rceil \qquad (N \in \text{Integer}).$$

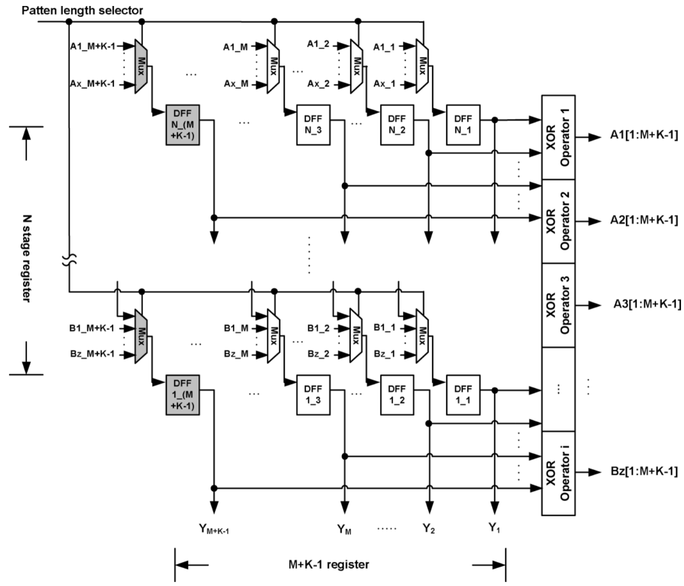


Fig. 8. Generic M-bit-wide, 2^L-1 PRWG with mark density up to $1/2^k$.

The detailed architecture is depicted in Fig. 8 [5]. In the initial state, one of the flip-flops is preset to 1 to avoid the generator being stuck at all zero. In contrast to conventional $1/M$-rate PRBS generators that are composed of M identical LFSR chains and at least $M\times(L+k-1)$ registers, the proposed architecture is much more area-efficient and low power in generating pseudorandom words.

As an experimental prototype, a 16-bit-wide PRWG targeted for 16:1 10-Gb/s SerDes is realized. This corresponds to an effective symbol rate of 625 MS/s for 10-Gb/s random bit generation. The PFSR scheme is a breakthrough for generating high-speed pseudorandom words in a relatively low-cost CMOS technology. Most important of all, it relaxes the operating speed of the digital logic circuits to save power.

III. Clock Multiplier Unit

The CMU is designed to provide a global clock for the PFSR PRWG and a 16:1 10-Gb/s data serializer. The serializer is composed of two-stage tree-like multiplexers. As the parallel to serial data conversion is achieved by means of time-division multiplexing, to alleviate jitter accumulation and relax the loading effect at the buffer stage, the CMU is operated at 1.25 GHz and provides eight phases for 10-Gb/s operations. The architecture of the CMU is depicted as shown in Fig. 9(a). Here, the 1.25-GHz output frequency is derived from a 625-MHz reference clock. A conventional tri-state PFD based on true single phase clocking (TSPC) dynamic logic circuit is utilized in this design, as is shown in Fig. 9(b).

Fig. 10(a) shows the VCO architecture, which is basically a four-stage ring oscillator. Each delay stage has four input terminals. To accelerate the operating speed of the oscillator while consuming less power, negative skew delay compensation technique is adopted [13]. In addition, the feedforward paths for the negative skew delay compensation (gray line) can keep the rising and falling times of the output waveform more balanced under various operating frequencies, which will be explained

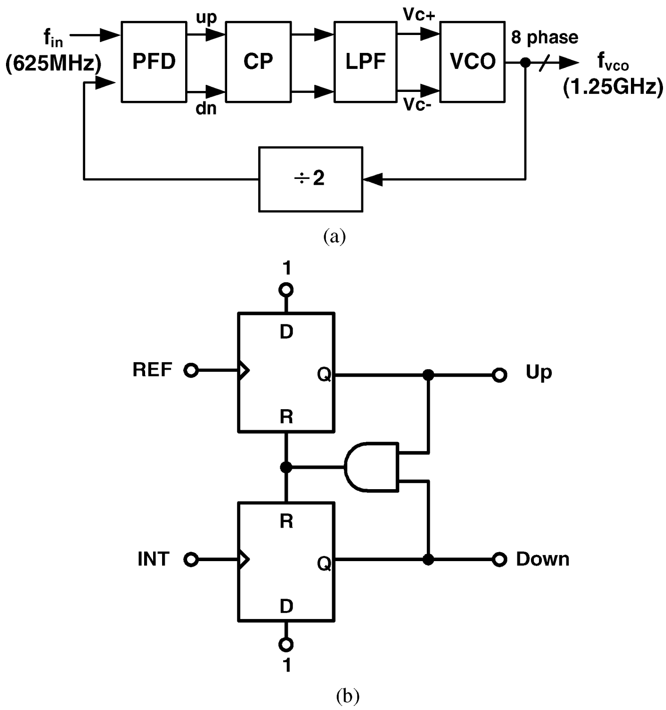


Fig. 9. (a) CMU architecture. (b) Phase frequency detector.

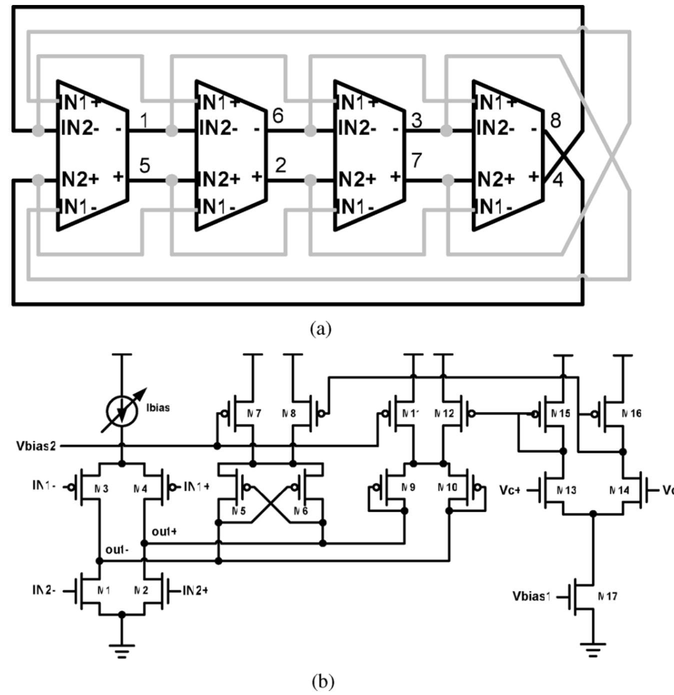


Fig. 10. (a) VCO architecture. (b) Delay cell.

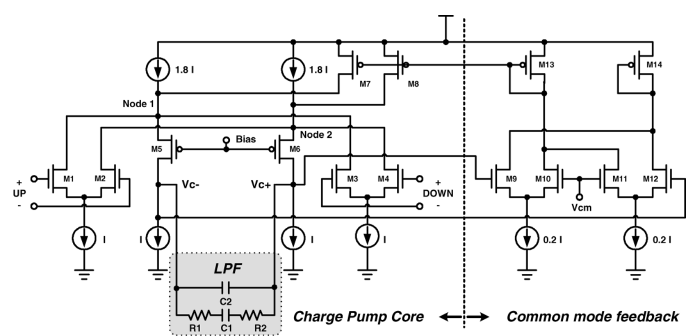


Fig. 11. Charge pump circuit.

below. The detailed circuit schematic of the proposed delay cell is illustrated in Fig. 10(b), which is composed of a complementary differential pair (M1-M4) with tunable resistive loads. To balance the switching speed of the nMOS (M1-M2) and pMOS differential pair (M3-M4), the signal path of the pMOS pair is configured in a feedforward loop. Thus, a lower phase noise performance can be achieved thanks to a more symmetric output waveform. The resistive loads are comprised of a negative resistance (M5-M6) and a positive resistance (M9-M10) in parallel.

To reduce the sensitivity of the VCO core, its output frequency is adjusted by a dual-loop frequency-tuning scheme. The coarse frequency tuning is accomplished by adjusting $I_{\rm bias}$, while the fine tuning is achieved by changing the current ratio between the positive and negative resistance. The control voltage (V_{c+}, V_{c-}) is converted to a differential control current though the frequency control unit (M13-M17) before being fed into the VCO. Also, since the control voltage is fully differential, the VCO has a higher immunity to common mode noise. As $(V_{c+} - V_{c-})$ is increased, the loading of the delay stage is reduced for high-speed operation. On the other hand, as $(V_{c+} - V_{c-})$ is reduced, the effective impedance loading is increased to slow down the VCO. In addition, two bleeding current sources M7 and M11 are injected at the tail nodes of the resistive load to avoid the VCO being driven into latched mode and solve the start-up problem.

Since the reference frequency of the CMU is as high as 625 MHz, for a low-noise operation, the response speed of the charge pump becomes critical. Fig. 11 illustrates the detailed circuit schematic of the charge pump circuitry, which is based on fully differential current-mode logic for both high-sensitivity and high-speed operations. The pumping currents are steered by the differential pairs (M1-M2) and (M3 -M4). When either the UP or DOWN signal is asserted, the pumping up or down current is equal to I. On the other hand, when both UP and DOWN are at high or low logic levels, the charge pump circuit is kept in the hold state. A second-order loop filter composed of $C1, C2, R1$, and $R2$ is adopted in this design. The output voltages at (V_c+) and (V_c-) are utilized for VCO frequency control. In order to preset the output common-mode voltage of the pumping circuit to comply with the tuning circuit of the VCO, a continuous-time common-mode feedback loop (M9-M14) is utilized.

IV. Experimental Result

The proposed PRWG and CMU have been integrated in a 10-Gb/s SerDes for loop-back BIST. Fig. 12 shows the chip micrograph of the 16:1 serializer. Implemented in an 0.18-μm CMOS process, the chip size is about 1160 μm $\times$ 1040 μm. The core size for the 16-bit-wide PRWG is about 500 μm $\times$ 250 μm, and the CMU occupies a chip area of about 1000 μm $\times$ 250 μm. Operating under a single 1.8-V supply, the power dissipation

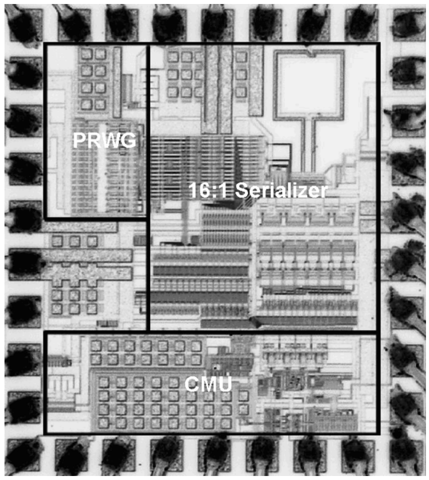
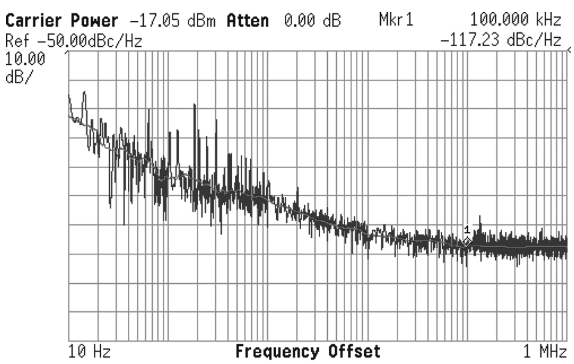
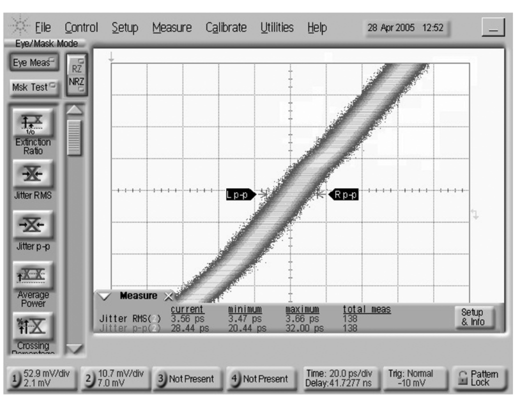


Fig. 12. Chip photograph.



(a)



(b)

Fig. 13. Measured CMU. (a) Phase noise. (b) Clock jitter at 1.25 GHz.

for the PRWG is only 10.8 mW, and the CMU consumes about 8.7 mW.

The measured phase noise and the timing jitter of the CMU at 1.25 GHz are shown in Fig. 13(a) and (b). The loop bandwidth of the phase-locked loop is about 10 MHz. The phase noise at 10-kHz offset is about -112 dBc/Hz, and is about -117 dBc/Hz at 100-kHz offset. The timing jitter is only 3.56 ps_{rms}. By the novelties of the VCO and the charge pump circuit, the proposed CMU utilizing a ring oscillator manifests a performance that is comparable to that of the *LC*-VCO-based CMU.

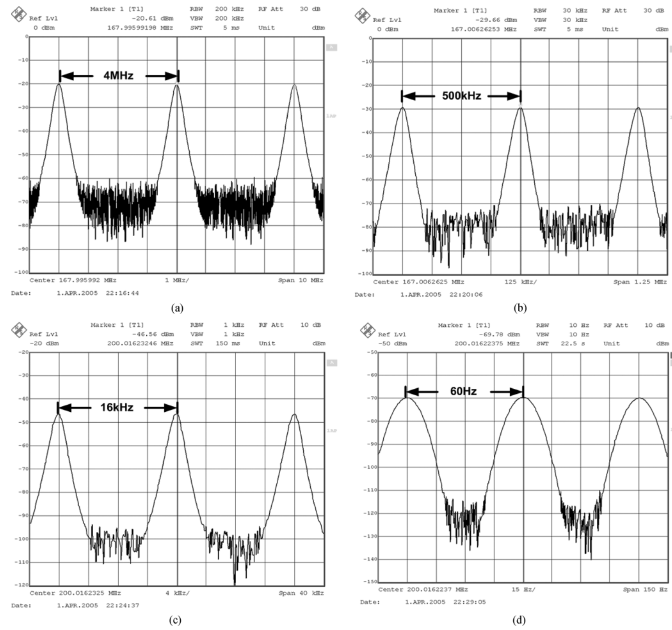


Fig. 14. Power spectra density of (a)2^7-1 PRBS @ 508 MS/s, (b) $2^{10}-1$ PRBS @ 511.5 MS/s, (c) $2^{15}-1$ PRBS @ 524.272 MS/s, and (d)$2^{23}-1$ PRBS @ 503.31642 MS/s.

The performance of the programmable PRW generator is characterized by the spectrum analyzer. For a nonreturn-to-zero pseudorandom bit sequence with pattern length of 2^n-1, its power spectra density $S(f)$ can be described as [15]

$$S_x(f)=\frac{L+1}{L}\left[\frac{\sin(\pi f\mathrm{T}_b)}{\pi f\mathrm{T}_b}\right]^2\sum\delta\left(f-\frac{n}{\mathrm{LT}_b}\right)+\frac{1}{L^2}\delta(f) \tag{14}$$

where T_b is the bit time, and $L=2^n-1$ is the pattern length. In other words, $S(f)$ consists of discrete spectral lines separated by $1/LT_b$ Hz.

In this experimental prototype, the measured maximum operating speed is around 500 MS/s due to layout parasitic, which can be applied for up to 8-Gb/s SerDes applications . The measured power spectra density of PRW with pattern lengths of 2^7-1, $2^{10}-1$, $2^{15}-1$, and $2^{23}-1$ are shown in Fig. 14(a)–(d), respectively. The spacing of the spectral line agrees well with that described in (14), which means that the PFSR-based PRWG works properly for the various pattern generations. The spectral line spacing of a $2^{31}-1$ PRW sequence is less than 0.3 Hz in the 625-MS/s frequency range, which is beyond the resolution of the spectrum analyzer and is not shown here.

V. Conclusion

In summary, a generic PFSR based, programmable PRWG architecture and a low noise, multiphase CMU are proposed for high speed SerDes applications. The 16 bits wide PRWG experimental prototype performs as a linear feedback shift register (LFSR) based counterpart with a 1 to 16 demultiplexer. It reduces the clock rate by 16 times, and is more feasible for parallel bit error rate measurement complying with multiplexer and demultiplexer. Most important of all, it consumes much less

TABLE II
BENCHMARK OF THE PRBS GENERATOR

	Technology	Applications	Power consumption
[1]	SiGe	15Gbps	2.3W
[2]	Si Bipolar	11.5 Gbps	6.2 W
[3]	Si Bipolar	12.5Gbps	4.6W
[6]	0.12μm CMOS	13Gbps	205.5mW
This work	0.18μm CMOS	8 Gbps (16x 500 Mbps)	10.8mW

power and is more area efficient compared to conventional architectures. Besides, a 1.25 GHz, 8 phase clock multiplier unit is realized. By the novelties of the VCO and charge pump circuits, the CMU manifests comparable jitter performance to that of LC-VCO based PLL.

The benchmark of the proposed PRW generator performance is summarized in Table II. The proposed PFSR-based PRW generator consumes much less power compared with those of conventional LFSR-based architecture [1]–[3], [6] and is more feasible as a test vehicle for a loop-back test combined with a multiplexer and demultiplexer.

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