Fourth-Order Cascaded $\Sigma\Delta$ Modulator Using Tri-Level Quantization and Bandpass Noise Shaping for Broadband Telecommunication Applications

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***Abstract*—This paper presents a 14-bit cascaded sigma-delta modulator for broadband telecommunication applications. The modulator is a 2-1-1 cascaded architecture that employs a resonator-based topology in the first stage, three tri-level quantizers, and two different pairs of reference voltages. As shown in the experimental result, for a 2.5-MHz signal bandwidth, the modulator achieves a dynamic range of 86 dB and a peak signal-to-noise and distortion ratio of 78.5 dB with an oversampling ratio of 16. The proposed modulator including reference voltage buffers and bandgap circuitry dissipates 62.5 mW from a 2.5-V supply. The active area is 1.2-mm^2 in a 0.25-μm CMOS technology.**

***Index Terms*—Analog-to-digital conversion, broadband telecommunication, MASH, resonator-based topology, sigma-delta ($\Sigma\Delta$)modulation.**

I. Introduction

THE growing trend in broadband telecommunication systems, such as asymmetric digital subscriber line (ADSL), is energizing the demand for low-cost low-power high-performance analog-to-digital converters (ADCs). The newly released ADSL standard ADSL2+, for instance, requires a 14-bit ADC with a signal bandwidth over 2.2 MHz while considering power dissipation and silicon cost. How one chooses the ADC architecture for optimizing the trade-off among power, resolution and bandwidth becomes a key issue.

Pipelined and sigma-delta ($\Sigma\Delta$) converters, among the existing ADC architectures, are most suitable candidates to meet the requirements of such applications. Generally speaking, pipeline ADCs can achieve wide bandwidth, but have limited dynamic range, high power dissipation, and large silicon area. On the other hand, the state-of-the-art $\Sigma\Delta$ ADCs can achieve high dynamic range and high bandwidth with noise shaping and oversampling techniques. Papers [1], [2] have presented single-bit cascaded $\Sigma\Delta$ modulators for ADSL application, which achieved 15-bit resolution and 1.1-MHz signal bandwidth with an oversampling ratio (OSR) of 24. To further extend the signal bandwidth and reduce the OSR, several papers [3]–[7] have presented modulators with high-order multibit topologies. As shown in their results, they can achieve 13-bit (or above) and up to 2 MHz of signal bandwidth when the OSRs range from 8 to 24. However, the use of the multibit quantizer requires data weighted averaging (DWA) algorithms to solve the nonlinear problem of multibit digital-to-analog converters (DACs). The DWA circuits usually consume extra power (say 30 40 mW with 2.5-V supply) [6], [7] and cost additional silicon area. Paper [8], [9] instead of using DWA, uses the cascaded architecture with the single-bit quantizer in the first stage and multibit quantizer in the last stage to relieve the linearity requirement of feedback DACs. Ideally, they can achieve high dynamic range for low-OSR design. Yet, in practical, the leakage quantization noise of such architectures may limit achievable dynamic range, and the multibit quantizer of the last stage may increase circuit complexity and power dissipation. Recently, paper [10] presents a single-loop fifth-order modulator with a tri-level quantizer, which is popular in pipelined ADCs, to achieve high dynamic range and consume low power for ADSL applications. Accordingly, we intend to take the advantage of the tri-level quantization and present a new topology for cascaded $\Sigma\Delta$ modulators to perform good trade-offs among power consumption, dynamic range and signal bandwidth.

Targeting on the specification of broadband telecommunication system, say ADSL2+, three architectural approaches are applied for the proposed cascaded $\Sigma\Delta$ modulator. First of all, the structure of the proposed cascaded modulator is 2-1-1 where uses the tri-level quantizer and DAC in each stage. Comparing with single-bit quantizer, the tri-level quantizer can reduce the quantization noise and result in larger inter-stage gain and, hence, larger dynamic range. Since the tri-level DAC suppresses the nonlinearity of the DAC to the required performance, the proposed modulator does not need DWA algorithm. Secondly, to improve the signal-to-noise ratio (SNR) of the modulator for low-OSR design, we employ a resonator-based topology in the first stage. The resonator-based topology adds in-band zeros in the noise transfer function (NTF) and hence suppresses the quantization noise over the signal band [11]. Furthermore, by adding an input feed-forward path into the first stage, the swing ranges and distortions of integrator outputs are reduced [12], [13]. Although this arrangement raises objections due to the increased difficulty of analog-digital mismatch (i.e., leakage quantization noise), with properly scaling the coefficients of the resonator, the proposed modulator can still achieve more than 80-dB SNR in case the capacitor mismatch is 0.5% and the opamp dc gain is 70 dB. Finally, we employed two different pairs of reference voltages for comparators and DACs to enhance the achievable dynamic range; a pair of 0.9 V is used

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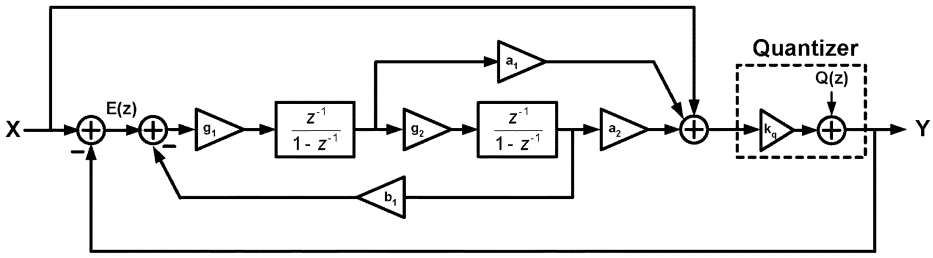

Fig. 1. Resonator-based second-order 1.5-bit modulator.

in the first stage and another pair of 0.45 V in the succeeded stages. The proposed modulator has been realized in a 0.25-μm CMOS technology. The experimental results show that the architecture, for a 2.5-MHz signal bandwidth, can achieve a dynamic range of 86 dB and a peak SNDR of 78.5 dB. It costs an active area of 1.2 mm^2 and consumes 62.5 mW from a 2.5-V supply voltage.

This paper is organized as follows. Section II describes the system-level design and architectural decisions of the proposed modulator with nonideality analysis. Section III provides circuit details for the implementation of proposed modulator. Section IV reports the measured results of the fabricated chip. Finally, Section VI concludes our work in terms of chip features.

II. Proposed Architecture

A. Design of Resonator-Based Modulator

The proposed architecture employs a resonator in the second-order stage of $\Sigma\Delta$ modulator. By adding in-band zeros, the resonator can suppress the in-band quantization noise and improve SNR. Fig. 1 illustrates the proposed resonator-based, second-order modulator. It uses a low-Q resonator-based loop filter that introduces a pair of zeros into NTF. The NTF of the resonator-based modulator can be expressed as

$$\mathrm{NTF}(z) = \frac{1 - 2z^{-1} + (1+r)z^{-2}}{1 - (2 - k_q c)z^{-1} + (1 + r + k_q d - k_q c)z^{-2}} \tag{1}$$

where $c = g_1 a_1$, $d = g_1 g_2 a_2$, and $r = g_1 g_2 b_1$. Note that r is the loop gain of the resonator and k_q is the gain of the quantizer. The zeros of NTF create a notch around the edge of signal band and hence suppress the in-band quantization noise. The suppression can improve the SNR of modulators, especially for low-OSR design [11]. The feedforward path from input to the adder followed by quantizer is used to suppress the signal swing and distortion caused by integrator nonidealities [12], [13]. Equation (2) shows the signal transfer function (STF) induced by the feedforward path

$$\mathrm{STF}(z) = \frac{k_q[1 - (2-d)z^{-1} + (1 + r + c - d)z^{-2}]}{1 - (2 - k_q d)z^{-1} + (1 + r + k_q c - k_q d)z^{-2}}. \tag{2}$$

Based on (2), the error signal $E(z)(= X(z) - \mathrm{Y}(z))$ becomes

$$\begin{aligned} E(z) &= [1 - \mathrm{STF}(z)]X(z) - \mathrm{NTF}(z)Q(z) \\ &= (1 - k_q)\mathrm{NTF}(z)X(z) - \mathrm{NTF}(z)Q(z). \end{aligned} \tag{3}$$

In (3), the term of $(1 - k_q)$ can be treated as the impact factor of $X(z)$ to $E(z)$. Obviously, the smaller the impact factor is, the less sensitive the loop filter is to input signal. When k_q is unity, the $E(z)$ does not have the component $X(z)$ and the integrators of the loop filter will only process the quantization noise $Q(z)$. In this case, the distortion caused by integrator nonidealities can be significantly reduced [12]. Unfortunately, k_q cannot be unity in practical design because there always exists quantization error between input and output of a quantizer. In case of using the single-bit quantizer, k_q is varying with the input signal of quantizer and its value can be much greater than unity. The variation of k_q causes the sensitivity of loop filter to input signal to be high. To take the advantage of making k_q unity, one can use the multibit quantizer to lower the sensitivity as much as possible [13]. Nevertheless, when using the multibit quantizer, the modulator requires the DWA algorithm to compensate the nonlinearity of the multibit DAC. Here we replace multibit quantizer with a tri-level one in that the k_q variation of tri-level quantizer can be reduced and the perfomacne is improved as compared with single-bit quantizer. Although the tri-level DAC introduces distortion, the 14-bit linearity can be achieved by careful sizing of transistors composing the OTA and symmetrical layout without using the DWA circuitry. The next subsection will detail the design of tri-level quantizer.

B. Analysis of Tri-Level Quantization

The tri-level quantization technique has been proved to be able to achieve high dynamic range without using DWA circuitry [14]. In our work, the use of tri-level quantization is twofold: 1) to keep the impact factor of $X(z)$ to $E(z)$ lower than that of the single-bit quantizer so the performance can meet the requirement of ADSL applications, and 2) to have the nonlinearity of feedback DAC lower than multi-bit quantizers so that the DWA is not a necessity for high dynamic range. To explain why the tri-level quantizer outperform single-bit one, we first define the value of k_q of tri-level quantization for a given threshold voltage V_{th} as shown as

$$k_q(S)_{\mathrm{tri-level}} = \begin{cases} Y/S, & \text{if } S \geq V_{\mathrm{th}} \text{ or } S \leq -V_{\mathrm{th}} \\ Y/||S| - V_{\mathrm{th}}| + V_{\mathrm{th}}, & \text{if } V_{\mathrm{th}} > S > -V_{\mathrm{th}}, \end{cases} \tag{4}$$

where S and Y are input and output amplitudes of tri-level quantizer. Based on (4), Fig. 2 illustrates the variation of k_q with the input amplitude of tri-level quantizer when $V_{\mathrm{th}} = 0.45$ V. As mentioned above, the smaller the impact factor is, the less sensitive the loop filter is to input signal. In this case, the value of k_q of tri-level quantizer ranges from 0.5 to 2 and the impact factor

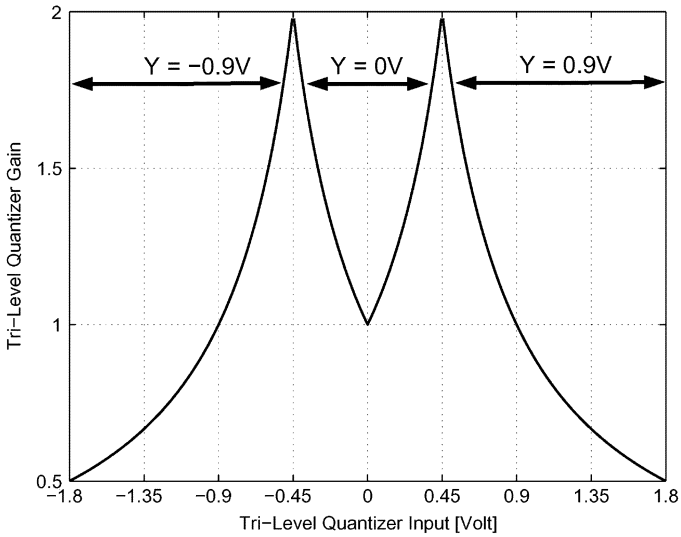

Fig. 2. Nonlinear gain of tri-level quantizer. ($V_{\rm th} = 0.45$ V).

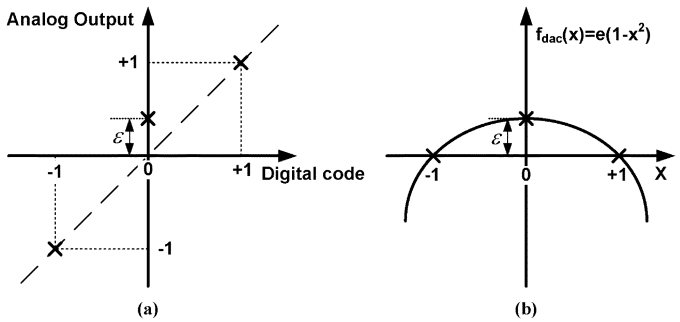

Fig. 3. (a) Transfer characteristic. (b) Error function of tri-level DAC. (The figures are excerpted from [14]).

from 0.5 to -1. However, for the single-bit quantizer, the value of k_q ranges from 0 to infinity and the impact factor from 1 to $-\infty$. Note that the infinity comes from the fact that the single-bit quantizer does not have a zero-level. If we consider the output levels of the quantizers between 1 and 0, the k_q of tri-level and single-bit quantizers with input level of 0.4 are 1.25 and 2.5, respectively. Therefore, the values of impact factor, $1 - k_q$, of tri-level quantizer are smaller than those of the single-bit quantizer.

The characteristic and nonlinearity of a tri-level DAC can be briefly described in Fig. 3(a). The horizontal axis represents the digital input codes while the vertical axis represents the analog output levels, which can vary due to circuit nonidealities. The nonlinearity is then defined by the displacement, ε, of medium level. With an approximation by using quadratic polynomial as shown in Fig. 3(b), the nonlinear error function of tri-level DAC can be expressed as [14]

$$e_{\rm DAC}(x) = \varepsilon(1 - x^2). \tag{5}$$

According to the analysis of paper [14], the well-sizing of the transistor of OTA and symmetrical layout will result in an ε of 0.01%, which enables 14-bit linearity.

To verify if the use of tri-level quantizer can reduce the harmonic distortion caused by integrator nonlinearities, we applied single-bit quantizer and tri-level quantizer for the resonator-based modulator. Given $V_{\rm th} = 0.45$ V, OSR $= 16$, and $f_s = 80$ MHz, Fig. 4 plots the third harmonic distortion results for 500-kHz sinusoid inputs. In the simulation, each integrator has a finite closed-loop pole at 240 MHz. The closed-loop pole frequency is three times of the sampling frequency f_s. As shown in Fig. 4, the third harmonic distortion of resonator-based modulator with tri-level quantizer is lower than -90 dB. So, its spurious-free dynamic range (SFDR) can be greater than 90 dB. Comparing with the single-bit version, the use of tri-level quantizer lowers the sensitivity of the loop filter to input signal and consequently reduces the distortion caused by integrator setting error.

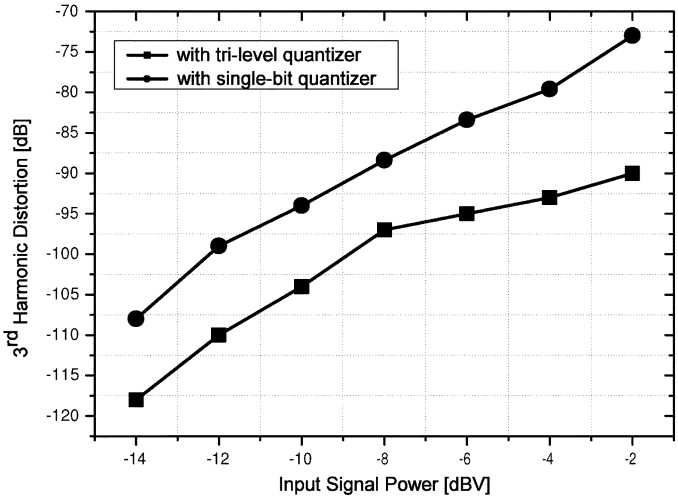

Fig. 4. The simulated 3rd harmonic distortion of resonator-based modulator with tri-level and single-bit quantizers. ($V_{\rm th} = 0.45$ V, fin $= 500$ kHz, OSR $= 16$, fs $= 80$ MHz).

C. Design of Fourth-Order Cascaded Modulators

The mostly popular fourth-order cascaded architectures are MASH 2-2 and MASH 2-1-1. An in-depth study on comparison of 2-2 and 2-1-1 cascaded architectures has been presented in [15]. Fig. 5 illustrates the block diagram of two resonator-based cascaded $\Sigma\Delta$ modulators, which are referred as RMASH 2-1-$1_{1.5b}$ and RMASH 2-$2_{1.5b}$. The first stage of the RMASH 2-1-$1_{1.5b}$, as mentioned above, uses the resonator-based modulator and the following two stages are the conventional first-order modulators. The $H_1(z)$ and $H_2(z)$ in Fig. 5(a) denote the digital error cancellation logic, which are used to cancel the first- and second-stage quantization noise of RMASH 2-1-$1_{1.5b}$. The transfer functions of $H_1(z)$ and $H_2(z)$ are deduced

$$\begin{aligned} H_1(z) &= 1 - 2z^{-1} + (1+r)z^{-2}, \\ H_2(z) &= (1 - z^{-1}) \cdot [1 - 2z^{-1} + (1+r)z^{-2}]. \end{aligned} \tag{6}$$

With ECL, the NTF of RMASH 2-1-$1_{1.5b}$ is given by

$$Y(z)/Q_3(z) = d_2[1 - 2z^{-1} + (1+r)z^{-2}] \cdot (1 - z^{-1})^2 \tag{7}$$

where $Q_3(z)$ is the quantization noise of tri-level quantizer in the third stage and d_2 is the inverse of $g_1g_2g_3g_4$. Obviously, the SNR can be improved by tuning parameters, d_2, r, and $Q_3(z)$. With the careful selection of the resonator loop gain r, the NTF zeros can produce a notch near the edge of the signal band to suppress the quantization noise over the desired signal band.

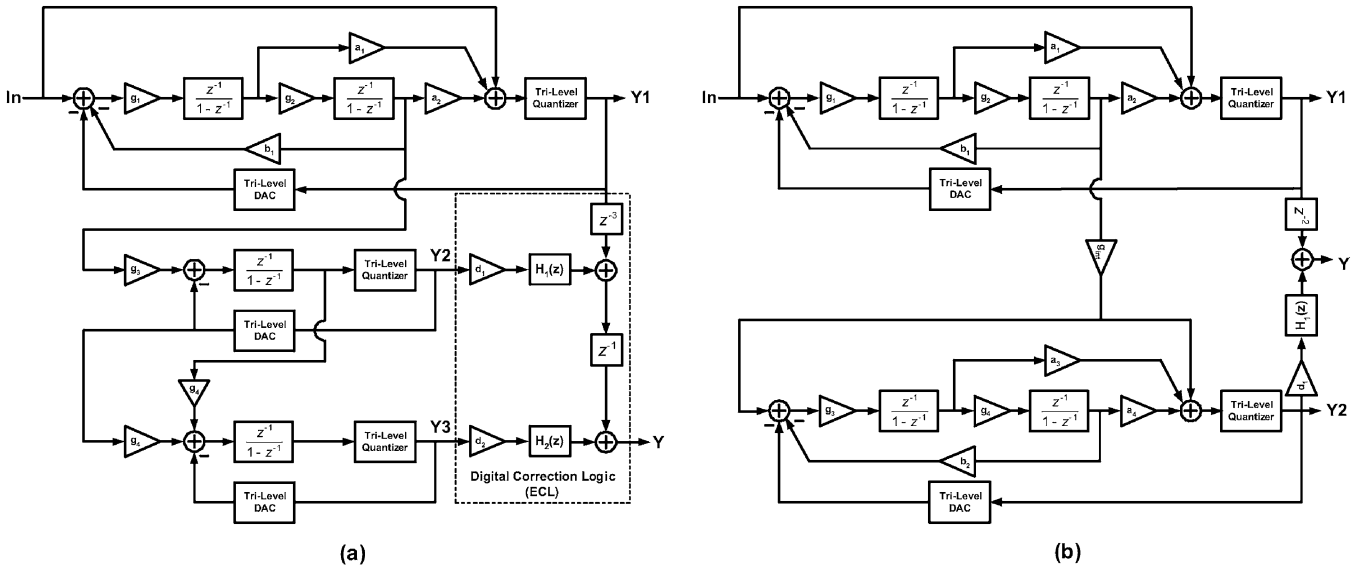

Fig. 5. Block diagrams of (a) RMASH 2-1-1$_{1.5b}$. (b) RMASH 2-2$_{1.5b}$.

According to [16], the NTF zeros are placed at the corner frequency of the signal band, and the value of r can be chosen by the following expression.

$$r = g_1 g_2 b_1 \approx [2\pi \cdot (f_{\text{notch}}/f_s)]^2. \tag{8}$$

At the OSR of 16, with in-band zeros, the four-order NTF can improve the SNDR by 14 dB.

Furthermore, we applied two pairs of reference voltages (TPRVs) for the proposed modulator; a pair of 0.9 V for the tri-level quantizer of first stage and another pair of 0.45 V for the quantizers in the second and third stages. The high voltage pair can have the first stage operate at high dynamic range while the low voltage pairs can reduce the output swing of the second stage and the power of $Q_3(z)$.

Based on (6), the theoretical quantization noise (TQN) can be expressed as

$$\text{TQN}_{\text{rms}} \approx 20\log_{10}\left(\frac{\Delta d_2 \pi^4}{108}\right) + 20\log_{10}\left(\frac{1}{\text{OSR}}\right) \tag{9}$$

where Δ is the step size of tri-level quantizer in the third stage. To reduce the TQN of the modulator, we cut down on paraments d_2 and Δ. Because of $d_2 = 1/g_1 g_2 g_3 g_4$, we first reduced the output swing of the second stage. The reduction implies that the integrator gain of g_4 can be increased and hence decreases d_2. Then, we halved the reference voltage of third stage to reduce the step size Δ of tri-level quantizer. Thus, with the proposed TPRVs, our work can have additional 12-dB SNR gain. The use of TPRVs does not affect the NTF and ECL equations. Although the SNR of the modulator is enhanced, this arrangement increases the effect of the leakage quantization noise, caused by capacitor mismatching and finite OTA dc gain. Fortunately, the desired SNR still can achieve 90 dB with 0.1% of capacitor mismatching and 70 dB of OTA dc gain. Using the same design methodology, the RMASH 2-2$_{1.5b}$ can achieve similar performance to RMASH 2-1-1$_{1.5b}$. One can also apply the second-order resonator-based modulator for stages of the RMASH 2-2$_{1.5b}$.

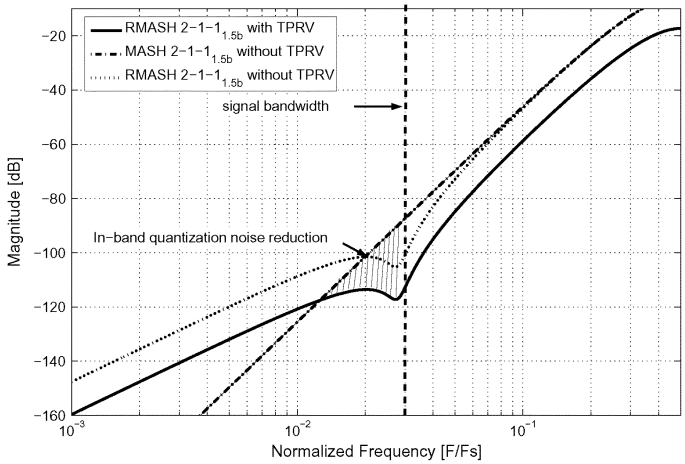

Fig. 6. TQN plots of RMASH 2-1-1$_{1.5b}$ with TPRVs, MASH 2-1-1$_{1.5b}$ without TPRVs, and RMASH 2-1-1$_{1.5b}$ without TPRVs.

Given the OSR of 16 and the d_2 of 2, Fig. 6 shows the NTFs of the proposed RMASH 2-1-1$_{1.5b}$ with TPRVs, conventional MASH 2-1-1$_{1.5b}$ without TPRVs, and RMASH 2-1-1$_{1.5b}$ without TPRVs. We can see the performance gain of 20 dB in the shadow region. Fig. 7 illustrates the SNR versus OSR in comparison of the fourth-order modulators using tri-level quantizer. To achieve the SNR of 90-dB (or higher), the single-loop architecture needs to operate at the OSR of 32 while the others need the OSR of 16. The lower OSR implies the lower power dissipation. To optimize the load of the second integrator of first-stage modulator and trade off the dynamic range of the opamp in the following stages, here we adopt the MASH 2-1-1$_{1.5b}$ as our design target.

In general, the leakage quantization noise is the major concern on the design of a cascaded ΣΔ modulator. The leakage quantization noise is mainly caused by the finite OTA gain and capacitor mismatching of the first-stage integrators. In the RMASH 2-1-1$_{1.5b}$, the capacitor mismatching is especially critical because the SNR improvement mainly relies on the in-band zeros induced by the first-stage resonator. Therefore,

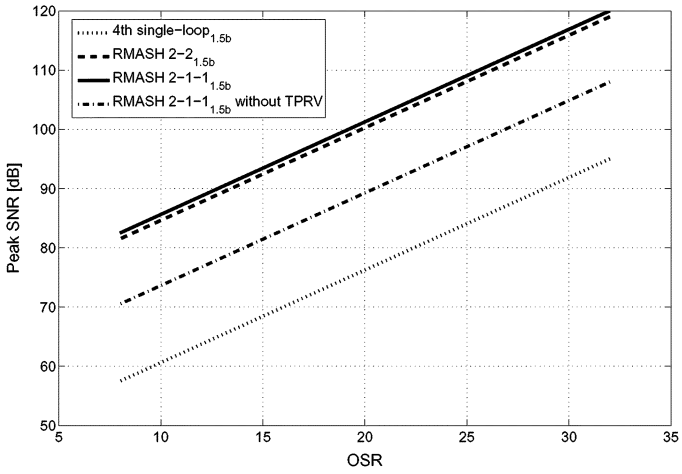

Fig. 7. Peak SNDR versus OSR plots for four different modulators.

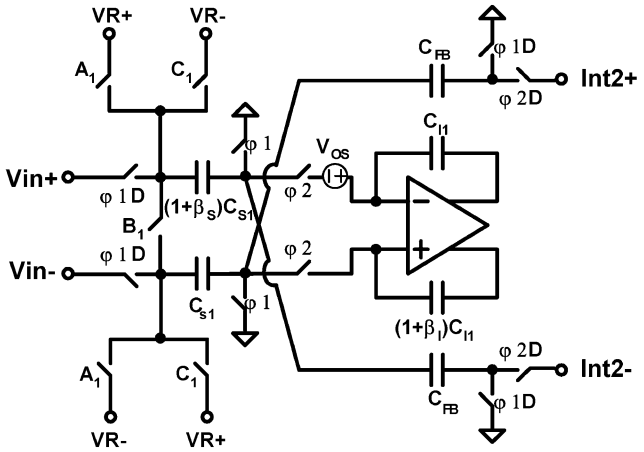

Fig. 8. Circuit implementation of the first integrator in the first stage of RMASH 2-1-$1_{1.5b}$.

we have to select coefficients of the loop filter in the first stage carefully to achieve the desired SNR. Fig. 8 shows a circuit implementation of the first integrator where the $g_1 = C_{S1}/C_{I1}$ and $b_1 = C_{\rm FB}/C_{S1}$. Given the notch and sampling frequencies of 2.25 and 80 MHz, the resonator loop gain $r = g1g2b1$, based on (8), approximates to 0.03125. In general, the g_1 and g_2 should be as large as possible to keep the thermal noise low, and thus b_1 has to be relatively small for the given r. Consequently, the difference between C_{S1} and $C_{\rm FB}$ may become large and cause a large ratio mismatching [17]. For instance, if $g_1 = 1, g_2 = 0.5$, and $C_{S1} = 1.5$ pF, b_1 and $C_{\rm FB}$ will be 0.0625 and 93.75 fF, respectively. The value of C_{S1} is much larger than that of $C_{\rm FB}$. To reduce the mismatch between C_{S1} and $C_{\rm FB}$ while keep transfer function unchaged, we scaled the g_1, g_2, and b_1 to 0.5, 0.25, and 0.25, respectively. In this case, the $C_{\rm FB}$ becomes 375 fF and the mismatch can be reduced. However, the integrating capacitor, C_{I1}, should be scaled up to 3 pF to keep the thermal noise contribution unchanged. This increases chip area. Table I shows the coefficient sets of the RMASH 2-1-$1_{1.5b}$ used in this work, and the proposed RMASH 2-1-$1_{1.5b}$ can achieve a peak SNR of 92 dB and a dynamic range of 95 dB, respectively.

TABLE I
COEFFICIENTS OF RMASH 2-1-$1_{1.5b}$ FOR $\mathrm{OSR} = 16$

Coefficients	Values	Coefficients	Values
g1	0.5	b1	0.25
g2	0.25	a1	2
g3	2	a2	4
g4	2	d2	2

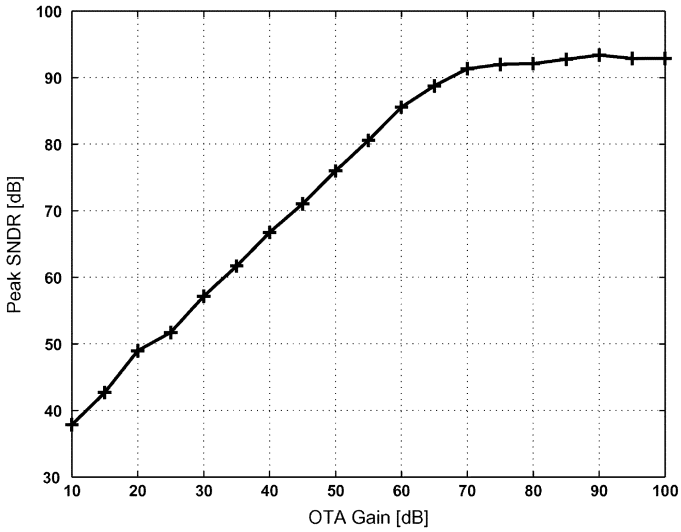

Fig. 9. Plots of simulated SNDR versus OTA dc gain. $(\mathrm{OSR} = 16)$.

D. Integrator Nonidealities

In switched-capacitor (SC) cascaded modulators, the capacitor mismatching and finite OTA gain are two main static nonidealities. These nonidealities can lead to imperfect cancellation of the first- and second-stage quantization noises at modulator output and thus degrade the performance. In addition, in the RMASH 2-1-$1_{1.5b}$, the nonlinearity of tri-level DACs can also introduce distortion to the modulator output, especially for the first-stage DAC. Paper [2] gives the practical model of a nonideal integrator for behavioral simulation to determine the minimum requirement of OTA gain. By applying their model for our simulation, Fig. 9 shows that increasing the finite OTA gain above 70 dB will not significantly improve the performance. So, in our work, we set the finite OTA gain to 70 dB. Given 70-dB OTA gain and 0.5% capacitor mismatching, Fig. 10 illustrates that the RMASH 2-1-$1_{1.5b}$ can achieve a peak SNR of 86 dB.

E. Nonidealities of Tri-Level DAC

The paper [14] has provided a good study and insight for the the nonidealities of tri-level DACs. The first integrator of the tri-level DAC is implemented as shown in Fig. 8. There are three major nonidealities in the tri-level DAC. They are the mismatch of sampling capacitor β_S, the mismatch of integrating capacitor β_I, and the input-referred OTA offset $V_{\rm OS}$.

One may claim other nonideality sources, such as charge injection, parasitic capacitors, and so on. However, these sources are negligible with careful design and layout schemes. To analyze the distortion of the tri-level DAC, we first calculate the

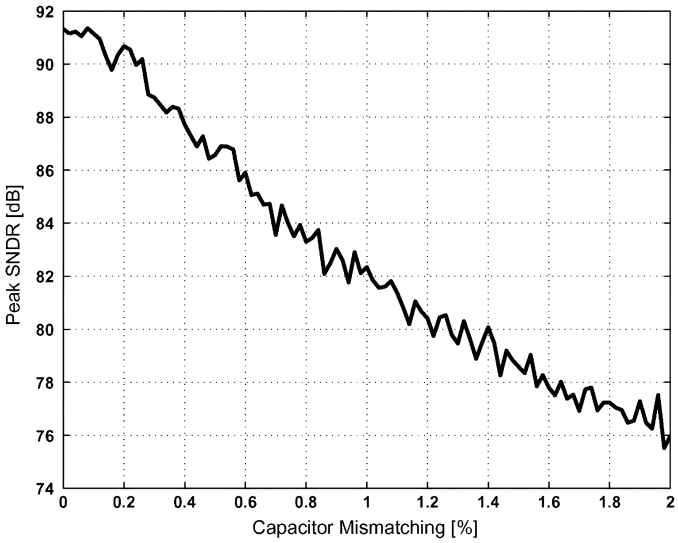

Fig. 10. Plots of simulated SNDR versus capacitor mismatching ($\mathrm{OSR} = 16$).

output voltages for three feedback signals, $\mathrm{A1} = 1, \mathrm{B1} = 1$, and $\mathrm{C1} = 1$

$$V_O^{A1} \cong V_{R+} \cdot \left[\frac{C_S}{C_I}\frac{(1+\beta_S)C_S + (1+\beta_{SI})C_I}{(1+\beta_{SI})C_S + (1+\beta_I)C_I}\right] + V_{\mathrm{OS}} \cdot \left[\frac{C_S}{C_I}\frac{(1+\beta_S)(C_S+C_I)}{(1+\beta_{SI})C_S + (1+\beta_I)C_I}\right] \tag{10}$$

$$V_O^{B1} = 0 \tag{11}$$

$$V_O^{C1} \cong V_{R-} \cdot \left[\frac{C_S}{C_I}\frac{(1+\beta_S)C_S + (1+\beta'_{SI})C_I}{(1+\beta_{SI})C_S + (1+\beta_I)C_I}\right] + V_{\mathrm{OS}} \cdot \left[\frac{C_S}{C_I}\frac{(1+\beta_S)(C_S+C_I)}{(1+\beta'_{SI})C_S + (1+\beta_I)C_I}\right] \tag{12}$$

where $\beta_{SI} = (\beta_S + \beta_I)/2$ and $\beta'_{SI} = (\beta_S + \beta_I + \beta_S\beta_I)/2$.

Accordingly, the nonlinearity factor defined in (5) can be calculated as

$$\varepsilon = \frac{V_O^{A1} + V_O^{C1} - 2V_O^{B1}}{2V_O^{A1}}. \tag{13}$$

By assuming $\beta_S, \beta_I \ll 1$ and $V_{\mathrm{OS}} \ll V_{R+}$ and by substituting (10), (11), and (12) in (13), we can find that

$$\varepsilon = \frac{\beta_S\beta_I}{2}\frac{(1+\beta_I)C_I^2 - (1+\beta_S)C_S^2}{(C_S+C_I)^2} - \frac{V_{\mathrm{OS}}}{V_{R+}}. \tag{14}$$

Since the β_S and β_I are small, the $\beta_S\beta_I/2$, first term of (14), can be considered negligible. By substituting (14) in (5), the discrete-time error function of tri-level DAC approximates

$$e_{\mathrm{DAC}}[k] \approx \frac{V_{\mathrm{OS}}}{V_{R+}}(1 + y_1[k]^2) \tag{15}$$

where V_{OS}, V_{R+}, and $y_1[\mathrm{k}]$ denote the offset voltage of OTA, reference voltage and output of tri-level quantizer, respectively. As shown in (15), the nonideality of tri-level DAC mainly depends on the offset voltage of OTA for a given reference voltage. Fig. 11 shows the simulated dynamic range of RMASH 2-1-$1_{1.5b}$ as a function of offset voltage of OTA. To target the dynamic range of 90 dB, the offset voltage of 5 mV is required. The offset voltage of 5 mV is achievable with carefully sizing and paying attention to layout of the input differential pairs of OTA.

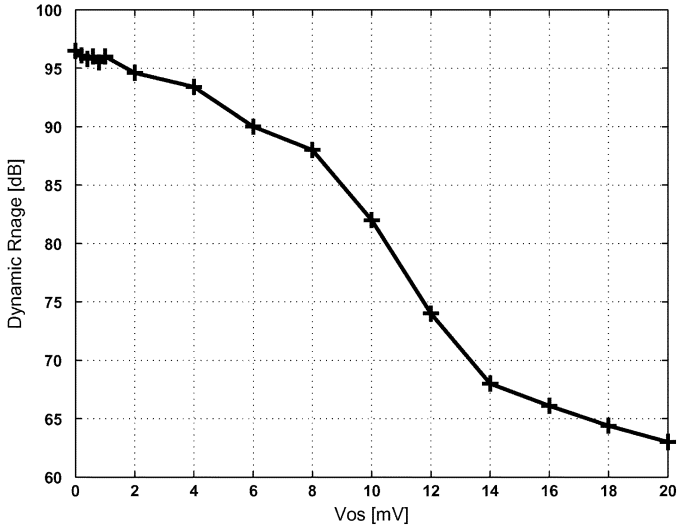

Fig. 11. Plots of simulated dynamic range versus OTA offset voltage. ($\mathrm{OSR} = 16$).

III. Circuit Implementation

A. Specifications for Building Blocks

Upon simulating the behavior of the proposed modulator, we determined the specifications of analog building blocks with consideration of power-performance trade-offs. Table II summarizes the circuit specifications for the 14-bit 5-MS/s RMASH 2-1-$1_{1.5b}$. To evaluate the robustness, we modeled the critical circuit parameters as Gaussian distribution with the standard deviation of 20% and executed the Monte Carlo analysis by using MATLAB. The critical parameters are dc gain, transconductance, unity gain bandwidth (GBW), output current, and input offset of OTAs, on-resistance of switches, and clock jitter. In addition, the standard deviations of integrator and feedforward gains are 0.5% and 2%, respectively. As shown in Fig. 12, the mean, minimum, and standard deviation of peak SNDR are 84.6 dB, 81.5 dB, and 0.72%, respectively.

B. OTA Circuit

According to Table I, the proposed modulator requires the dc gain of 75 dB and the GBW of 300 MHz for the OTA with a supply voltage of 2.5 V. To meet the requirements, we chose a folded-cascode OTA with additional gain-boosting amplifier. By carefully design and sizing of the gain-boosting amplifiers, the induced nondominant pole can be located at 1 GHz. As mentioned in Section II, the output swing of the first-stage integrators can be reduced by using the tri-level quantizer and the input feedforward path. Hence, for a supply voltage of 2.5 V, the required single-ended output swing of OTA is approximately 1 V.

Fig. 13 shows the schematic of the folded-cascode OTA being used for the first-stage integrators. The single-ended output

TABLE II
CIRCUIT SPECIFICATIONS FOR 14-BIT 5 MS/S RMASH $2\text{-}1\text{-}1_{1.5b}$

Optimized Spec. For	14-bit@5MS/s	
Modulator	Topology	RMASH $2\text{-}1\text{-}1_{1.5b}$
	Oversampling ratio	16
	Sampling frequency	80MHz
	Clock jitter	15ps
	Reference voltage	$\pm$0.9V for 1st stage
		$\pm$0.45V for other stages
OTAs	Gm	10mS for 1st stage
		5mS for other stages
	DC-gain	75 dB for 1st stage
		60 dB for other stages
	Output swing range	1.2V
	Max. output current	3mA for 1st stage
		1mA for other stages
	Unity gain bandwidth	300MHz for 1st stage
		200 MHz for other stages
	Input noise	$8\text{nV}/\sqrt{Hz}$
	Input offset	2.5mV
Integrators	Input sampling capacitor	2pF
	Unit capacitor	0.5pF
	Capacitor deviation	0.5%
	Switch on-resistance	150Ω
Comparators	Offset	$\pm$15mV

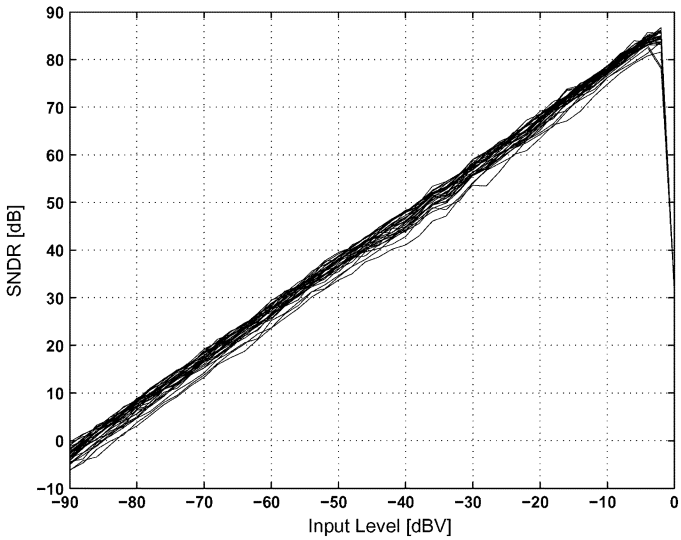

Fig. 12. Plots of simulated SNDR versus input level with 30 Monte Carlo analysis runs.

swing of OTA is 1.4 V, which can sufficiently accommodate the required output swing at the integrator outputs, and a dc gain of 75 dB is accomplished over the entire output range. The OTA, including gain-boosting and biasing circuits, dissipates 15 mW from a 2.5-V supply and achieves a GBW of 300 MHz with a capacitive loading of 5 pF, while the phase margin is 75 degree. The total thermal noise contribution over 2.5-MHz signal bandwidth is about 12.6 μV. The SC common-mode feedback (CMFB) is used for designed OTA because it does not dissipate the static power. The capacitors used in the CMFB circuitry are properly chosen to maximize the gain bandwidth, and thus avoid the settling error. We also used the similar OTA for other stages, and it dissipates 0.7 times of the power consumption the first-stage OTA consumes.

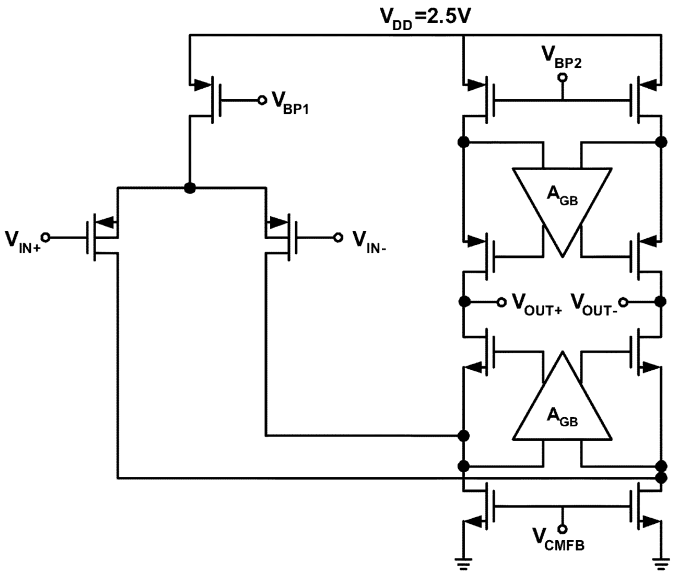

Fig. 13. Circuit schematic of the OTA.

C. First-Stage Circuit

Fig. 14 illustrates the circuit diagram of the first-stage modulator. Since the dynamic range of the modulator is targeted at 90 dB at the sampling rate of 80 MHz, the sampling capacitor is chosen to be 1.5 pF and, accordingly, the integrating and resonator feedback capacitors are 3 and 0.375 pF, respectively. The closed-loop bandwidth of front-end integrator is about 255 MHz, which is larger than three times the sampling frequency. Because the feedback gain of the tri-level DAC is equal to one, we can use the share-capacitor switching technique to eliminate coefficient mismatch. The share-capacitor switching technique is to have the input sampling and feedback DAC share a common sampling capacitor C_{S1} [18]. However, the dependent load on the reference voltage may cause harmonic distortion. In our work, we used a dummy SC network to reduce the distortion [19]. The output two-bit code of tri-level quantizer is used to switch $\mathrm{A}_1, \mathrm{B}_1$, and C_1 at the integrating phase.

The summing circuit in front of the quantizer is implemented by using a passive SC network to avoid the use of additional OTA and save the power dissipation. The summed signal can be expressed as

$$V_S(z) = \frac{C_{\mathrm{FF1}} V_{\mathrm{in}}(z) + C_{\mathrm{FF2}} \mathrm{Int1}(z) + C_{\mathrm{FF3}} \mathrm{Int2}(z)}{C_{\mathrm{FF1}} + C_{\mathrm{FF2}} + C_{\mathrm{FF3}}} \quad (16)$$

where $C_{\mathrm{FF1}}, C_{\mathrm{FF2}}$, and C_{FF3} are the capacitors for feedforward gains. According to behavioral simulation, the feedforward gains are not critical and can tolerate the variation up to 2%. This allows the use of small capacitance to implement the feedforward gains. We set the values of $C_{\mathrm{FF1}}, C_{\mathrm{FF2}}$, and C_{FF3} to 0.125, 0.25, and 0.5 pF, respectively. Note that the summed signal is scaled down by 1/7 when comparing with the parameters of Table I and Fig. 1. In order not to affect the desired performance of the modulator, the reference voltages of the quantizers must be scaled down by a factor of 1/7 from the nominal value. This also scales down the quantizer step size, and hence increases the requirement of the comparator resolution. In our case, the required step size of the tri-level quantizer is about 150 mV. This requirement is feasible because, in practice, the

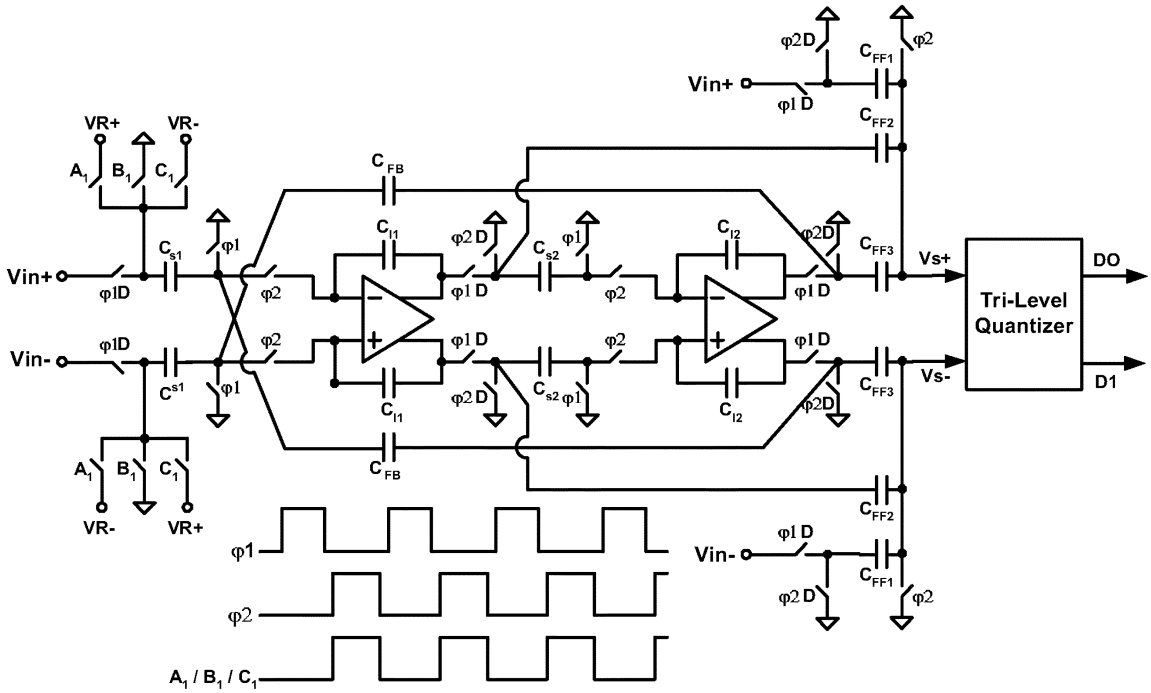

Fig. 14. Circuit implementation of the first-stage modulator.

CMOS comparator with preamplifier can provide a resolution better than 50 mV.

D. Tri-Level Quantizer Circuit

The circuit diagram of tri-level quantizer is shown in Fig. 15. As mentioned above, the SC network must scale down the reference voltages, VR+ and VR-, by a factor of 1/7. So, we set the values of the capacitors C_{Q0} and C_{Q1} to 0.125 pF and 0.75 pF, respectively. In our design, we used a high-speed, high-accuracy CMOS comparator with preamplifier which is presented by [20]. The clock $\varphi 2\mathrm{A}$ is used to control the generation of $\mathrm{A}_1, \mathrm{B}_1$, and C_1. Because of the time-delay of AND gates, the nonoverlapping interval of $\varphi 2\mathrm{A}$ is limited to 1–2 ns when a sampling rate of 80 MHz.

E. Reference Buffer Circuit

Since the first integrator samples the input signal, it draws a signal-dependent current from the voltage reference and introduces harmonic distortion due to the finite output impedance of reference buffers. Our design requires a high-bandwidth reference voltage buffer. The reference buffer must have fast settling behavior during the integrating phase $\varphi 2$. However, such kind of reference buffer is power-consuming, especially for high signal-bandwidth design. In this work, we used a class-A amplifier with an external capacitor to make output impedance low enough to meet desired linearity requirement [21]. The schematic of the class-A amplifier is shown in Fig. 16. The output impedance of the amplifier increases with frequency due to its finite gain-bandwidth product. Because of the large external capacitor, the output impedance remains low in high-frequency band. That is, the transient charge of the reference voltage is almost delivered from the external capacitor. Fig. 16(b) shows the decoupling scheme of TPRVs used in the printed circuit board (PCB). The decoupling capacitors C_{mid1} and C_{mid2} are important because

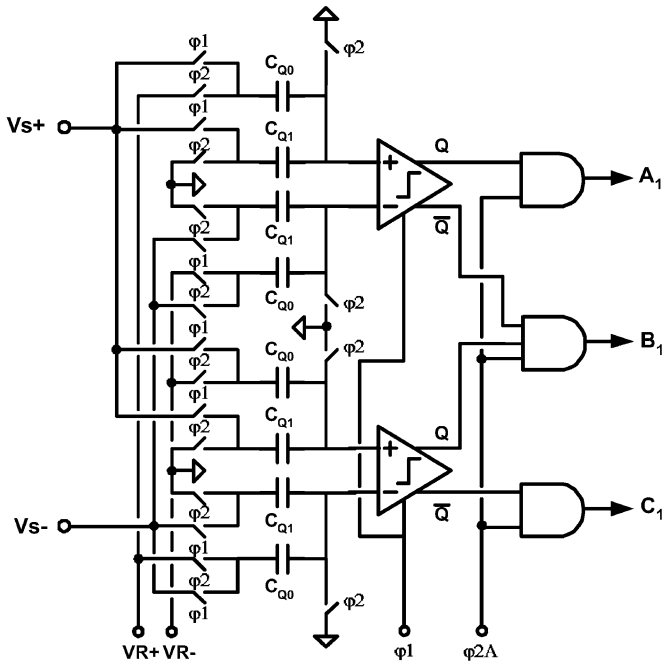

Fig. 15. Circuit implementation of tri-level quantizer.

they can reduce high-frequency common-mode noise between the differential reference voltages. By using this topology, the reference buffer in first stage consumes only 5 mW at the cost of using large external decoupling capacitors. The buffers for the reference voltages of the second and third stages are similar to Fig. 16, but dissipate approximately half of that of the first stage. This arrangement is practical because the settling errors of reference voltages in the second and third stages will be suppressed by the high-pass noise shaping of $H_1(z)$ and $H_2(z)$, respectively.

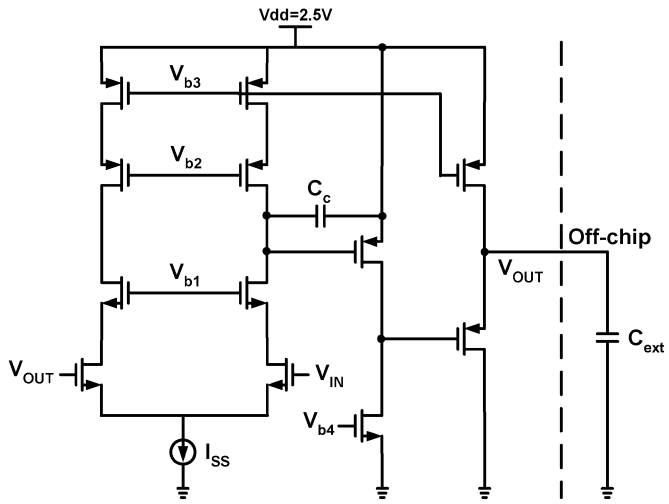

Fig. 16. (a) The schematic of the voltage buffer amplifier. (b) The off-chip decoupling scheme of reference voltages.

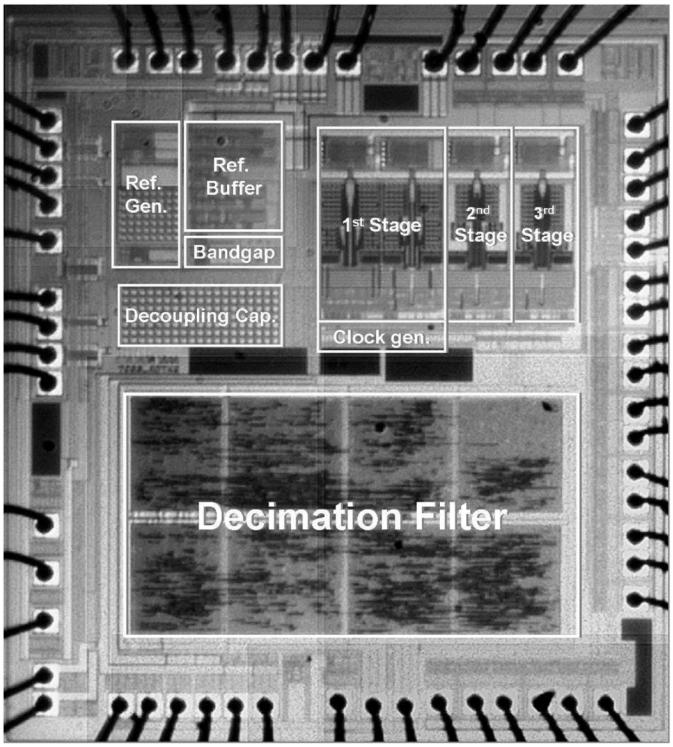

Fig. 17. Chip micrphotograph.

IV. Experimental Results

The modulator is designed for a sampling rate of 80 MHz and a fixed OSR of 16; so, the signal bandwidth is 2.5 MHz. The signal bandwidth is slightly larger than the requirement of ADSL2+ (say 2.2 MHz) because we intend to reduce the cost of the decimation filter. Increasing the signal bandwidth from 2.2 to 2.5 MHz makes the required order of decimation filter lower. The modulator was fabricated in a 0.25-μm 1P5M CMOS technology with metal–insulator–metal (MIM) capacitors. In the experiment, to fairly compare with existing wide-band $\Sigma\Delta$ modulators, we collected the results without counting the decimation filter part. The active area of the modulator is 1.2 mm2. The power dissipation of the modulator with I/O pads is 62.5 mW with a 2.5-V supply while the core of modulator consumes 53 mW. Fig. 17 shows the chip microphotograph in which the experimental modulator includes the clock generator, reference buffer, and bandgap circuitry. To measure the performance data, the chip was mounted onto a four-layer printed circuit board to separate the analog signal from digital signal and hence reduce the coupling. The input clock is generated from an external 80-MHz low-jitter crystal with independent power supply voltages to avoid the switching-noise coupling. Fig. 18 shows that the modulator can achieve a dynamic range of 86 dB, a peak SNR of 83 dB, and a peak SNDR of 78.5 dB for a 2.5-MHz signal band.

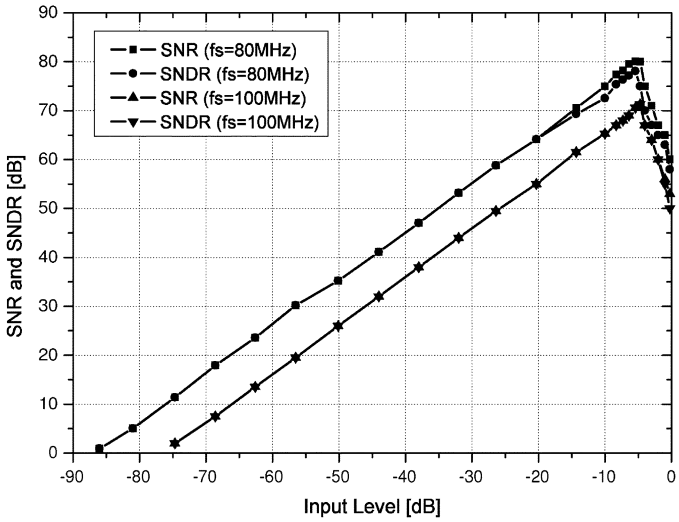

Fig. 18. Plots of measured SNDR and SNR versus input signal level.

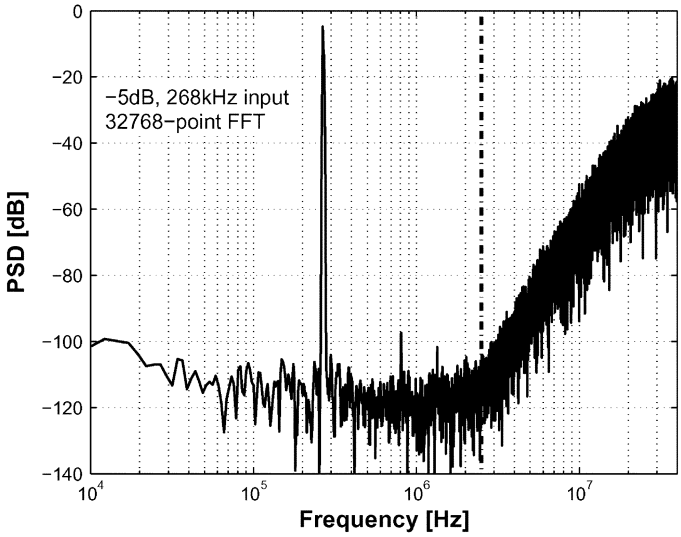

Fig. 19. Measured output PSD of RMASH 2-1-$1_{1.5b}$ operating at 80-MHz sampling rate.

Fig. 19 illustrates the unfiltered power spectral density (PSD) of the measured output signal; the input sinusoid is -5 dB and 268 kHz. The result implies that the spurious-free dynamic range (SFDR) is 93 dB. When the modulator operates at a sampling rate of 100 MHz, as shown in Fig. 20, it still stay functional without significant harmonic distortion and can achieve a SFDR of 90 dB. However, because of the switching activity of the digital output buffers, the in-band noise floor

TABLE III
CIRCUIT SPECIFICATIONS FOR 14-BIT 5 MS/S RMASH 2-1-$1_{1.5b}$

Refs	Topology	Bandwidth (MHz)	OSR	SNDR/DR (dB)	Technology (CMOS)	Die Size (mm2)	Power (mW)	FOM (pJ/conv)
[4]	5th	2	8	82 / 83	0.18-μm 1.8V	2.9	150	3.25
[5]	2nd	1.92	12	70 / 76	0.18-μm 2.7V	1.4	50	2.53
[6]	4th	2	12	74 / 80	0.25-μm 2.5V	2.6	105	3.21
[7]	2-2-1	2	16	87 / 95	0.5-μm 2.5V	10	150	0.82
[9]	2-1-1	2.2	16	72.7 / 78	0.25-μm 2.5V	2.78	65.8	2.3
this work	2-1-1	2.5	16	78.5 / 86	0.25-μm 2.5V	1.2	62.5	0.77
		3.125		72 / 77.5			65	1.69

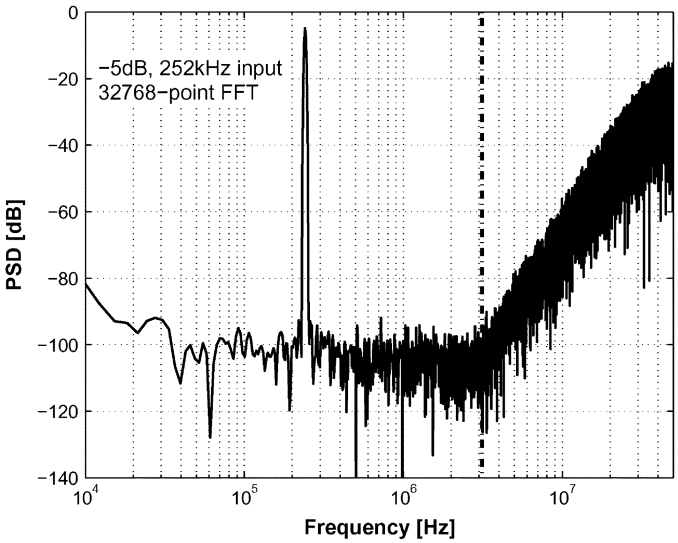

Fig. 20. Measured output PSD of RMASH 2-1-$1_{1.5b}$ operating at 100-MHz sampling rate.

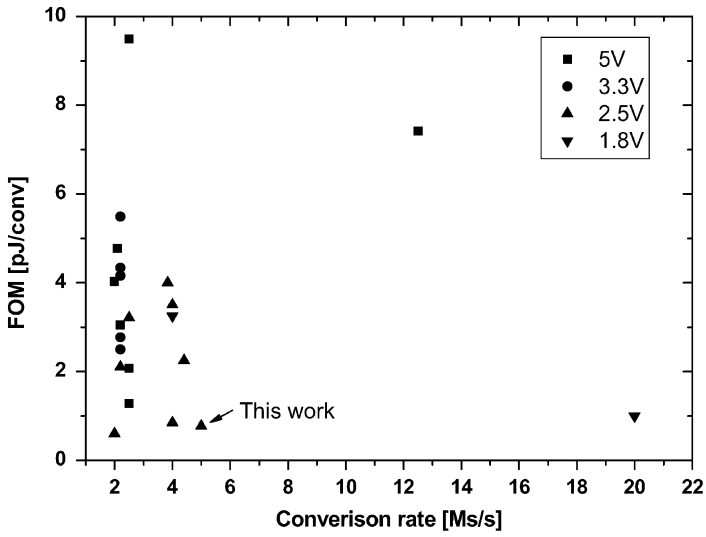

Fig. 21. FOM distribution of wide-band SC ΣΔ modulators with respect to conversion rate.

rapidly increases at the pad-pin level, and the dynamic range and peak SNDR become 77.5 and 72 dB, respectively, for a 3.125-MHz bandwidth.

To quantitatively evaluate the efficiency among power dissipation, dynamic range, and conversion rate, we use the formulas for the effective number of bits (ENOB) of ADC and the figure-of-merit (FOM) as shown below [9], [22]

$$\text{ENOB} = \frac{\text{dynamic range} - 1.76}{6.02}$$
$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \times \text{Conversion Rate}} 10^{12}. \quad (17)$$

Fig. 21 shows the FOM distribution of our work and existing wide-band (>1 MHz) SC ΣΔ modulators. Table III summarizes the measured performance and specifications of the proposed modulator, and compares with the other wide-band SC ΣΔ modulators as well.

V. CONCLUSION

This work addresses a low-power low-cost cascaded ΣΔ modulator architecture appropriate for ADSL2+ application. This work uses three approaches to improve performance and reduce power consumption: using the resonator-based topology, applying the tri-level quantization, and using two pairs of reference voltages. The proposed modulator has been fabricated in TSMC 0.25-μm 1P5M CMOS technology. Including reference voltage buffers and bandgap circuitry, the chip dissipates 62.5 mW from a 2.5-V supply. As shown in the experimental result, the designed RMASH 2-1-$1_{1.5b}$ can achieve a peak SFDR of 93 dB, a dynamic range of 86 dB, a peak SNDR of 78.5 dB, and a low FOM of 0.77 pJ/conv with the OSR of 16 and bandwidth of 2.5 MHz.

ACKNOWLEDGMENT

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REFERENCES

[1] A. M. Marques, V. Peluso, M. S. J. Steyaert, and W. Sansen, "A 15-b resolution 2-MHz nyquist rate ADC in a 1-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 1065–1075, Jul. 1998.

[2] Y. Geerts, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 3.3-V, 15-bit, delta-sigma ADC with a signal bandwidth of 1.1 MHz for ADSL applications," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 927–936, Jul. 1999.

[3] Y. Geerts, M. S. J. Steyaert, and W. Sansen, "A high-performance multibit ΔΣ CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1829–1840, Dec. 2000.

[4] R. Jiang and T. S. Fiez, "A 14-bit $\Sigma\Delta$ ADC with 8x OSR and 4-MHz conversion bandwidth in a 0.18-μm CMOS process," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 63–74, Jan. 2004.
[5] M. R. Miller and C. S. A. Petrie, "A multibit sigma-delta ADC for multimode receivers," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 475–482, Mar. 2003.
[6] T.-H. Kuo, K.-D. Chen, and H.-R. Yeng, "A wide-band CMOS sigma-delta modulator with incremental data weighted averaging," *IEEE J. Solid-State Circuits*, vol. 37, no. 1, pp. 2–10, Jan. 2002.
[7] K. Vleugels, S. Rabii, and B. A. Wooley, "A 2.5-V sigma-delta modulator for broadband communications applications," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1887–1899, Dec. 2001.
[8] S. K. Gupta and V. Fong, "A-64-MHz clock-rate $\Sigma\Delta$ ADC with 88-dB SNDR and 105-dB IM3 distortion at a 1.5-MHz signal frequency," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1653–1661, Dec. 2002.
[9] R. delRio, "Highly linear 2.5-V CMOS $\Delta\Sigma$ modulator for ADSL+," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 1, pp. 47–62, Jan. 2004.
[10] R. Reutemann, P. Balmelli, and Q. Huang, "A 33 mW 14b 2.5 Msample/s $\Delta\Sigma$ A/D converter in 0.25-μm digital CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2002, pp. 316–317.
[11] , S. R. Norsworthy, R. Schreier, and G. C. T. , Eds., *Delta-Sigma Data Converters: Theory, Design, and Simulation*. New York: IEEE Press, 1996.
[12] A. A. Hamoui and W. Martin, "High-order multibit modulators and pseudo data-weighted-averaging in low oversampling $\Sigma\Delta$ ADCs for broadband applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 1, pp. 72–85, Jan. 2004.
[13] K. Nam, S.-M. Lee, D. K. Su, and B. A. Wooley, "A low-voltage low-power sigma-delta modulator for broadband analog-to-digital conversion," *IEEE J. Solid-State Circuits*, vol. 40, pp. 1855–1864, Sep. 2005.
[14] P. Balmelli, "Broadband sigma-delta A/D converters," Ph.D. dissertation, Swiss Federal Institute of Technology, Zurich, Switzerland, 2003.
[15] F. Medeiro, B. Perez-Verdu, J. M. Rosa, and A. Rodriguez-Vazquez, "Fourth-order cascade SC $\Sigma\Delta$ modulator: A comparative study," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 45, no. 10, pp. 1041–1051, Oct. 1998.
[16] R. Schreier, "An empirical study of higher order single-bit delta-sigma modulators," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 40, no. 8, pp. 461–466, Aug. 1993.
[17] J.-B. Shyu, G. C. Temes, and F. Krummenacher, "Random error effects in matched MOS capacitor and current sources," *IEEE J. Solid-State Circuits*, vol. SC-19, no. 6, pp. 948–955, Dec. 1984.
[18] D. Ribner, R. Baertsch, S. Garverick, D. McGrath, J. Krisciunas, and T. Fujii, "A third-order multistage sigma-delta modulator with reduced sensitivity to nonidealities," *IEEE J. Solid-State Circuits*, vol. 26, no. 6, pp. 1764–1774, Dec. 1991.
[19] I. Fujimori, K. Koyama, D. Trager, F. Tam, and L. Longo, "A-5 V single-chip delta-sigma audio A/D converter with 111 dB dynamic range," *IEEE J. Solid-State Circuits*, vol. 32, no. 3, pp. 329–336, Mar. 1997.
[20] G. Yin, F. O. Eynde, and W. Sansen, "A high-speed CMOS comparator with 8-b resolution," *IEEE J. Solid-State Circuits*, vol. 27, Feb. 1992.
[21] P. C. Maulik, "A 16-bit 250-kHz delta-sigma modulator and decimation filter," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 458–467, Apr. 2000.
[22] F. Goodenough, "Analog techniques of all varieties dominate ISSCC," *Electron. Design*, vol. 44, pp. 96–111, Feb. 1996.

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