Carrier Transportation Mechanism of the $TaN/HfO_2/IL/Si$ Structure With Silicon Surface Fluorine Implantation

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***Abstract*—In this paper, the current transportation mechanism of HfO_2 gate dielectrics with a TaN metal gate and silicon surface fluorine implantation is investigated. Based on the experimental results of the temperature dependence of gate leakage current and Fowler–Nordheim tunneling characteristics at 77 K, we have extracted the current transport mechanisms and energy band diagrams for $TaN/HfO_2/IL/Si$ structures with fluorine incorporation, respectively. In particular, we have obtained the following physical quantities: 1) fluorinated and as-deposited interfacial layer (IL)/Si barrier heights (or conduction band offsets) at 3.2 and 2.7 eV; 2) TaN/fluorinated and as-deposited HfO_2 barrier heights at 2.6 and 1.9 eV; and 3) effective trapping levels at 1.25 eV (under both gate and substrate injections) below the HfOF conduction band and at 1.04 eV (under gate injection) and 1.11 eV (under substrate injection) below the HfO_2 conduction band, which contributes to Frenkel–Poole conduction.**

***Index Terms*—Current transport, fluorinated HfO_2, fluorine implantation.**

I. Introduction

HIGH-k gate dielectrics as an alternative to conventional SiO_2 gate oxides are widely investigated for their capability to reduce gate leakage current for the same electrical capacitance [1]–[3]. Among all high-k gate materials, hafnium-based dielectrics are considered the most promising candidates, or at least the most studied, due to their excellent thermal stability, wide bandgap, and high dielectric constant [4]–[6]. Nevertheless, the metal-gate electrode has also attracted attention as a solution to the polydepletion effect that appears under gate inversion conditions in poly-Si gates, as well as the incompatibility between some high-k materials and poly-Si [7]. As a result, metal-gate/high-k stacks have been explored in recent years [7]–[10].

However, HfO_2 gate dielectrics with fluorine incorporation could also exhibit better dielectric performance and reliability [11]–[15]. F incorporation into a HfSiON dielectric has been shown to be highly effective in lowering V_{th} and improving negative bias temperature instability in p-channel field-effect transistors, and the drive current could aggressively be increased [11]. F is believed to form stronger Hf–F and Si–F bonds than Hf–H and Si–H bonds, which improves the reliability of HfO_2/SiO_2 [12]. Recently, we have also documented several studies of ultrathin fluorinated HfO_2 gate dielectrics. First, the thermal stability of HfO_2 gate dielectrics can be much improved by fluorine ion implantation on the silicon surface [16]. Second, the interfacial layer (IL; between HfO_2 film and Si substrate) formation can effectively be suppressed by a pre-CF_4 plasma treatment [17]. Third, the charge-trapping phenomenon can largely be eliminated for the HfO_2 gate dielectrics fluorinated by a postdeposition CF_4 plasma treatment [18]. Although several recent studies have investigated fluorinated HfO_2 gate dielectrics [11]–[18], its carrier transport mechanisms have not been well investigated. Only a few studies have demonstrated the carrier transport and tunneling mechanisms of conventional HfO_2 gate dielectrics [19]–[21], and none have explored fluorinated HfO_2 gate dielectrics. Electron transport in high-k gate dielectrics will instead be governed by a trap-assisted mechanism, such as Frenkel–Poole (F–P) conduction or hopping conduction, due to the charge-trapping phenomenon. In order to explain higher current density traps in the band gap of the high-k dielectrics, charge trapping has to be assumed. In the known trap-assisted tunneling (TAT) models and the F–P conduction mechanism, the current density only linearly depends on the trap concentration [22]. In addition, in previous studies [22]–[31], the F–N tunneling is usually used for current transport analysis of high-k gate stacks. The F–N fitting can be used for the high-k gate insulator of a MOS capacitor, whereas the gate insulator is a dielectric bilayer [22]–[28] or oxide–nitride–oxide (ONO) stacks [29]–[31] in order to extract the tunneling barrier. On the other hand, the band diagram of the metal/HfO_2/Si capacitor has been investigated, although without consideration of the IL [19]. However, the IL is a critical issue for high-k gate dielectrics and, therefore, deserves an in-depth discussion.

Manuscript received August 2, 2007; revised March 27, 2008. This work was supported by the National Science Council, R.O.C., under Contract NSC-94-2215-E-182-008. The review of this paper was arranged by Editor J. Suehle.

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Digital Object Identifier 10.1109/TED.2008.925150

0018-9383/$25.00 © 2008 IEEE

In this paper, we investigate the carrier transportation mechanism in devices integrating both HfO_2 gate dielectrics with and without fluorine incorporation and a metal gate (TaN). We present new accurate characterizations of TaN/as-deposited and fluorinated HfO_2/Si capacitors, including F–P conduction and Fowler–Nordheim (F–N) tunneling, under both gate and substrate injection modes. The strong temperature dependence of the gate leakage current suggests that the current tunneling mechanism is F–P conduction for both as-deposited and fluorinated HfO_2 gate dielectrics. The effective extracted trapping level of fluorinated HfO_2 gate dielectrics is, thus, larger than the as-deposited one. We also report the F–N tunneling characteristics at 77 K, from which we can deduce the energy band diagrams for $TaN/HfO_2/IL/Si$ and $TaN/HfOF/(IL + F)/Si$ structures, as well as their current transport mechanisms.

II. Experiment

The devices used in this paper were MOS capacitors fabricated on p-Si(100) wafers. First, standard RCA cleaning was performed on all samples. Then, 30-nm screen oxide films were grown in order to prevent implantation damage. Fluorine ions were implanted through the 30-nm screen oxide films at a low energy of 25 keV, with different dosages ranging from $1 \times 10^{13}/cm^2$ to $1 \times 10^{15}/cm^2$, designated F 1E13, F 1E14, and F 1E15 (without F implantation, which is denoted as-dep.), respectively. Then, annealing in a N_2 ambient at 850 °C for 30 min was performed to remove any implant-induced damage. At that time, the fluorine atoms diffused into the silicon surface.

Before HfO_2 thin-film deposition, the 30-nm screen oxide was removed by a wet HF solution. Then, a HfO_2 thin film was then deposited on a HF-last Si surface by an electron beam evaporation system. For the HfO_2 thin-film crystallization study, some samples were annealed by rapid thermal annealing (RTA) in the N_2 ambient for 30 s at 600 °C. The HfO_2 thin film was crystallized after the 600 °C RTA, as approved in X-ray diffraction analysis (not shown here). A metal gate (TaN) film of 50 nm was deposited by reactive RF sputter for all samples. Thereafter, a 300-nm-thick Al film was deposited on the TaN film by a thermal evaporator. The gate of the capacitor was lithographically defined and etched. Finally, a 300-nm-thick Al film was also deposited on the backside of the wafer to form the ohmic contact.

The electrical properties were analyzed by an HP 4285 LCR meter for capacitance–voltage (C–V) characteristics at 100 kHz, and the capacitance effective thickness (CET) was extracted from the capacitance under the accumulation region without consideration of the quantum effects. The current–voltage (I–V) curves were measured by a Keithley 4200 semiconductor characterization system. Furthermore, the I–V characteristics were measured at elevated (318–373 K) and low temperatures (77 K) in order to study the current transportation and band diagram of the MOS capacitor, respectively. Moreover, the physical thickness was checked by transmission electron microscopy (TEM) to obtain the dielectric constant of the HfO_2 thin film.

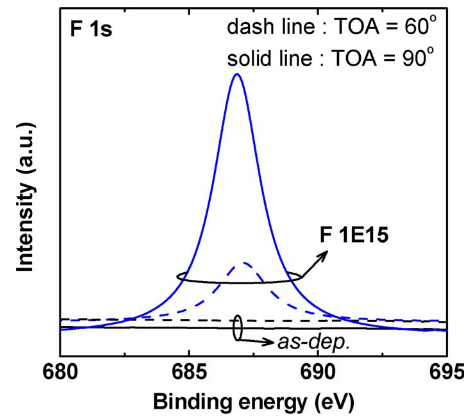

Fig. 1. XPS analysis of the F 1s electronic spectra of as-deposited and fluorinated samples. TOAs of 60° and 90°, respectively.

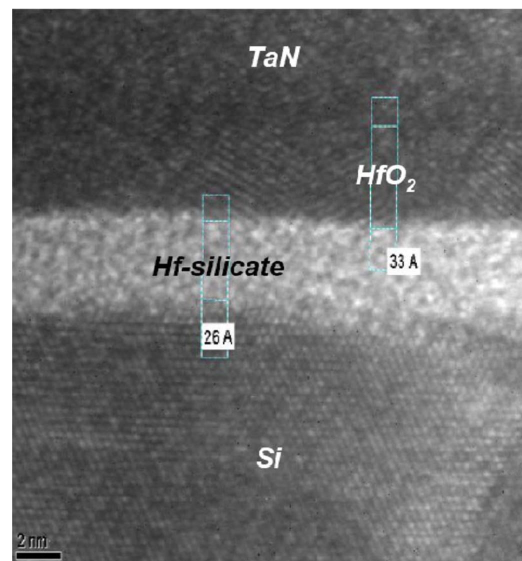

Fig. 2. TEM image of the $TaN/HfO_2/IL/Si$ MOS structure with fluorine incorporation (F 1E15) with 600 °C PDA.

III. Results and Discussion

Takeoff angles (TOAs) of 60° and 90° were used to measure the X-ray photoelectron spectroscopy (XPS) spectra of surface and bulk HfO_2 thin films with fluorine incorporation (Fig. 1). In Fig. 1, for all samples except the as-deposited sample, a distinct F 1s peak at 687 eV can be observed. The silicon surface fluorine implantation (SSFI) processes are apparently introducing fluorine atoms into the dielectrics to form the HfOF gate dielectrics. However, the fluorine intensity was larger for the TOA = 90° than the TOA = 60°, indicating that less fluorine would distribute in bulk HfO_2 gate dielectrics. Fig. 2 shows the TEM image of the $TaN/HfO_2/IL/Si$ structure with fluorine incorporation $(1 \times 10^{15}/cm^2)$ and 600 °C postdeposition annealing (PDA). The great quality of the HfO_2 thin film was demonstrated in this paper, as shown in Fig. 2. As discussed before, physical vapor deposited HfO_2 thin films tend to have ILs at the HfO_2/Si interfaces, as shown in the TEM images. In addition, the composition of the IL is believed to be hafnium silicate, because the estimated dielectric constant of the IL is higher than that of the SiO_2. Furthermore, the

thicknesses of HfO_2 and Hf-silicate were about 3.3 and 2.6 nm, respectively. As a result, the k value of the HfOF (with Hf-silicate) thin film was about 14. In this paper, the carrier transportation mechanism of both as-deposited and fluorinated HfO_2 gate dielectrics was investigated while taking into account the Hf-silicate IL.

Fig. 3(a) and (b) shows the gate current density versus the gate voltage (J–V) characteristics of all samples with and without 600 °C RTA under gate and substrate injection modes, respectively. As we can see, the gate leakage current of the sample without fluorine implantation was much larger than that of films with fluorine incorporation under both gate and substrate injection modes. Both the leakage current and the breakdown voltage were improved for the sample with fluorine incorporation. Furthermore, these characteristics were improved as the fluorine implantation dosage increased, as illustrated in this figure. In addition, the gate leakage current increased for the samples with 600 °C RTA, owing to HfO_2 thin-film crystallization. However, the gate leakage current reduction may still be observed for the fluorinated samples, as shown in Fig. 3. The gate leakage current for the samples with fluorine incorporation was much smaller than that of the samples without fluorine incorporation, whereas the CET was also decreased for fluorinated samples with and without 600 °C PDA (Fig. 4). The decrease in CET for the samples with 600 °C PDA resulted from densification of the HfO_2 thin film. However, the HfO_2 films with fluorine incorporation appeared to possess properties superior to those of the as-deposited samples, including thin equivalent oxide thickness and low leakage current. Fig. 4 demonstrates the relationship between gate leakage current density at $V_G = V_{\mathrm{FB}} - 1$ V and capacitance equivalent oxide thickness for all samples. The gate leakage current density of the sample with 1×10^{15} cm^{-2} F implantation displayed a two-order-of-magnitude improvement by comparison with the as-deposited sample with PDA at 600 °C under the gate injection mode. The same tendency was shown in the CET performance. Even after PDA at 600 °C, a low CET (16.9 Å) was obtained, whereas the leakage current was kept at less than 0.01 $\mathrm{mA/cm^2}$ for the HfO_2 films with fluorine incorporation under substrate injection. The gate leakage current reduction of the F-incorporated HfO_2 gate dielectrics can be explained by F-atom incorporation into the HfO_2 layer. The fluorine atoms can be bonded to Hf (or Si) dangling bonds, resulting in annihilation of oxygen vacancies. In addition, the fluorine incorporation will effectively eliminate some shallow traps in HfO_2 thin films, resulting in lower F–P conduction leakage current for fluorinated HfO_2 gate dielectrics [16], [18]. This shallow trap elimination will be discussed in the next paragraph. Fig. 5 shows the Weibull distribution plots of the gate leakage current density at $V_G = V_{\mathrm{FB}} - 1$ V for all samples. Both the performance and uniformity distribution of the fluorinated HfO_2 gate dielectrics were superior to those of the as-deposited samples under both gate and substrate injection modes, without an increase in the CET.

The temperature dependence of the gate leakage current was studied to understand the current transport mechanisms. The gate leakage currents were measured from 318 to 373 K, as shown in Fig. 6(a) and (b) for gate electron injection

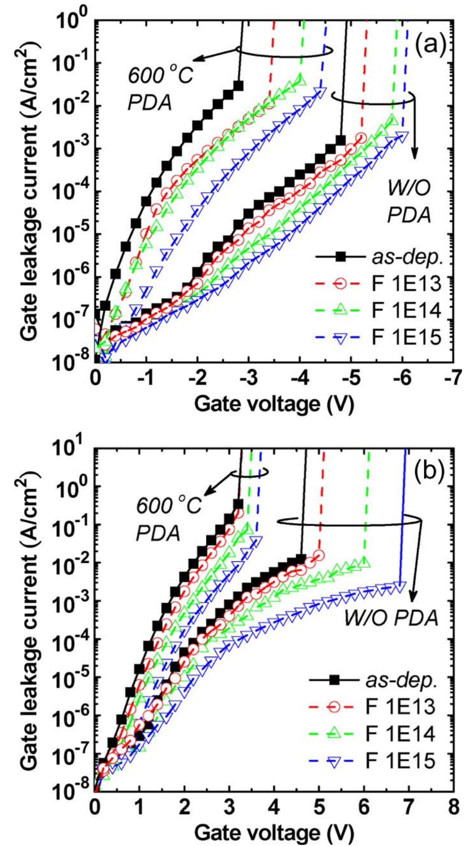

Fig. 3. I–V characteristics for the as-deposited and fluorinated HfO_2 gate dielectrics with and without PDA under (a) gate injection and (b) substrate injection.

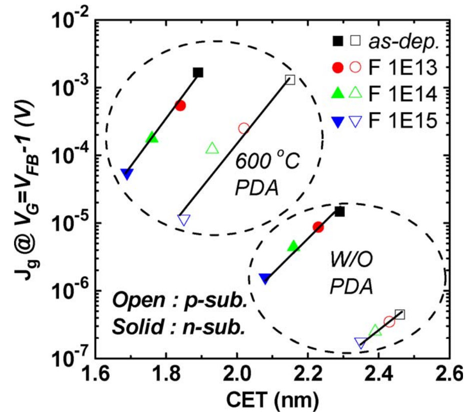

Fig. 4. Relationship between gate leakage current and CET for all samples. The fluorinated HfO_2 gate dielectrics have lower leakage current and CET.

(negative V_G) and in Fig. 6(c) and (d) for substrate electron injection (positive V_G). The gate leakage current increases with increasing measuring temperature under both gate and substrate injections for all samples, thus showing obvious temperature dependence. As a result, the commonly used equations for direct and F–N tunnelings do not fit the experimental current density of the high-k dielectrics, which are larger by orders of magnitude than the calculated currents. To further investigate the carrier transportation of as-deposited and fluorinated HfO_2 gate dielectrics with and without RTA, the F–P conduction fitting is performed, as shown in the inset of

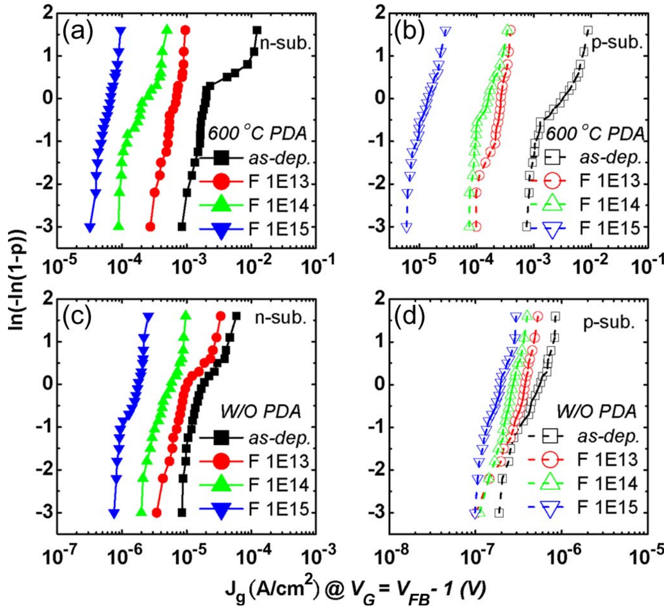

Fig. 5. Weibull distribution of gate leakage current for the as-deposited and fluorinated HfO_2 gate dielectrics under (a), (c) gate injection and (b), (d) substrate injection. A good distribution performance of the fluorinated HfO_2 gate dielectrics was observed.

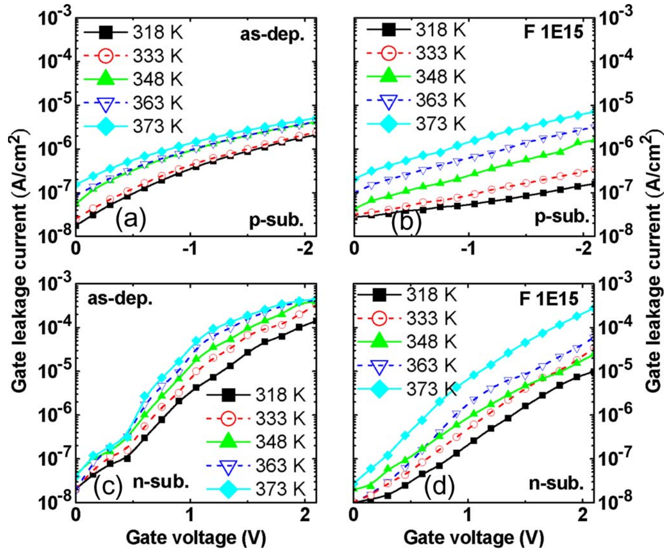

Fig. 6. Temperature dependence of gate leakage current increase for (a), (c) as-deposited and (b), (d) fluorinated HfO_2 (with F 1E15 SSFI) gate dielectrics under (a), (b) gate injection and (c), (d) substrate injection.

Fig. 7. The data in the inset of Fig. 7 were extracted from the good F–P fitting [22] $(J = E_{\mathrm{OX}} \times \exp\{-q[\Phi_B - (qE_{\mathrm{OX}} - \pi\varepsilon_i)^{1/2}]/kT\})$, where Φ_B is the effective F–P barrier, and ε_i is the dielectric constant of SiO_2. The electric field $E_{\mathrm{OX}} = V/T_{\mathrm{OX}}$ is an "effective" electric field because T_{OX} is the CET. As a result, Φ_B is named the effective F–P barrier, which is determined by the effective electric field E_{OX}. In addition, as described in Fig. 2, there is an interfacial oxide layer between HfO_2 and Si. Therefore, the barrier parameters to be discussed in this paper are "effective" values that include the effects of these ILs [19]. Both gate and substrate injections were aggressively studied, as shown in this figure. It should be noted

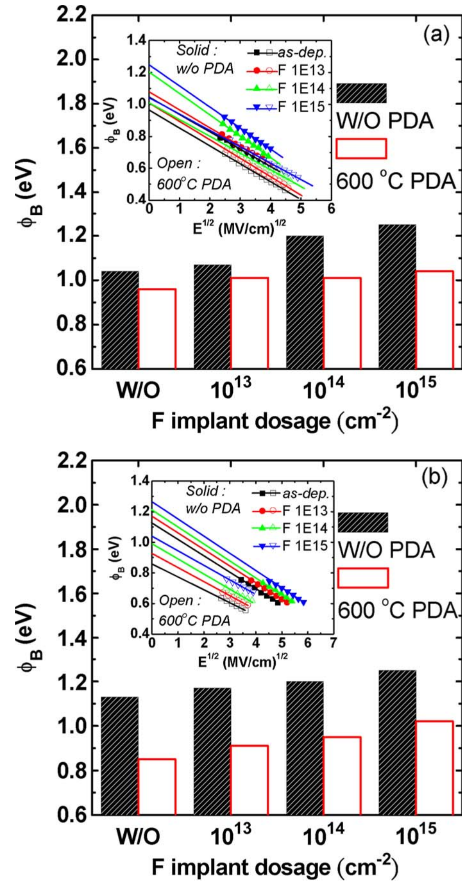

Fig. 7. Effective F–P trapping level for the as-deposited and fluorinated HfO_2 gate dielectrics under (a) gate injection and (b) substrate injection. Inset shows the F–P curve fit for all samples.

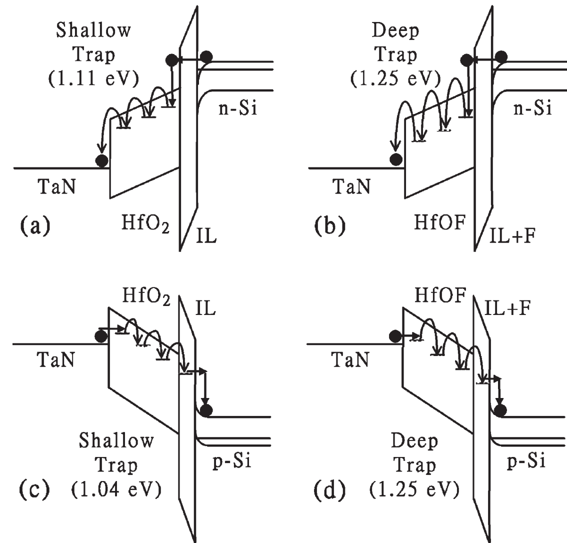

Fig. 8. Physical model of (a), (c) as-deposited and (b), (d) fluorinated gate dielectrics for F–P conduction under (a), (b) substrate injection and (c), (d) gate injection.

that this effective barrier height includes the effect of the IL between HfO_2 and Si. The extracted trap energy Φ_B under substrate injection for the as-deposited sample is 1.11 eV from the conduction band of HfO_2, whereas that of the fluorinated sample (F 1E15) is about 1.25 eV. Similarly, the extracted

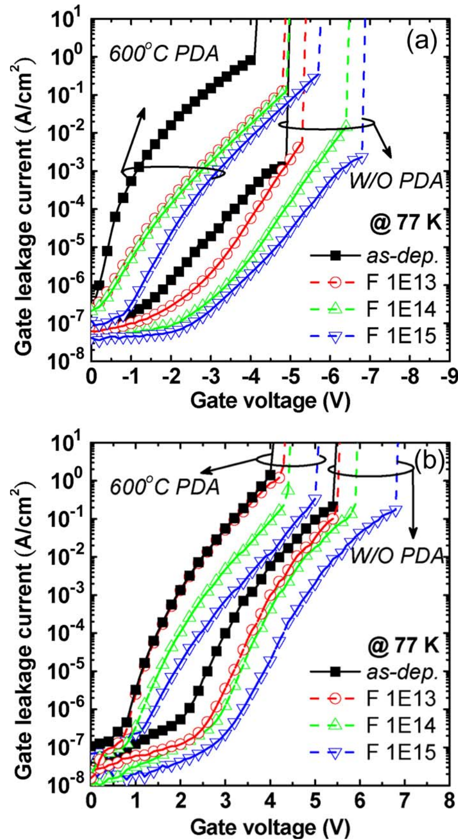

Fig. 9. I–V characteristics at 77 K measured for the as-deposited and fluorinated HfO$_2$ gate dielectrics with and without PDA under (a) gate injection and (b) substrate injection.

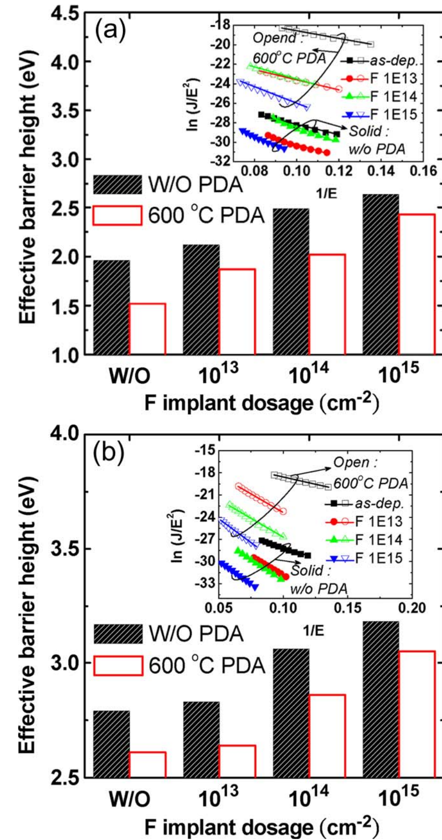

Fig. 10. Effective F–N barrier height for the as-deposited and fluorinated HfO$_2$ gate dielectrics under (a) gate injection and (b) substrate injection. Inset shows the well FN fitting for all samples.

trap energy under gate injection for the as-deposited sample is 1.04 eV from the conduction band of HfO$_2$, whereas that of the fluorinated sample (F 1E15) is about 1.25 eV. As the F-implant dosage increases, the increase in the effective trapping level is easily observed, which means that most of the shallow traps in the HfO$_2$ film can be eliminated using this fluorine implantation technique. In addition, the decreased effective trapping level can be observed for the annealed samples. The gate leakage current will increase for the annealed samples, owing to film crystallization discussed earlier. As a result, the effective trapping level extracted from F–P conduction current will decrease, as shown in this figure. Furthermore, the Schottky emission barrier $(J = A^*T^2 \exp[-q(\Phi_B - \sqrt{qE/4\pi\varepsilon I})/kT])$ was also calculated. The Schottky emission barrier Φ_B is also an effective barrier, as previously mentioned. Moreover, A^* is the Richardson's constant, and E is an effective electric field. The same as F–P conduction, the gate current of Schottky emission will be dependent on temperature variation. This obvious temperature dependence of the gate leakage current was shown in Fig. 6. However, because the barrier height extracted from Schottky emission was larger than the trap energy extracted from F–P conduction, the F–P conduction mechanism would dominate the Schottky emission for both as-deposited and fluorinated HfO$_2$ gate dielectrics. Fig. 8 shows the energy band diagrams of carrier injection through TAT from the silicon substrate into the HfO$_2$ gate dielectric [Fig. 8(a) and (b)] and from the TaN metal gate into the HfO$_2$ gate dielectric [Fig. 8(c) and (d)]. As aforementioned, the fluorinated HfO$_2$ gate dielectric had deep trapping, resulting in lower gate leakage current than the as-deposited HfO$_2$ gate dielectric, due to shallow trap elimination.

In order to obtain the energy band diagram of the TaN/HfO$_2$/IL/Si structure with and without fluorine incorporation, we studied the tunneling current under gate and substrate injections by biasing the p- and n-type Si substrates to accumulation at 77 K. The current tunneling under gate and substrate injections can be observed for the MOS capacitors with p- and n-type Si substrates, respectively. In addition, at such a low temperature, the F–P conduction is suppressed, and the F–N tunneling current is dominant. In previous studies [23]–[31], the F–N tunneling is usually used for current transport analysis of high-k gate stacks. The F–N fitting can be used for the high-k gate insulator of a MOS capacitor, whereas the gate insulator is a dielectric bilayer [23]–[28] or ONO stacks [29]–[31]. As described in Fig. 2, there is an interfacial oxide layer between HfO$_2$ and Si. As a result, the F–N barrier parameters to be discussed in this paper are "effective" values with consideration of these ILs. Fig. 9(a) and (b) shows the leakage current of as-deposited and fluorinated HfO$_2$ with a TaN gate measured at 77 K under gate and substrate injections, respectively. Similar to the J–V characteristics at room temperature, both the leakage current and the breakdown voltage improved for the samples with fluorine incorporation. The characteristics improved with increasing fluorine implantation

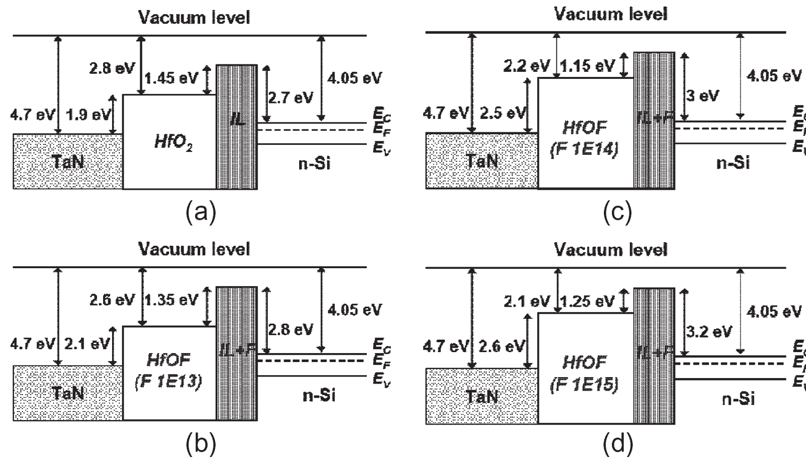

Fig. 11. Band diagrams of (a) as-deposited, (b) SSFI (F 1E13) HfO_2, (c) SSFI (F 1E14) HfO_2, and (d) SSFI (F 1E15) HfO_2, with a TaN gate extracted from leakage current at 77 K.

dosage, as illustrated in this figure. The inset of Fig. 10 shows the FN tunneling barrier heights fitted in the high-field region ($J = E^2 \exp[-4\sqrt{2m^*}(q\phi_B)^{3/2}/3q\hbar E]$), where the electron effective mass in HfO_2 was $0.1m_0$ (m_0 is the free electron mass) [19], and $\hbar$ is the Planck's constant. Φ_B is the effective barrier height that takes into account barrier height lowering and quantization of electrons at the semiconductor surface. The slope of the fitted line in the inset yields the following relationship: $B = -(8\pi(2qm^*)^{1/2}/3h)\phi_{\mathrm{eff}}^{3/2}$. In addition, the FN tunneling is quite different from F–P conduction and Schottky emission. There is no temperature parameter in this equation. What is measured is the gate current as a function of gate voltage. On the other hand, it should be noted that the FN tunneling current originating from gate injection is determined by the metal/HfO_2 barrier and is essentially not affected by the presence of the IL between HfO_2 and Si substrate. By the same token, the current originating from the substrate injection is determined by the IL/Si barrier. Thus, we can obtain both the TaN/HfO_2 and IL/Si barrier heights from the FN tunneling current under gate and substrate injections, respectively. Both the TaN/HfO_2 and IL/Si barrier heights were increased with the F-implant dosage (Fig. 10). As previously noted in this paper, the IL was Hf-silicate, not pure oxide. Therefore, the effective IL/Si barrier height was 2.7 eV, which is smaller than the SiO_2/Si barrier height (3.1 eV). However, the Hf-silicate with fluorine incorporation is increased, as shown in Fig. 10. It seems likely that F atoms incorporated into the HfO_2 layer are bonded to the Hf (or Si) dangling bond, resulting in annihilation of the oxygen vacancies, resulting in a greater barrier, as previously noted. The IL/Si barrier heights were also increased under substrate injection, owing to fluorine accumulating in the IL to passivate defect vacancies in the Si dangling bonds. On the other hand, the TaN/HfO_2 barrier height for the as-deposited sample is 1.9 eV, indicating that the conduction band of the HfO_2 film to the vacuum level is 2.8 eV, which is similar to previous research [19]. In addition, the effective TaN/HfO_2 and IL/Si barrier heights will decrease for the samples with PDA, as shown in this figure. The effective barrier was extracted from the FN equation, which was affected by J_{FN}. The J_{FN} will increase for the annealed samples due to HfO_2 film crystallization, as we previously mentioned. Therefore, the effective TaN/HfO_2 and IL/Si barrier heights will decrease for the annealed samples with consideration of HfO_2 film crystallization.

In summary, our results imply that the HfO_2 gate dielectrics with fluorine incorporation in CMOS applications would have lower leakage current due not only to the shallow trap elimination but also to the barrier increases. Fig. 11(a)–(d) shows the band diagrams of TaN/HfO_2/IL/Si, TaN/HfO_2/IL/Si (with F $1 \times 10^{13}/\mathrm{cm}^2$), TaN/$HfO_2$/IL/Si (with F $1 \times 10^{14}/\mathrm{cm}^2$), and TaN/$HfO_2$/IL/Si (with F $1 \times 10^{15}/\mathrm{cm}^2$) capacitors, respectively, at flat band, which serve to summarize the key results we have obtained from analysis of their F–N tunneling characteristics.

IV. Conclusion

The carrier transportation mechanism of fluorinated HfO_2 gate dielectrics was successfully investigated in this paper. First, the F–P conduction under gate and substrate injections for as-deposited and fluorinated HfO_2 gate dielectrics was analyzed. The effective F–P barriers increased with increasing fluorine implantation dosage, indicating that the fluorinated HfO_2 gate dielectrics have a deep trapping level, resulting in lower F–P current. Second, the F–N tunneling mechanism for fluorinated HfO_2 gate dielectrics was also studied by the J–V measurement at 77 K. The energy band diagram of the TaN/HfO_2/IL/Si capacitors with fluorine incorporation can be extracted from the good F–N fitting in this paper. Furthermore, the energy band diagram of the TaN/HfO_2/IL/Si capacitors was demonstrated by taking into account the IL, which is useful for understanding fluorinated HfO_2 in CMOS applications.

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