Improving the Retention and Endurance Characteristics of Charge-Trapping Memory by Using Double Quantum Barriers

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***Abstract*—We have studied the performance of double-quantum-barrier $[\mathrm{TaN}-\mathrm{Ir_3Si}]-[\mathrm{HfAlO}-\mathrm{LaAlO_3}]-\mathrm{Hf_{0.3}N_{0.2}O_{0.5}}-[\mathrm{HfAlO}-\mathrm{SiO_2}]$-Si charge-trapping memory devices. These devices display good characteristics in terms of their $\pm$9-V program/erase (P/E) voltage, 100-μs P/E speed, initial 3.2-V memory window, and ten-year extrapolated data retention window of 2.4 V at 150 °C. The retention decay rate is significantly better than single-barrier MONOS devices, as is the cycled retention data, due to the reduced interface trap generation.**

***Index Terms*—Erase, high-κ, nonvolatile memory, program.**

I. Introduction

METAL-OXIDE-Nitride-Oxide-Silicon (MONOS) devices [1]–[13] are attractive candidates for highly scaled sub-50-nm nonvolatile memories (NVMs). This is due to their discrete charge-trapping property, which can avoid stored charge leakage via a single oxide defect, when compared with conventional conductive poly-Si floating-gate memory devices. However, good data retention at high temperatures is difficult in MONOS memory—this is due to the shallower trap energy in Si_3N_4 [14] when compared with poly-Si floating-gate memory, which displays a 3.2-eV trap energy. To address this issue, we previously used deep trap-energy Al(Ga)N and HfON to replace the Si_3N_4 in MONOS devices [10]–[12], leading to improved retention when compared with Si_3N_4 [13]. Unfortunately, the 85 °C retention showed a charge decay (at 42%–46% of the initial memory window) that was relatively high and unacceptable. The high temperature retention can be improved via bandgap-engineered SONOS (BE-SONOS) [9], but the erase speed is low (10–100 ms) and the program/erase (P/E) voltages are high (18–20 V), contrary to the requirements of the ITRS scaling roadmap.

In this paper, we report a new double-quantum-barrier charge-trapping NVM device with good high temperature retention, low P/E voltages, and high speed. For instance, for a 9-V P/E voltage applied between the gate and Si channel at 100 μs, the extrapolated ten-year retention window was 2.4 V at 150 °C, where the initial value was 3.2 V. The observed retention P/E decay at this temperature was only 82/26 mV/decade (or 25% of the initial memory window), which is better than that of Ga(Al)N [10], [11] and HfON [12] MONOS devices. This is due to the double quantum barriers comprising the lower $[\mathrm{HfAlO}-\mathrm{SiO_2}]$ and the upper $[\mathrm{LaAlO_3}-\mathrm{HfAlO}]$, which confine the carriers trapped in the deep energy $\mathrm{Hf_{0.3}O_{0.5}N_{0.2}}$ quantum well. The high electric field across the $[\mathrm{HfAlO}-\mathrm{SiO_2}]$ tunnel oxide leads to the 100-μs P/E speed. For the double-barrier devices, we have found good 10^5 cycling and cycled retention characteristics, which arise from the rapid 100-μs P/E—this produces less stress to the tunnel oxide and, thus, less interfacial trap generation than in the single-barrier devices. By using $\pm$4.5- and $\mp$4.5-V P/E voltages applied between the gate and channel, these devices are promising candidates for embedded SoC applications using a 5-V voltage source [12].

II. Experimental Details

The $[\mathrm{TaN}-\mathrm{Ir_3Si}]-[\mathrm{HfAlO}-\mathrm{LaAlO_3}]-\mathrm{Hf_{0.3}N_{0.2}O_{0.5}}-[\mathrm{HfAlO}-\mathrm{SiO_2}]-\mathrm{Si}$ NVM device design involved choices of the oxide barrier height and its thickness. First, a 2.5-nm-thick thermal SiO_2 layer was grown on a standard p-Si substrate and a 2-nm layer of HfAlO was deposited by PVD to form the double tunneling layers. Then, a 10-nm $\mathrm{Hf_{0.3}N_{0.2}O_{0.5}}$ layer was deposited by reactive sputtering, under mixed O_2 and N_2 conditions [12], [15]. (The composition of N and O in the $\mathrm{Hf}_{1-x-y}\mathrm{N}_x\mathrm{O}_y$ was measured by X-ray photoelectron spectroscopy.) An 8-nm $LaAlO_3$ layer and then a 7-nm HfAlO were deposited to form the double blocking layers. Finally, a 15-nm Ir_3Si and a 150-nm TaN layer was added by PVD. The high work function Ir_3Si gate was used to make metal-gate/high-κ p-MOSFETs [16]. After standard processing, the MONOS devices were fabricated by using self-aligned As^+ ion implantation and given a 950 °C 30-s rapid thermal anneal activation to form the source–drain regions. For comparison, we also fabricated a $\mathrm{TaN}-\mathrm{HfLaON}-\mathrm{Hf_{0.3}N_{0.2}O_{0.5}}-\mathrm{SiO_2}-\mathrm{Si}$

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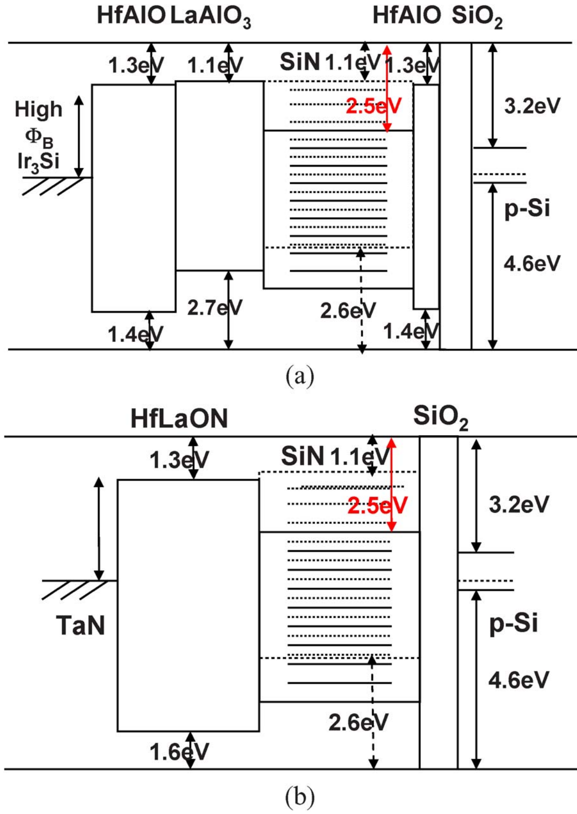

Fig. 1. Band diagrams of (a) [Metal-gate]-[High-κ barrier]-[Trapping Layer]-SiO_2-Si MONOS nonvolatile memory device and (b) [Metal-gate]-[High-κ top barrier 1-High-κ top barrier 2]-[Trapping Layer]-[High-κ bottom barrier 2-SiO_2]-Si double-quantum-barrier charge-trapping NVM. The conventional SiN trapping layer is shown in dotted lines.

single-barrier MONOS device. This device had a 2.9-nm-thick thermal SiO_2, a 9-nm $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layer, and a 15-nm HfLaON blocking oxy-nitride layer. Other procedures were the same as for the double-barrier device. The equivalent oxide thickness (EOT) of the $[\text{HfAlO} - \text{SiO}_2]$ tunnel oxide in the double-quantum-barrier device is 3.0 nm, which is close to the 2.9-nm SiO_2 tunnel oxide used in the single-barrier MONOS device. The EOT of the $[\text{HfAlO} - \text{SiO}_2]$ blocking oxide in the double-barrier device is 3.0 nm—the same as the single-barrier HfLaON MONOS device. Hence, the EOTs of both the top blocking oxide and bottom tunnel oxide are almost the same for both the double- and single-barrier charge-trapping memory. The memory devices were characterized by different P/E tests, retention experiments, and cycling endurance at 25 °C, 85 °C, and 125 °C.

III. Results and Discussion

A. Band Diagram and P/E Characteristics

In Fig. 1(a) and (b), we compare the schematic band diagrams of the single- and double-quantum-barrier devices, respectively. The conventional SiN trapping layer has a small conduction band discontinuity (ΔE_C) with respect to the barrier oxide of only 1.1 eV [14], where the stored charges in shallow trap energy levels can leak out at elevated temperatures. The other ΔE_C and valence band discontinuity (ΔE_V) values

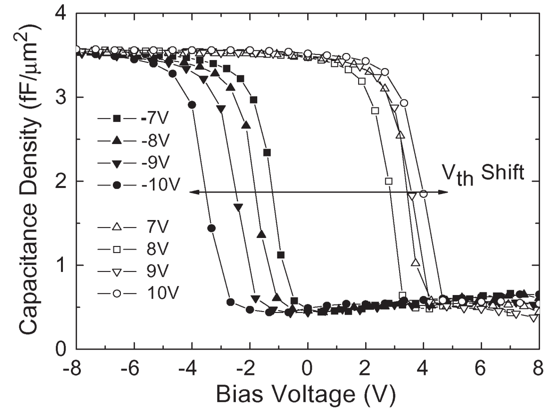

Fig. 2. C–V hysteresis for double-quantum-barrier device showing a large V_{th} shift.

are from published literature [16]–[18]. Thus, the SiN MONOS devices are expected to have poor retention properties. The retention in charge-trapping memory can be improved by increasing ΔE_C with respect to the barrier oxide, for instance, by using Al(Ga)N and HfON when compared with SiN [10]–[12]. The use of $Hf_{0.3}N_{0.2}O_{0.5}$ gives a deeper ΔE_C of 2.5 eV [16] compared with SiN [14], Al(Ga)N [10], [11], and our previously reported HfNO with N–10% [12]. However, the trapped carriers can still escape via sequential Schottky emission and tunneling at higher temperatures in the 85 °C–150 °C range. For NVM devices, good 85 °C–150 °C retention is required because of the increasing chip temperatures arising from the higher power dissipation and larger density of future ICs. As a result, the double-quantum-barrier structure is useful to improve the trapped carrier confinement within the $Hf_{0.3}N_{0.2}O_{0.5}$ quantum well, with its deep trapping energy.

Fig. 2 shows the C–V hysteresis characteristics of the double-quantum-barrier charge-trapping device with its $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layer. The hysteresis window increases with increasing voltage, indicating good charge storage. A large hysteresis window of 7.3 V was measured under swept voltages of ± 10 V in this device, which suggests a high trap density and/or deep trap energy in the $Hf_{0.3}N_{0.2}O_{0.5}$ [10]–[12].

In Fig. 3(a) and (b), the P/E characteristics are displayed for various gate voltages, for single- and double-quantum-barrier devices, respectively. The devices had the same $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layer and almost the same EOT for the barrier oxides. The threshold voltage change (ΔV_{th}) increases with increasing P/E voltage and time due to the increased number of trapped charges. For the single-quantum-barrier MONOS device, a memory window of 2.8 V was obtained at ± 9 V and at 100-μs P/E. For comparison, the double-quantum-barrier charge-trapping device showed a larger ΔV_{th} memory window of 3.2 V for the same testing conditions. It is noticed that the ΔV_{th} for both program and erase are improved compared with that of the single-barrier device. The combined $[\text{HfAlO} - \text{SiO}_2]$ tunnel oxide, with its EOT close to that for the single-barrier MONOS device, gives a lower energy barrier for electrons to tunnel through and leads to a larger memory window. The better erase characteristics are due to the higher work function of Ir_3Si gate electrode than that of TaN in single-barrier device.

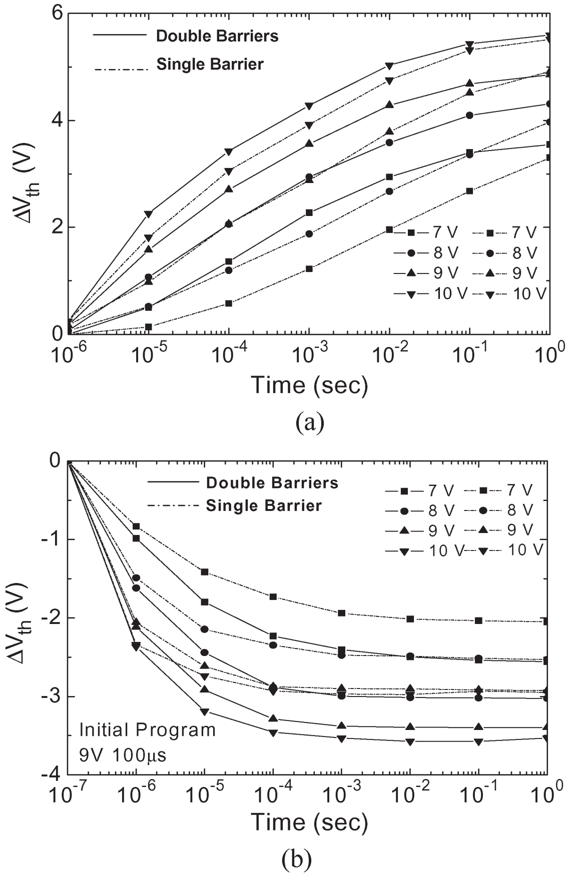

Fig. 3. Comparison of (a) program and (b) erase characteristics between single- and double-quantum-barrier devices under different voltages and times. For the erase, both devices were initially programmed at 9 V for 100 μs.

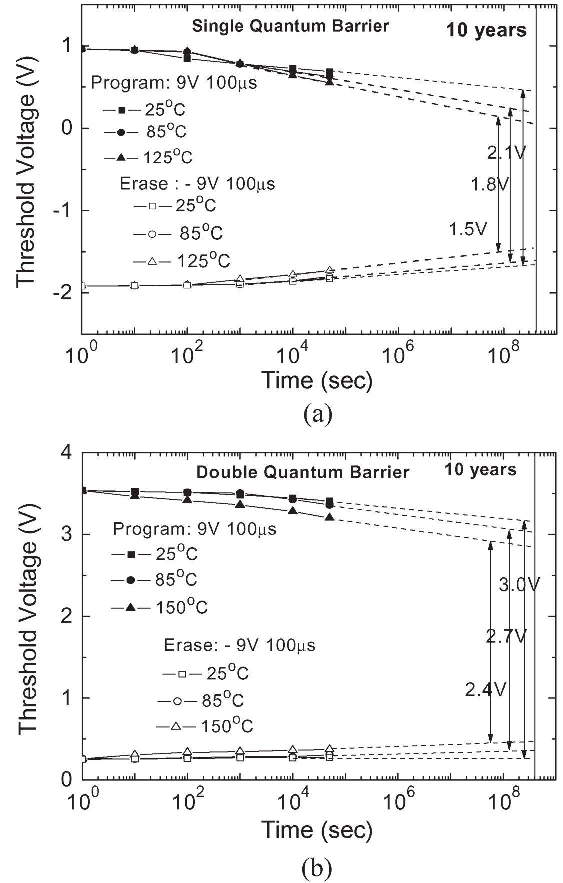

Fig. 4. Device retention characteristics of (a) single- and (b) double-quantum-barrier charge-trapping devices at different temperatures.

In both cases, the low P/E voltage arises from the small voltage drop and electric field (E) in the high-κ barriers and the high-κ $\mathrm{Hf}_{0.3}\mathrm{N}_{0.2}\mathrm{O}_{0.5}(\kappa = 22)$ trapping well. This also gives a high E in the tunnel oxide to produce the high P/E speed using tunneling mechanism. Because an inverter circuit can be used to generate the opposite polarities of ± 4.5 and ∓ 4.5 V applied between the gate and channel [12], this low P/E voltage is important for embedded SoC applications using a 5-V voltage source.

B. Retention and Endurance

Good data retention is a challenge for MONOS charge-trapping memory. Fig. 4(a) shows the retention characteristics of the single-quantum-barrier MONOS device. The initial ΔV_{th} was 2.8 V under 100 μs and $\pm$9-V P/E, and the extrapolated ten-year memory windows were 2.1, 1.8, and 1.5 V at 25 °C, 85 °C, and 125 °C, respectively. The decay rates at 85 °C and 125 °C were 92 and 110 mV/dec for the high state or 36 and 55 mV/dec for the low state. For comparison, in Fig. 4(b), we show the retention data of a double-quantum-barrier charge-trapping device at 25 °C, 85 °C, and 150 °C. The initial ΔV_{th} was 3.2 V under 100 μs and $\pm$9-V P/E, and the extrapolated ten-year memory windows were 3.0, 2.7, and 2.4 V under 25 °C, 85 °C, and 150 °C, respectively. The retention P/E decay rates at 85 °C and 150 °C were only 62 and 82 mV/dec for the high state and 15 and 26 mV/dec for the low state (16% and 25% of initial memory window). This improvement in the high temperature data retentions, compared with a single-barrier MONOS device, indicates the advantage of using double quantum barriers to confine the trapped charges. Because the EOT is close for both single- and double-barrier devices, using physically thicker high-κ tunnel layers can improve retention in double-barrier devices. Using double blocking layer may also improve the retention due to the slightly higher ΔE_C and misaligned trap energies similar to the ONO blocking oxide case. The read disturbance may be a concern in this low voltage operated device to cause charge loss. A similar low voltage P/E at 10 V/$-$9 V was also reported, where the stored charges were not largely lost as evident from the small V_{th} change even after 1000 s of gate stresses [19].

Endurance is another important factor for NVM. In Fig. 5(a), we compare endurance data for single- and double-barrier charge-trapping devices. Windows of 2.4 and 2.9 V (after 10^5 cycles) were obtained for the single- and double-barrier devices, respectively. This arises from the rapid 100-μs P/E at 9 V, which causes reduced electric field stress to the tunnel oxide. The degradation after 10^5 cycles is better for the double-barrier device than that for the single-barrier device, with ΔV_{th} degradations of 0.3 and 0.4 V or 9% and 14%, respectively. The effect of long-term cycling on the retention appears in Fig. 5(b), where the 10^3-cycle ten-year retention windows of

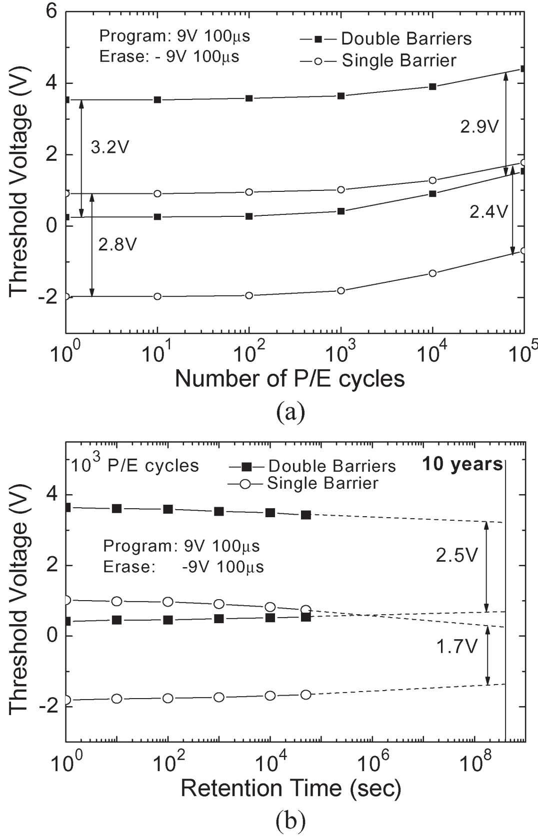

Fig. 5. Comparison of (a) endurance and (b) retention characteristics after 10^3 P/E cycling of single- and double-quantum-barrier devices.

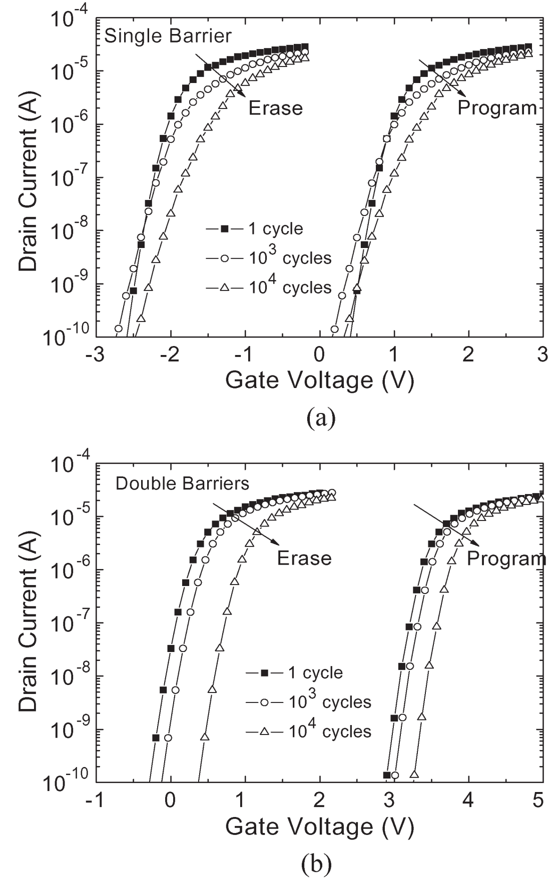

Fig. 6. I_d–V_g characteristics of (a) single- and (b) double-quantum-barrier devices after cycling.

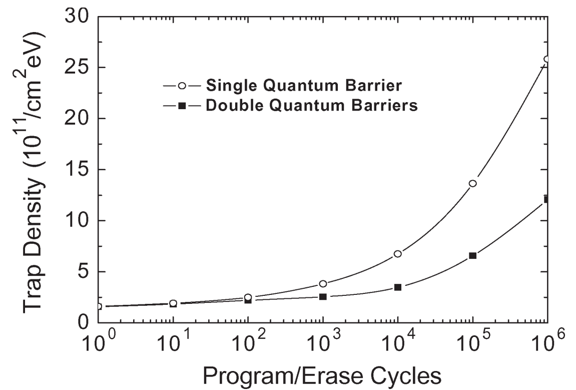

Fig. 7. Comparison of the interface trap densities $(D_{\rm it})$ for single- and double-barrier devices after P/E cycling.

1.7 and 2.5 V are shown for the single- and double-quantum-barrier devices, which were initially 2.8 and 3.2 V, respectively.

To understand such improvement, we also measured the I_d–V_g characteristics of the devices before and after cycling. As shown in Fig. 6, the single-barrier MONOS device shows an increase of subthreshold swing (SS) with increasing cycling stress, which suggests the generation of $\mathrm{SiO_2/Si}$ interface traps. In contrast, the double-barrier device shows the same SS after cycling. Besides the SS change, a shift of I_d–V_g curves was also found for both devices after cycling. The cycling-induced linear I_d–V_g shift or $\Delta V_{\rm th}$ in Fig. 5(a) is also slightly larger for single-barrier devices than the double-barrier ones, indicating a slightly larger amount of oxide charge generation. The generation of $\mathrm{SiO_2/Si}$ interface traps in the single-barrier MONOS device from degraded SS also explains the relative poor retention after cycling, as shown in Fig. 5(b), because the trapped carriers may tunnel out via these low energy interface traps within the Si bandgap.

We examined the interface trap generation by charge pumping methods [20]. Fig. 7 shows the interface trap density $(D_{\rm it})$ of single- and double-quantum-barrier devices after P/E cycling. The initial $D_{\rm it}$ is nearly the same for both devices. However, under extensive P/E cycling, more interface traps are created for the single- than for the double-barrier device. This improved $D_{\rm it}$ generation in the double-barrier device leads to better retention after cycling, which is a key factor for achieving good device integrity for NVM.

IV. Conclusion

At 150 °C under a fast 100-μs and low ±9-V P/E voltage, we show that a double-quantum-barrier $[\mathrm{TaN-Ir_3Si}]-\mathrm{HfAlO}-\mathrm{LaAlO_3}-\mathrm{Hf_{0.3}O_{0.5}N_{0.2}}-\mathrm{HfAlO}-\mathrm{SiO_2}-\mathrm{Si}$ charge-trapping device has good NVM integrity in terms of a 3.2-V initial $\Delta V_{\rm th}$ and 2.4-V ten-year extrapolated retention. Compared with its single-quantum-barrier MONOS counterpart, the double-quantum-barrier device showed significantly better high temperature retention and cycled retention data, due to better

carrier confinement and lower interface trap generation after the P/E cycling.

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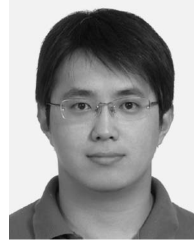

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