Journal of ELECTRONIC MATERIALS, Vol. 37, No. 7, 2008
DOI: 10.1007/s11664-008-0463-y

Regular Issue Paper

Effect of Migration and Condensation of Pre-existing Voids on Increase in Bump Resistance of Flip Chips on Flexible Substrates during Electromigration

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In Pb-free solder joints formed by reflowing a bump of solder paste, voids are formed within the solder due to the residue of flux in the reflow process. These voids migrate toward the cathode contact during electromigration under current stressing. Accompanying the electromigration, resistance jumps of a few 100 mΩ were observed. It was postulated that a jump occurs when a void touches the cathode contact. This study investigated the effect of the void migration and condensation on the change in bump resistance using three-dimensional (3D) simulations and finite element analysis. It was found that there was negligible change in bump resistance during void migration towards the high-current-density region before touching the cathode contact opening. When a small void condensed on the contact opening and depleted 18.4% of the area, the bump resistance increased only 0.4 mΩ. Even when a large void depleted 81.6% of the opening, the increase in bump resistance was 3.3 mΩ. These values are approximately two orders of magnitude smaller than those reported in the literature for the change in resistance due to void migration in flip chips on flexible substrates. We conclude that the reported change in resistance was most likely that of the Al or Cu interconnection in the flip-chip samples.

Key words: Electromigration, flip-chip solder joints, packaging

INTRODUCTION

Electromigration in flip-chip solder joints has become an important reliability issue due to the current requirement of high density and high performance in electronic devices,[1,2] and it has been studied extensively in recent years.[3–7] The current-crowding-induced void formation and propagation on the cathode/chip side was proposed to be responsible for the failure of flip-chip solder joints.[2,4,5] For Al and Cu interconnects, electromigration-induced void nucleation and propagation have been monitored by the change in resistance.[8–10] In addition, the Kelvin structure, in which four electrical terminals are employed to measure the contact resistance, has been utilized to measure the via or contact resistance in Al and Cu interconnects for over 20 years.[11–13] In most previous electromigration studies of flip-chip solder joints, daisy-chain structures were utilized to monitor the change in resistance. Nevertheless, the resistance of a solder bump was estimated to be on the order of a few milliohms, whereas the resistance of the metallization trace ranges from several hundred to several thousand milliohms, depending on its dimensions. Thus, the bump resistance is quite small compared with the resistance of the metallization traces,[14] and the daisy-chain structure cannot detect the slight changes in resistance due to void formation in the solder

(Received August 24, 2007; accepted March 31, 2008; published online May 1, 2008)

joint. Kelvin probes have recently been implemented in flip-chip solder joints for electromigration study.[15] The effect of void nucleation and propagation on the change in bump resistance has been reported.[15,16] The change ranges from sub-milliohm to tens of milliohms, depending on the size of the void.

During the fabrication process of flip-chip Pb-free solder joints, large voids are left in the solder bump due to the residue of flux burnt during reflow. The voids tend to migrate to the chip/cathode contact opening during current stressing.[17] Nah et al. reported that void migration and condensation on under-bump metallization (UBM) opening might cause a resistance jump of 0.2 Ω to 0.5 Ω.[18] However, the change in resistance is too large to come from the solder bumps. To clarify the effect of void migration and depletion of contact opening on bump resistance, we employed a three-dimensional (3D) simulation to investigate the changes in bump resistance due to void migration in a solder bump at various positions. Results of this study contribute to a better understanding of the changes in bump resistance due to void migration in flip-chip solder joints.

SIMULATION

Figure 1a shows a schematic diagram of the flip-chip bumps used in this study. The Al trace on the chip side was 1.5 μm thick and 100 μm wide. The UBM was 5-μm Cu electroplated on Ti/Cu layers. Eutectic SnPb solder was adopted with passivation with UBM openings of 85 μm and 110 μm in diameter, respectively. The pad metallization on the substrate was comprised of 1-μm Au and 5-μm electroless Ni layers. The diameter of the pad opening was 130 μm. Cu lines were 30 μm thick and 100 μm wide. The bump height was approximately 75 μm. The electroplated Cu on the chip side reacted with the solder to form Cu_6Sn_5 intermetallic compounds (IMCs), with an average thickness of 1.4 μm. Ni_3Sn_4 IMCs were formed on the substrate side in the interface of the electroless Ni and the solder, and the average thickness of the IMCs was 1 μm.

Figure 1b shows the path of migration for a void in the solder. It is assumed that the void is formed in the middle of the solder bump after fabrication, then it propagated toward the UBM opening during electromigration but did not deplete the UBM opening. Finally, it condensed on the UBM opening, and depleted the UBM opening. The void changed shape and became pancake-type when it condensed on the UBM opening, and the volume of the pancake-type void was kept the same as that of the original spherical void. In this study, four paths of void migration were simulated, and their effect on the changes of the bump resistance will be discussed.

Figure 1c shows the 3D simulation model with the mesh used in this study. Since the Ti layer was quite thin compared with the bump height, it was ignored in the simulation model to avoid meshing problems. In addition, we assumed both Cu_6Sn_5 and

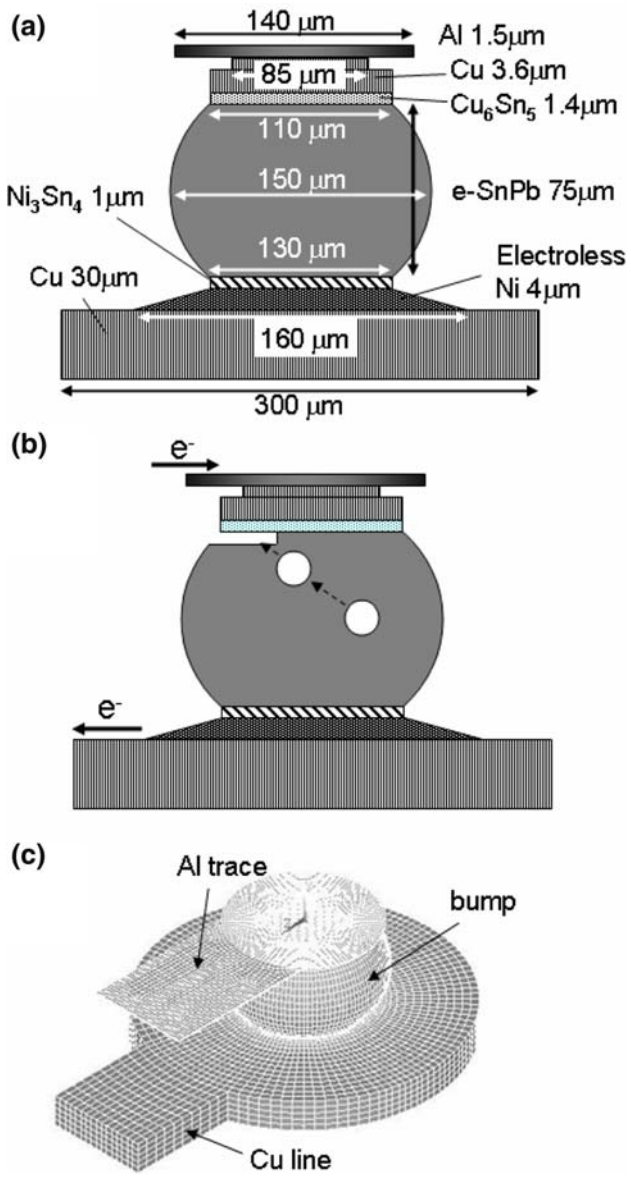

Fig. 1. (a) Cross-sectional schematic drawing for solder joints used in the simulation model. (b) Migration path of a pre-existing void during electromigration. (c) Mesh used in the simulation model.

Ni_3Sn_4 IMCs to be of layered type. The resistivity of the materials used in this simulation are listed in Table I. Ansys simulation software was employed to perform the simulation, and the model used SOLID69 eight-node hexahedral coupled field elements. The dimension of the mesh was 3.8 μm. A current of 0.2 A was applied during the modeling to obtain the bump resistance.

RESULTS AND DISCUSSION

The increase in bump resistance was less than 1 mΩ when a small void condensed on the passivation opening. Figure 2 shows the current density distribution in the solder joint without a pre-existing void. The electron flow entered from the upper-left corner

Table I. Properties of the Materials Used in the Simulation Models

Materials	Al	Cu	IMC Cu_6Sn_5	e-SnPb	IMC Ni_3Sn_4	Electroless Ni
Resistivity ($\mu\Omega$ cm at 20°C)	3.2	1.7	17.5	14.6	28.5	70

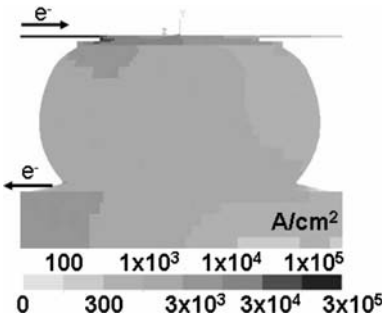

Fig. 2. Cross-sectional current-density distribution in solder joints without voids.

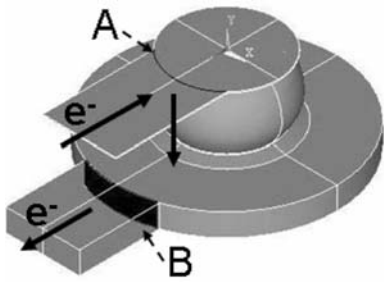

Fig. 3. Schematic drawing of the current path in the simulation model. The bump resistance was defined as the difference in voltage between position A (Al pad) and position B (Cu pad) divided by the applied current.

of the bump and exited from the lower-left Cu line. Current crowding occurred at the entrance point of the Al trace. Bump resistance is defined as follows and is shown in Fig. 3. First, the electrical potential of cross section A was measured by averaging the node potential in the area, which was the junction of the Al trace and the Al pad above the solder bump. The junction was 110 μm long and 1.5 μm thick. Moreover, the potential of cross section B was obtained in a similar way by averaging the value in a 110 μm $\times$ 30 μm Cu line. The bump resistance was obtained by dividing the voltage drop by the applied current; it was 7.7 mΩ for the bump without pre-existing voids. When a void formed inside the solder bump, the current distribution did not change much, as is illustrated in Fig. 4a. The void of 21.9 μm diameter was assumed to be located in the low-current-density region. The bump resistance was measured to be 7.7 mΩ, which was the same as that for the bump without pre-existing voids. This stage is referred to as stage I in this paper. During electromigration, atoms in the solder bump will be driven to the anode due to the high current density, and a corresponding vacancy flux goes to the cathode interface.[17] Therefore, the void migrates toward the UBM opening,[18] as shown in Fig. 4b. This stage is denoted as stage II. The current redistributes when the voids propagate to a distance of about 5 μm from the UBM opening. The current bypasses the void, and the current distribution becomes slightly more uniform than that in stage I. The bump resistance decreased only slightly to 7.6 mΩ. In stage III, the void condensed on the UBM opening and changed its shape from a sphere to a pancake, which occupied 18.4% of the UBM opening. The pancake void was assumed to be 1 μm thick. Since the void is an insulator, the current drifted further ahead in the Al pad, and then drifted down to the solder bump. The current density redistribution is clearly shown in Fig. 4c. The current-crowding region was relocated closer to the center of the UBM opening. The measured bump resistance increased to 8.1 mΩ, since electrons drifted longer in the Al pad, which was a high-resistance path.

The size of the pre-existing void could be larger, and thus exerted a larger effect on bump resistance. It was assumed that a large void of 35.9 μm diameter was formed in the same location, as shown in Fig. 5a. With this large void, the bump resistance remained the same at 7.7 mΩ. As the void moved toward the UBM opening, at a distance of 5 μm, shown in Fig. 5b, the current path inside the solder joint was affected slightly, yet the bump resistance did not change. When the large void condensed to become a pancake void 1 μm thick, it depleted 81.6% of the UBM opening, as illustrated in Fig. 5c. The current passed by the void and entered the solder at the right-hand side of the bump. Owing to the longer electrical path, the bump resistance increased to 11 mΩ. Table II lists the changes in bump resistances for void migration and condensation in the three models.

The increase in resistance due to the extra path of current flow can be calculated as follows. Figure 6 shows a schematic drawing for an Al trace $2W$ wide and t thick near a solder joint. The dashed circle represents the passivation opening to the solder bump, where electrons enter the solder bump. The increase in resistance dR due to the extra current path in the X-direction dx in the Al pad can be expressed as

$$\mathrm{d}R = \rho_{\mathrm{Al}} \frac{\mathrm{d}x}{2Wt} \tag{1}$$

The term dx can be written as

$$\mathrm{d}x = -\mathrm{d}(R_1 \cos\theta) = (R_1 \sin\theta)\mathrm{d}\theta, \tag{2}$$

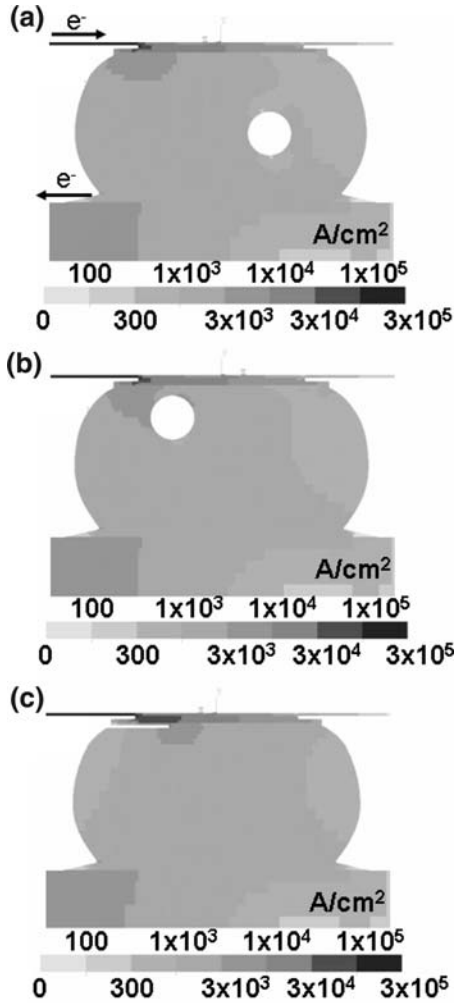

Fig. 4. Cross-sectional view of the current-density distribution in a solder bump with: (a) a pre-existing spherical void of diameter 21.9 μm in the middle of the bump, (b) a pre-existing spherical void of diameter 21.9 μm near the UBM opening, and (c) a pancake void occupying 18.4% of the UBM opening.

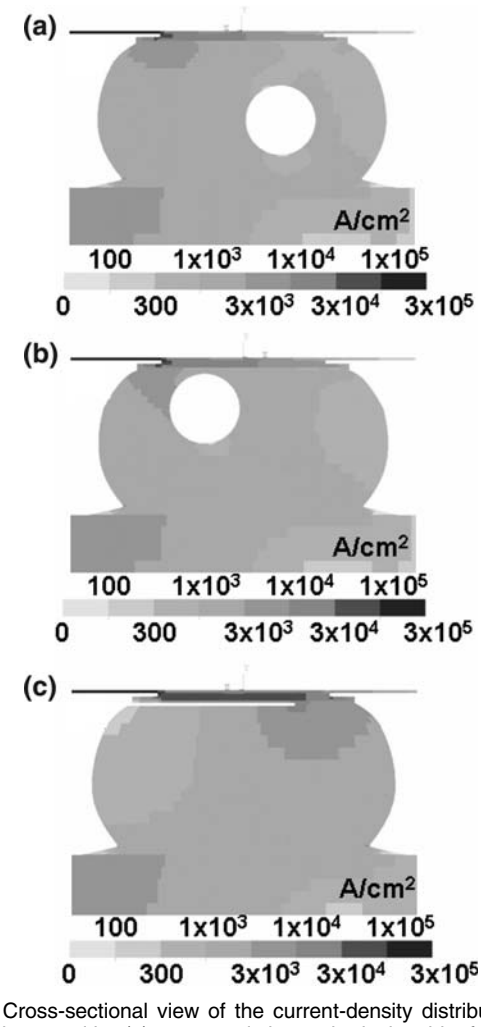

Fig. 5. Cross-sectional view of the current-density distribution in a solder bump with: (a) a pre-existing spherical void of diameter 35.9 μm in the middle of the bump, (b) a pre-existing spherical void of diameter 35.9 μm near the UBM opening, and (c) a pancake void occupying 81.6% of the UBM opening.

and W can be expressed as

$$W = R_1 \sin\theta. \tag{3}$$

Thus, the increase in resistance for the Al pad (the shaded region in Fig. 6) above the solder bump can be obtained as follows

$$R_{\text{total}} = \int_{\theta_1}^{\theta_2} \rho_{\text{Al}} \frac{(R\sin\theta)\mathrm{d}\theta}{2t \cdot R\sin\theta} = \frac{\rho_{\text{Al}}}{2t}\Big|_{\theta_1}^{\theta_2} = \frac{\rho_{\text{Al}}}{2t}(\theta_2 - \theta_1), \tag{4}$$

where

$$\theta_1 = \sin^{-1}\left(\frac{W}{R_1}\right), \tag{5}$$

$$\theta_2 = \cos^{-1}\left(-\frac{R_2}{R_1}\right). \tag{6}$$

It can be seen that the resistance of the Al pad varies with the resistivity and the thickness of the

Table II. Bump Resistances Estimated in Three Stages for Three Approaches

Void Size	Small			Large		
Stage	I	II	III	I	II	III
Bump resistance (mΩ)	7.7	7.6	8.1	7.7	7.7	11.0

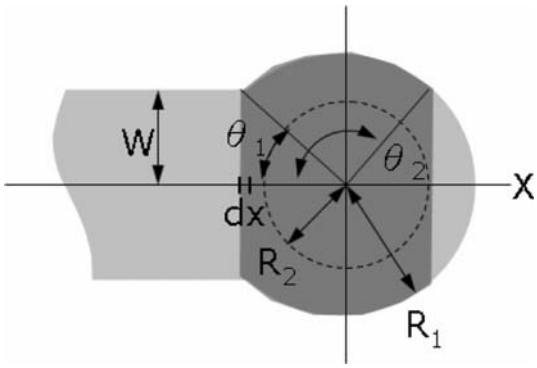

Fig. 6. Schematic drawing for an Al trace 2*W* wide. R_1 represents the Al pad opening, and R_2 denotes the passivation opening.

Al pad. Table III summarizes the resistance for various layers of UBM structures with R_1 = 70 μm, R_2 = 42.5 μm, and W = 50 μm, assuming that the current passes through the entire structure laterally. In general, the void forms at the interface between the IMC and the solder. Therefore, we need to include the IMC layer when calculating the increase in resistance due to void formation. The IMC layer also conducts current in parallel once the void forms. With a thicker Cu UBM, the increase in resistance due to void formation appears to be as low as 2 mΩ. However, with a thin-film UBM of Al/Ni(V)/Cu and a 0.5-μm-thick Al trace, the increase in resistance due to void condensation may be around 15 mΩ.

Therefore, void migration inside the solder bump had an almost negligible effect on the bump resistance. Moreover, as the void condensed on the UBM opening, the bump resistance increased only a few milliohms when the opening was depleted by 81.6%. The increase in the bump resistance was mainly because electrons needed to drift farther in the Al trace, as shown in Fig. 5c. Since the cross-section of the Al trace was very small, the resistance of the Al trace was much larger than that of the solder bump. For an Al trace 100 μm wide, 100 μm long, and 1.5 μm thick, which are typical dimensions for the Al pad above the solder bump, the resistance was calculated to be 15 mΩ. We also simulated other cases, such as the position of the pre-existing void and depletion of the UBM opening in the low-current-density region. The bump resistance remained the same regardless of the position of pre-existing voids. In addition, voids condensed in the low-current-density region (upper-right corner) had less influence on the bump resistance than those condensed in the high-current-density region. Unless a large void condenses on the UBM opening and depletes it completely, the increase in bump resistance remains insignificant.

The above results imply that the resistance jump reported by Nah et al.[18] cannot be attributed to void migration and condensation. They found that the resistance increased stepwise on the order of several 100 mΩ when they monitored the total resistance of a daisy-chain structure. The initial resistance for the structure was as large as 2 Ω, which included the bump resistance of 32 joints, the line resistance of the Al trace, the line resistance of the Cu trace on their flexible substrate, contact resistance, and the additional wiring for current stressing. Although there were 32 bumps in the daisy chain, only a few of the UBM openings were severely depleted. It is estimated that the total increase in resistance due to void condensation on UBM opening was only tens of milliohms. Therefore, the changes in resistance might mainly be due to degradation of the rest of the circuit rather than void migration and condensation.

To investigate the reason behind the stepwise increases in resistance, *in situ* voltage measurements were carried out by four-point probes. The resistance jumps were still observed. Thus, the contact resistance could be excluded. We speculate that the stepwise increase in resistance is due to the line resistance of the Al trace on the chip side and of the Cu wire on the flexible substrate side.

It is noteworthy that the effect of the temperature coefficient of resistivity (TCR) may contribute to the increase in resistance. However, according to our previous results,[19] even when the voids deplete 80% of the contact opening, there is no obvious Joule heating. Therefore, in the above two models, the condensation of voids does not contribute to significant Joule heating and increase in resistance. On the other hand, if the wiring traces are damaged, Joule heating may be significant.[20] Then the TCR

Table III. Resistance for Various Layers of UBM Structures with R_1 = 70 μm, R_2 = 42.5 μm, and W = 50 μm

	Thickness, t (μm)	Resistivity, ρ ($\mu\Omega$ cm)	Resistance, R (mΩ)
Al trace and pad	1.5	3.2	15.2
Cu UBM	5.0	1.7	2.4
Ni UBM	2.6	6.8	18.7
Al/Ni(V)/Cu UBM	0.7	29.4	299.8
Ni_3Sn_4 IMC	1.4	28.5	145.3
Cu_6Sn_5 IMC	1.4	17.6	89.7

The intermetallic compound layer was also considered.

effect may contribute to the increase in resistance significantly. This is because the major source of Joule heating is the wiring traces. The bump resistance appears quite small compared with that of the wiring traces.

When the pancake-type void forms on the contact opening, it may affect the stress in the Al trace and may etch or corrode the Al trace due to the residue flux gas in the void, thus increasing the resistance. On the other hand, the same stepwise increase in resistance should also occur in electromigration studies of Pb-free flip-chip joints (containing pre-existing voids) on rigid substrates having Al trace on the chip side. For the Cu wiring on the flexible substrate, because the flexible substrates are made of polyimide and the Cu leads on it were electroplated on a sputtered Cu seed layer, the adhesion between the Cu leads and the polyimide layer may not be good enough. Furthermore, the flexible substrate is a free-standing film with a worse ability on heat dissipation than a rigid substrate. Joule heating effects may be more serious in the structure, causing the degradation of Cu leads and thus contributing to the resistance jumps during electromigration testing of flip-chip solder joints. Further study will be needed to clarify these speculations.

CONCLUSIONS

The effect of migration and condensation of pre-existing voids on bump resistance has been investigated by 3D simulation. The simulation results show that the bump resistance increased only a few milliohms during electromigration when the void condensed on the UBM opening and depleted some of the opening. The bump resistance increased only a few milliohms because the void blocked the original current path, and the current needed to drift further in the thin Al pad. Thus the increase is too small to be responsible for the observed increase of a few 100 mΩ. We speculate that the change is more likely due to the change in resistance in the Al and Cu interconnections in the daisy-chain circuit.

ACKNOWLEDGEMENTS

The authors would like to thank the National Science Council of Taiwan of the Republic of China for the financial support under Grant No. NSC 95-2218-E-009-022. In addition, the assistance from the simulation facility of the National Center for High-Performance Computing (NCHC) in Taiwan is greatly appreciated.

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