A Novel Multiple-Gate Polycrystalline Silicon Nanowire Transistor Featuring an Inverse-T Gate

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***Abstract*—A novel multiple-gate field-effect transistor with poly-Si nanowire (NW) channels is proposed and fabricated using a simple process flow. In the proposed structure, poly-Si NW channels are formed with sidewall spacer etching technique, and are surrounded by an inverse-T gate and a top gate. When the two gates are connected together to drive the NW channels, dramatic performance enhancement as compared with the cases of single-gate operation is observed. Moreover, subthreshold swing as low as 103 mV/dec at Vd = 2 V is recorded. Function of using the top gate bias to modulate the threshold voltage of device operation driven by the inverse-T gate biases is also investigated in this letter.**

***Index Terms*—Field-effect transistor, multiple gate (MG), nanowire (NW), poly-Si.**

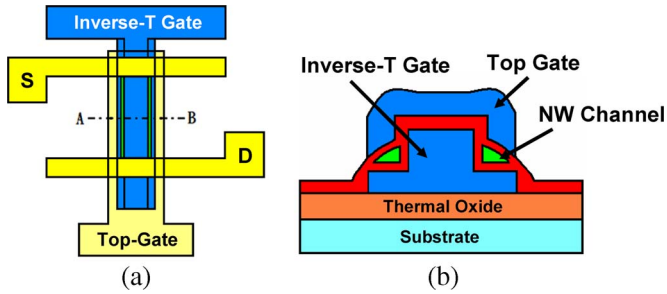

Fig. 1. (a) Top and (b) cross-sectional views of the proposed MG FET device with poly-Si NW channels surrounded by an inverse-T gate and a top gate.

RECENTLY, we proposed a new field-effect transistor structure which utilizes poly-Si nanowire (NW) as the channels [1], [2]. Fabrication of such device is very simple and requires no advanced lithography tools to generate the nanoscale patterns. Nevertheless, the fine-grain structure of poly-Si NW is considered to affect the carrier transport and device performance. Several ways are possible to relax such concern. One of that is to enhance the film crystallinity by implementing available schemes such as metal-induced lateral crystallization in the fabrication [3]. An alternative strategy is the adoption of multiple-gated (MG) configuration to increase the gate controllability over the channel. This has been widely demonstrated in the literature for devices with double-gate (DG) [4] and triple-gate [5], as well as surrounding-gate schemes [6]. Since poly-Si NWs are with a tiny volume and, thus, a limited amount of defects are contained, MG configuration is also expected to significantly improve the performance of poly-Si NW devices performance. The MG configuration may consist of several separate gates and each gate can be biased independently. Such design allows more freedoms for device operation [7].

In this letter, a new MG structure which consists of an inverse-T-gate and a top-gate employed to surround the poly-Si NW channels is proposed. Top and cross-sectional views of the structure are shown in Fig. 1. From the figure, it can be understood that the poly-Si NW channels are almost fully surrounded by an inverse-T gate and a top gate. Moreover, the two gates can be biased independently to operate the device.

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Schematic flow of the fabrication process for the proposed device is shown in Fig. 2. First, silicon wafers were capped with a 100-nm-thick wet oxide. After depositing a 150-nm-thick *in situ*-doped n^+ poly-Si, the inverse-T gate was fabricated by twice standard G-line lithography and dry etching steps [Fig. 2(a) and (b)]. This was followed by the deposition of a 20-nm-thick low-pressure chemical vapor deposition (LPCVD) oxide layer serving as the dielectric of inverse-T gate. A 100-nm-thick amorphous-Si layer was then deposited by LPCVD system. Next, an annealing step was performed at 600 °C in N_2 ambient for 24 h to transform the amorphous-Si into poly-Si. Subsequently, source/drain (S/D) implantation was performed [Fig. 2(d)]. After S/D photoresist patterns were formed, a reactive plasma etching step was employed to form the NW channels simultaneously with S/D definition. Note that the height of upper step (h_1) of the inverse-T gate was designed to be higher than the lower one (h_2), so, in the process, we could control the etching time to make only two NW channels remained on the upper step corners of the inverse-T gate [Fig. 2(e)]. Another LPCVD TEOS oxide layer with thickness of 20 nm was deposited to serve as top gate oxide. Then, a 100-nm-thick *in situ* doped n^+ poly-Si was deposited and patterned to serve as the top gate electrode [Fig. 2(f)]. All devices were then covered with 200-nm-thick oxide passivation layer. The fabrication was completed after the formation of test pads using standard metallization steps. All fabricated devices received a NH_3 plasma treatment at 300 °C for 3 h before characterization.

The cross-sectional transmission electron microscopic (TEM) image of a fabricated device showing the NW channel and the gates is shown in Fig. 3. In the figure, an enlarged view of the NW is also shown and three corners, denoted as A, B, and C, are specified. Corner A is the one that directly faces the reentrant of the inverse-T gate. Owing to the nature of poly-Si etching, the corner is rounded and has an angle larger than 90°.

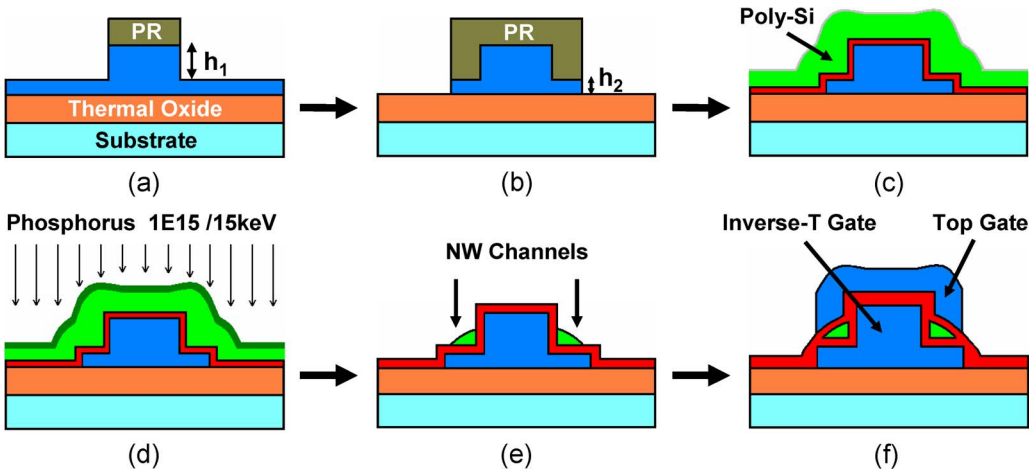

Fig. 2. Schematic process flow of the proposed MG FET device.

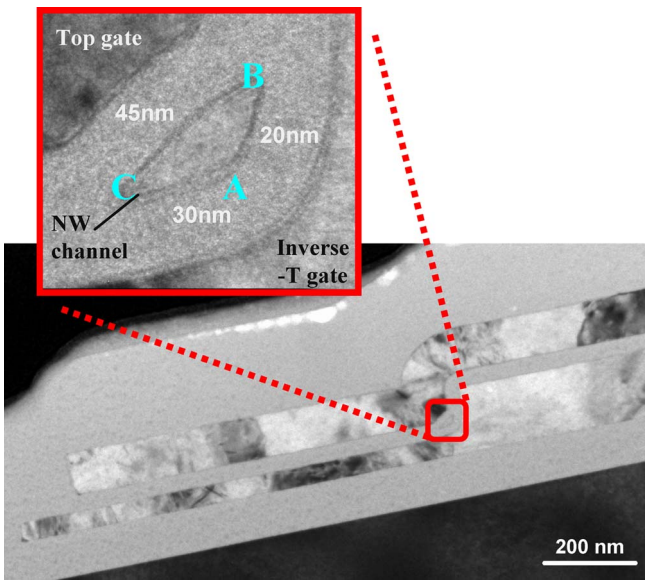

Fig. 3. Cross-sectional TEM picture of a fabricated device.

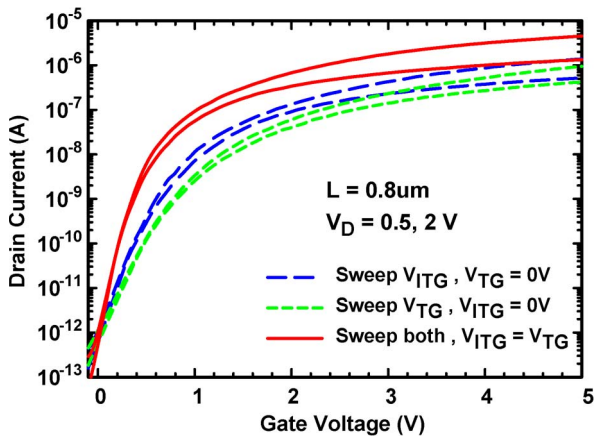

Fig. 4. Transfer characteristics of a fabricated device under SG and DG operations.

This will help relax the corner effect [8] and improve gate oxide reliability. Although the other two corners (B and C) are sharp, they are unlikely to cause any negative effect as they are sandwiched between the two gates. Note that the largest width of NW channel is smaller than 20 nm.

Fig. 4 shows and compares transfer characteristics of a device for operations in either single-gate (SG) or DG modes. In SG modes, varying bias was applied to one of inverse-T gate and top gate electrodes with the other one grounded, whereas in DG mode, both the inverse-T gate and top gate electrodes are connected together during the operation. Because of wider surface conduction width and better gate controllability over the NW channels, DG mode of operation apparently exhibits higher ON current and a good subthreshold swing (SS) as low as 90 mV/dec at $V_D = 0.5$ V and 103 mV/dec at $V_D = 2$ V is obtained. Note that such SS performance is comparable to that of modern CMOS devices, despite the use of polycrystalline channels for the devices characterized in this letter. The SS is expected to reduce further as a thinner gate dielectric is used, while the ON current can be further improved by scaling the channel length. These trends were actually observed in a recent report [9]. It is also interesting to see that the drain current under DG mode is larger compared to the counterpart of the SG mode. Such phenomenon is postulated to be caused by the volume inversion effect [10] owing to the very thin body thickness of NW.

The two independent gate electrodes in the proposed configuration increase the flexibility in device operation. An example is shown in Fig. 5, in which the transfer characteristics of a device are depicted by sweeping inverse-T gate voltage with a fixed bias ranging from 3 to -3 V applied to the top gate. The figure also includes the characteristics under DG operation (the dashed line). For the SG-mode operations, it is clearly seen that the threshold voltage can be effectively modulated by the top gate voltage. Owing to the small volume of poly-Si NW, the channel potential is sensitive to both gates, and thus such strong gate-to-gate coupling phenomenon is observed. According to back-gate effect [7], the driven gate (or the inverse-T gate in the present case) has to overcome the impact of the back-gate (the top gate) bias on NW channel potential. As a consequence, the subthreshold slope in SG modes is reasonably larger than that in DG mode, as shown in the figure.

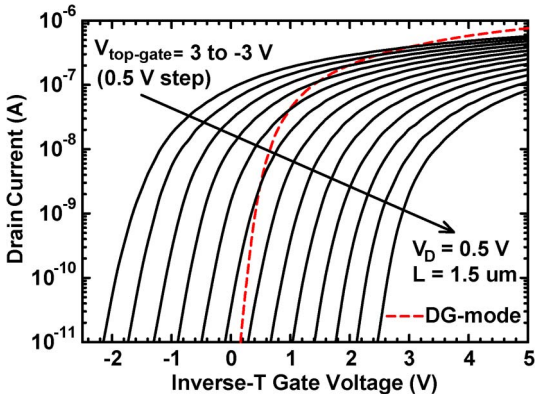

Fig. 5. Transfer characteristics of the MG device with inverse-T gate as the drive gate and top gate as the V_{TH} control gate. The dashed line is the results of the same devices under DG-mode operation.

In summary, a novel MG poly-Si NW device featuring an inverse-T gate together with a top gate to surround the poly-Si NW channels is proposed and fabricated. With this scheme, enhanced performance has also been demonstrated, including higher ON current, larger ON/OFF ratio and sharper subthreshold slope reaching around 90 mV/dec. Moreover, since the dimensions of the NW channel are small and the body is thin enough to cause strong coupling between the inverse-T gate and the top gate, the threshold voltage can be finely adjusted with suitable gate bias control.

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REFERENCES

[1] H. C. Lin, M. H. Lee, C. J. Su, T. Y. Huang, C. C. Lee, and Y. S. Yang, "A simple and low-cost method to fabrication TFTs with poly-Si nanowire channel," *IEEE Electron Device Lett.*, vol. 26, no. 9, pp. 643–645, Sep. 2005.

[2] H. C. Lin, M. H. Lee, C. J. Su, and S. W. Shen, "Fabrication and characterization of nanowire transistors with solid-phase crystallized poly-Si channels," *IEEE Trans. Electron Devices*, vol. 53, no. 10, pp. 2471–2477, Oct. 2006.

[3] H. C. Lin and C. J. Su, "High-performance poly-Si nanowire NMOS transistors," *IEEE Trans. Nanotechnol.*, vol. 6, no. 2, pp. 206–212, Mar. 2007.

[4] D. Hisamoto, W. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asana, T. King, J. Bokor, and C. Hu, "A folded channel MOSFET for deep-sub-tenth micron era," in *IEDM Tech. Dig.*, 1998, pp. 1032–1034.

[5] J. P. Colinge, A. J. Quinn, L. Floyd, G. Redmond, J. C. Alderman, W. Xiong, C. R. Cleavelin, T. Schulz, K. Schruefer, G. Knoblinger, and P. Patruno, "Low-temperature electron mobility in trigate SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 27, no. 2, pp. 120–122, Feb. 2006.

[6] S. D. Suk, S. Y. Lee, S. M. Kim, E. J. Yoon, M. S. Kim, M. Li, C. W. Oh, K. H. Yeo, S. H. Kim, D. S. Shin, K. H. Lee, H. S. Park, J. N. Han, C. J. Park, J. B. Park, D. W. Kim, D. Park, and B. I. Ryu, "High performance 5 nm radius twin silicon nanowire MOSFET (TSNWFET): Fabrication on bulk Si wafer, characteristics, and reliability," in *IEDM Tech. Dig.*, 2005, pp. 735–738.

[7] M. Masahara, Y. Liu, K. Sakamoto, K. Endo, T. Matsukawa, K. Ishii, T. Sekigawa, H. Yamauchi, H. Tanoue, S. Kanemaru, H. Koike, and E. Suzuki, "Demonstration, analysis and device design considerations for independent double-gate MOSFETS," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 2046–2053, Sep. 2005.

[8] F. J. García Ruiz, A. Godoy, F. Gámiz, C. Sampedro, and L. Donetti, "A comprehensive study of the corner effects in Pi-Gate MOSFETs including quantum effects," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3369–3377, Dec. 2007.

[9] M. Im, J.-W. Han, H. Lee, L.-E. Yu, S. Kim, S. C. Jeon, K. H. Kim, G. S. Lee, J. S. Oh, Y. C. Park, H. M. Lee, and Y.-K. Choi, "Multiple-gate CMOS thin-film transistor with polysilicon nanowire," *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 102–104, Jan. 2008.

[10] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance," *IEEE Electron Device Lett.*, vol. EDL-8, no. 9, pp. 410–412, Sep. 1987.