Impact of Process-Induced Strain on Coulomb Scattering Mobility in Short-Channel n-MOSFETs

William P. N. Chen, Pin Su, *Member, IEEE*, and K. Goto, *Member, IEEE*

***Abstract*—This letter provides an experimental assessment of Coulomb scattering mobility for advanced short-channel strained devices. By accurate mobility extraction under various temperatures, we examine the impact of process-induced uniaxial strain on Coulomb mobility in short-channel nMOSFETs. This letter indicates that the Coulomb mobility has significant stress dependency. Moreover, the stress sensitivity of the Coulomb mobility shows strong temperature dependence. Because it is the interface scattering that counteracts the stress sensitivity of the bulk-impurity-limited mobility, further reducing the interface charges will be crucial to future mobility scaling.**

***Index Terms*—Coulomb mobility, MOSFET, strained silicon.**

I. INTRODUCTION

UNIAXIAL strained-Si technology is critical to transistor performance in nanoscale CMOS development [1], [2]. The improvement of current drive shows strong correlation with the low-field mobility enhancement by uniaxial strain [3]. Recently, several studies [4]–[9] reported degraded carrier mobility for short-channel devices and pointed out the increasing importance of Coulomb scatterings. Whether or not the Coulomb scattering mobility can be enhanced by process-induced strain merits investigation.

Although Gamiz *et al.* [6] and Nayfeh *et al.* [5] have shown that Coulomb mobility is not enhanced in strained-Si nMOSFETs, Weber and Takagi [4] have demonstrated that the mobility that is limited by substrate impurity scattering is still enhanced in long-channel strained devices ($L = 10\ \mu$m). These findings seem to be inconsistent, and further examination on Coulomb mobility is needed.

In this letter, we tackle the problem by using advanced short-channel strained devices. By accurate mobility extraction under various temperatures, we assess the impact of process-induced uniaxial strain on Coulomb mobility in short-channel nMOSFETs.

II. EXPERIMENTAL

N-channel MOSFETs with channel direction $\langle 110 \rangle$ with neutral and compressive uniaxial Contact Etch Stop Layers (CESLs) were manufactured based on state-of-the-art CMOS technology on 300 mm (100) silicon substrate. The devices with neutral and compressive CESL films were implanted by same p-pocket conditions. The effective bulk concentrations are 2×10^{18} cm^{-3} and 3×10^{17} cm^{-3} at short- and long-channel devices, respectively, based on TCAD simulation.

The compressive CESL induces stronger compressive stress along the silicon channel direction as gate length becomes shorter. This is mainly attributed to the corner and the direct CESL effect [18]. The corner effect is due to the interaction of lateral and bottom CESLs, resulting in compressive stress along the channel direction. The direct CESL effect is dominated by the bottom-CESL effect. Both corner and direct CESL effects have higher stress efficiency on shorter channel devices. Based on TCAD stress simulation, the average stress levels for $L_G = 90$ nm along the channel direction are -0.165 and -0.599 GPa ("$-$" means compressive stress) for neutral and compressive CESL nitride films, respectively. The average stress levels vertical to the silicon surface are -0.079 and 4.120 GPa for neutral and compressive CESL nitride films, respectively. The average stress levels along the width direction are -0.684 and -0.522 GPa for neutral and compressive CESL nitride films, respectively. The way to control the stress level of CESL films is to modify film compositions or thicknesses by different deposition parameters. In general, stronger compressive CESL or thicker compressive CESL film means stronger compressive stress applied along the silicon channel.

The devices with effective channel length (L_{EFF}) ranging from 975 to 90 nm were examined. In order to extract the short-channel mobility, special transistor arrays were designed. Split C–V measurement [10], [11], [15] was used to characterize the inversion charge density (Q_{inv}) and the bulk charge density (Q_b) for long- and short-channel devices, respectively. After the gate-to-channel capacitance with floating bulk terminal (C_{gc}) was calibrated by considering the parasitic components such as overlap capacitance and fringing capacitance [12], [13], Q_{inv} was obtained by integrating the entire C_{gc} curve from the flatband voltage. When the gate-to-channel capacitance with source/drain/bulk tied together (C_{gg}) was calibrated by using the same procedure, Q_b can be obtained [16].

The intrinsic drain–current (I_d) was calibrated by considering the series-resistance (R_{sd}) effect [14]. The physical poly gate length (L_{phy}) was obtained by using inline SEM measurement. The LDD overlap region under the gate (L_{ov}) was

Manuscript received February 11, 2008. This work was supported in part by the National Science Council, Taiwan, under Contract NSC95-2221-E-009-327-MY2 and in part by the Ministry of Education, Taiwan, under the ATU program. The review of this letter was arranged by Editor Y. Taur.

W. P. N. Chen is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C., and also with Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu 300, Taiwan, R.O.C.

P. Su is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

K. Goto is with Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu 300, Taiwan, R.O.C.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2008.2000909

0741-3106/$25.00 © 2008 IEEE

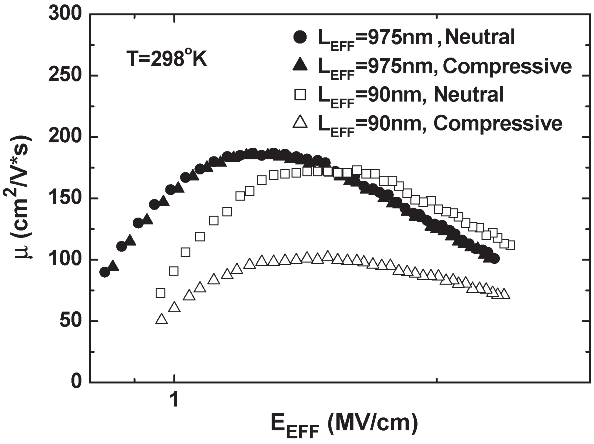

Fig. 1. Our extracted short-channel mobility shows significant dependence on the uniaxial stressor applied.

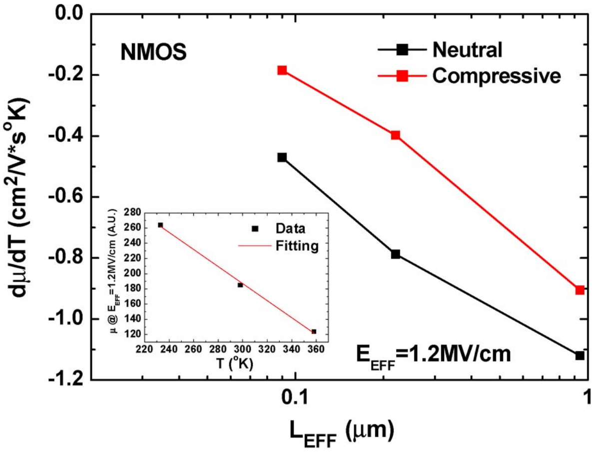

Fig. 2. Temperature dependence of the mobility at ($E_{\mathrm{EFF}} = 1.2$ MV/cm) versus L_{EFF}. (Inset) $d\mu/dT$ is extracted in the temperature range from 233 °K to 358 °K.

extracted by the split CV method [7]. The effective channel length (L_{EFF}) can then be derived by subtracting L_{ov} from L_{phy}. Finally, the mobility can be extracted by Eq. (1):

$$\mu = \frac{I_d \cdot L_{\mathrm{EFF}}}{W \cdot Q_{\mathrm{inv}} \cdot V_{\mathrm{ds}}}. \tag{1}$$

III. RESULTS AND DISCUSSION

Fig. 1 shows the extracted mobility of long- and short-channel devices versus the vertical electrical field (E_{EFF}). It can be seen that the short-channel mobility significantly depends on the stress level. Fig. 2 shows the temperature dependence of the mobility at $E_{\mathrm{EFF}} = 1.2$ MV/cm. As gate length decreases, the temperature sensitivity of the mobility changes. It has been known that the importance of Coulomb mobility also increases as gate length decreases [4]–[9].

To extract the Coulomb mobility, we use Matthiessen's rule and assume that the universal mobility curve (UMC) follows the measurement data in the high-field region [5]. In order to verify the accuracy of the extracted Coulomb mobility, we have compared the extracted Coulomb mobility under various UMCs (±10%), as shown in Fig. 3. It can be seen that the extracted

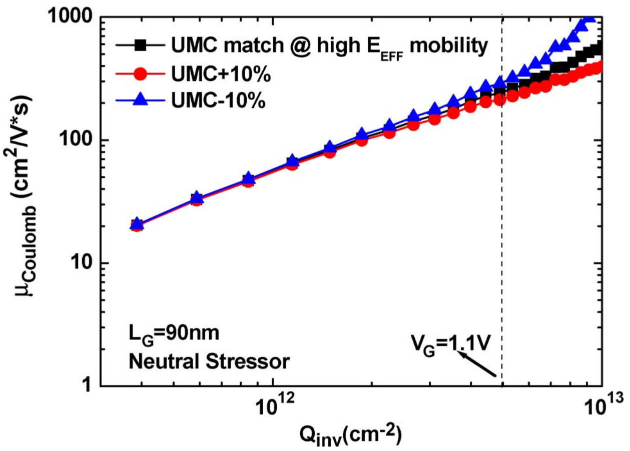

Fig. 3. We have varied the UMC by ±10% to verify the accuracy of our extracted Coulomb mobility.

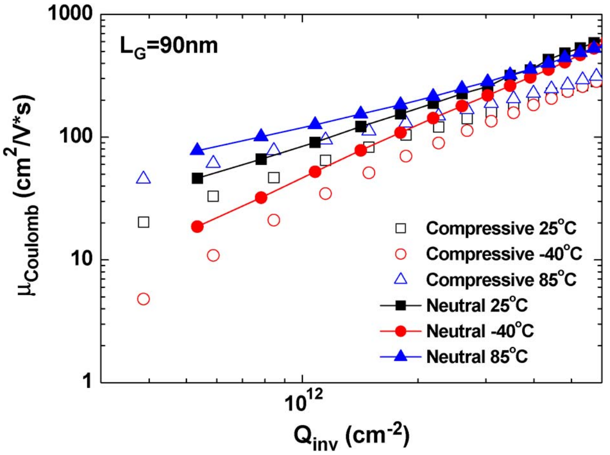

Fig. 4. Coulomb mobility for short-channel devices with different stressors under various temperatures.

Coulomb mobility curves remain almost the same when Q_{inv} is smaller than 5×10^{12} cm^{-2}, at which V_G is about 1.1 V.

Fig. 4 shows the Coulomb mobility for the short-channel devices with different stressors under various temperatures. It can be seen that, in the low vertical field region, the Coulomb mobility decreases with temperature. This is because slower electrons are more susceptible to Coulomb scattering [17]. Moreover, the Coulomb mobility shows significant stress dependency. In other words, strain engineering can still be employed to modulate the Coulomb scattering mobility of short-channel nMOSFETs. It is worth noting that our result is inconsistent with the results in [5] and [6].

Fig. 5 shows the stress sensitivity of the short-channel Coulomb mobility at various temperatures. It can be seen that, in the low vertical field region, the stress sensitivity decreases as temperature increases. It is plausible that two competing mechanisms, namely, bulk impurity scattering and interface scattering, are responsible for our observation. As pointed out in [4], the mobility that is limited by bulk impurity scattering (μ_b) shows opposite stress sensitivity to the mobility that is limited by interface scattering (μ_{it}). Although the bulk impurity scattering of the short-channel nFET increases under the compressive stress, the interface scattering becomes less because there are more electrons in the 4-fold valley. These two

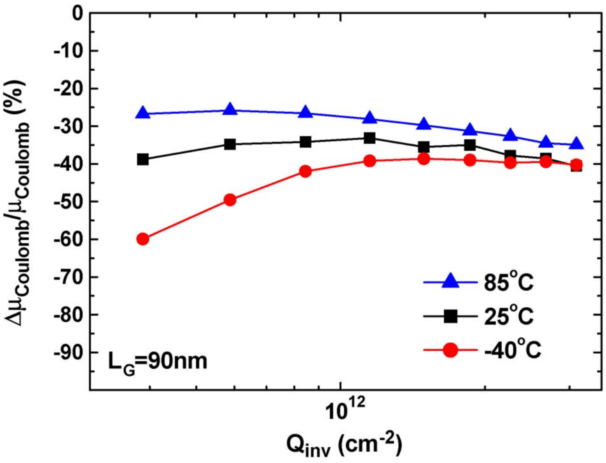

Fig. 5. Stress sensitivity of Coulomb mobility under various temperatures. The $\Delta\mu_{\text{Coulomb}}$ represents $\mu_{\text{Coulomb\_strain}} - \mu_{\text{Coulomb\_neutral}}$.

mechanisms counteract each other and determine the overall stress dependency of Coulomb mobility. As temperature increases, the importance of interface scattering increases [17]. As a result, the stress dependency of the overall Coulomb mobility decreases.

IV. CONCLUSION

We have examined the impact of process-induced uniaxial strain on Coulomb mobility for short-channel nMOSFETs. This letter indicates that the Coulomb mobility has significant stress dependency. Moreover, the stress sensitivity of the Coulomb mobility shows strong temperature dependence. Because it is the interface scattering that counteracts the stress sensitivity of the bulk-impurity-limited mobility, further reducing the interface charges will be crucial to future mobility scaling.

REFERENCES

[1] Z. Luo, N. Rovedo, S. Ong, B. Phoong, M. Eller, H. Utomo, C. Ryou, H. Wang, R. Stierstorfer, L. Clevenger, S. Kim, J. Toomey, D. Sciacca, J. Li, W. Wille, L. Zhao, L. Teo, T. Dyer, S. Fang, J. Yan, O. Kwon, D. Park, J. Holt, J. Han, V. Chan, J. Yuan, T. Kebede, H. Lee, S. Kim, S. Lee, A. Vayshenker, Z. Yang, C. Tian, H. Ng, H. Shang, M. Hierlemann, J. Ku, J. Sudijono, and M. Ieong, “High performance transistors featured in an aggressively scaled 45nm bulk CMOS technology,” in *VLSI Symp. Tech. Dig.*, 2007, pp. 16–17.

[2] F. Andrieu, T. Ernst, F. Lime, F. Rochette, K. Romanjek, S. Barraud, C. Ravit, F. Boeuf, M. Jurczak, M. Casse, O. Weber, L. Brevard, G. Reimbold, G. Ghibaudo, and S. Delenibus, “Experimental and comparative investigation of low and high field transport in substrate- and process-induced strained nanoscaled MOSFETs,” in *VLSI Symp. Tech. Dig.*, 2005, pp. 176–177.

[3] K.-W. Ang, J. Lin, C.-H. Tung, N. Balasubramanian, G. Samudra, and Y.-C. Yeo, “Beneath-the-channel strain-transfer-structure (STS) and embedded source/drain stressors for strain and performance enhancement of nanoscale MOSFETs,” in *VLSI Symp. Tech. Dig.*, 2007, pp. 42–43.

[4] O. Weber and S.-I. Takagi, “New findings on Coulomb scattering mobility in strained-Si nFETs and its physical understanding,” in *VLSI Symp. Tech. Dig.*, 2007, pp. 130–131.

[5] H. M. Nayfeh, C. W. Leitz, A. J. Pitera, E. A. Fitzgerald, J. L. Hoyt, and D. A. Antoniadis, “Influence of high channel doping on the inversion layer electron mobility in strained silicon n-MOSFETs,” *IEEE Electron Device Lett.*, vol. 24, no. 4, pp. 248–250, Apr. 2003.

[6] F. Gamiz, J. B. Roldan, J. A. Lopez-Villanueva, and P. Cartujo, “Coulomb scattering in strained-silicon inversion layers on $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ substrates,” *Appl. Phys. Lett.*, vol. 69, no. 6, p. 797, Aug. 1996.

[7] A. Cros, K. Romanjek, D. Fleury, S. Harrison, R. Cerutti, P. Coronel, B. Dumont, A. Pouydebasque, R. Wacquez, B. Duriez, R. Gwoziecki, F. Boeuf, H. Brut, G. Ghibaudo, and T. Skotnicki, “Unexpected mobility degradation for very short devices: A new challenge for CMOS scaling,” in *IEDM Tech. Dig.*, 2006, pp. 1–4.

[8] K. Rim, S. Narasimha, M. Longstreet, A. Mocuta, and J. Cai, “Low field mobility characteristics of sub-100 nm unstrained and strained Si MOSFETs,” in *IEDM Tech. Dig.*, 2002, pp. 43–46.

[9] H. Ohta, H. Fukutome, T. Sakuma, A. Hatada, K. Ohkoshi, K. Ikeda, T. Miyashita, T. Mori, and T. Sugii, “Novel thin sidewall structure for high performance bulk CMOS with charge-assisted source–drain-extension,” in *VLSI Symp. Tech. Dig.*, 2007, pp. 120–121.

[10] K. Romanjek, F. Andrieu, T. Ernst, and G. Ghibaudo, “Improved split C–V method for effective mobility extraction in sub-0.1-μm Si MOSFETs,” *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 583–585, Aug. 2004.

[11] K. Romanjek, F. Andrieu, T. Ernst, and G. Ghibaudo, “Characterization of the effective mobility by split $C(V)$ technique in sub 0.1 μm Si and SiGe PMOSFETs,” *Solid-State Electron.*, vol. 49, no. 5, pp. 721–726, May 2005.

[12] F. Pregaldiny, C. Lallement, and D. Mathiot, “A simple efficient model of parasitic capacitances of deep-submicron LDD MOSFETs,” *Solid-State Electron.*, vol. 46, no. 12, pp. 2191–2198, Dec. 2002.

[13] J. R. Hauser *et al.*, “Characterization of ultrathin oxides using electrical C–V and I–V measurements,” in *Proc. Int. Conf. Characterization Metrol. ULSI Technol.*, 1998, p. 235.

[14] W. P. N. Chen, P. Su, J. S. Wang, C. H. Lien, C. H. Chang, K. Goto, and C. H. Diaz, “A new series resistance and mobility extraction method by BSIM model for nano-scale MOSFETs,” in *VLSI Symp. Tech. Dig.*, 2006, pp. 143–144.

[15] F. Aandrieu, T. Ernst, C. Ravit, M. Jurczak, G. Ghibaudo, and S. Deleonibus, “In-depth characterization of the hole mobility in 50-nm process-induced strained MOSFETs,” *IEEE Electron Device Lett.*, vol. 26, no. 10, pp. 755–757, Oct. 2004.

[16] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. Hoboken, NJ: Wiley, 2006.

[17] K. Chain, J.-H. Huang, J. Duster, P. K. Ko, and C. Hu, “A MOSFET electron mobility model of wide temperature range (77–400 K) for IC simulation,” *Semicond. Sci. Technol.*, vol. 12, no. 4, p. 355, Apr. 1997.

[18] S. Orain, V. Fiori, D. Villanueva, A. Dray, and C. Ortolland, “Method for managing the stress due to the strained nitride capping layer in MOS transistors,” *IEEE Trans. Electron Devices*, vol. 54, no. 4, p. 814, Apr. 2007.