Temperature-Dependent Capacitance Characteristics of RF LDMOS Transistors With Different Layout Structures

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***Abstract*—In this letter, the capacitance characteristics of RF LDMOS transistors with different temperatures and layout structures were studied. In a conventional fishbone structure, the peaks in capacitances decrease with increasing temperature. For the ring structure, two peaks in a capacitance–voltage curve have been observed at high drain voltages due to the additional corner effect. In addition, peaks in gate-to-source/body capacitance decrease and peaks in gate-to-drain capacitance increase with increasing temperature at high drain voltages. By analyzing the effects of temperature on threshold voltage, quasi-saturation current, and drift depletion capacitance, the variations of capacitances with temperature were investigated.**

***Index Terms*—Capacitance, drift region, laterally diffused MOS (LDMOS), layout structure, nonuniform doping, temperature.**

I. Introduction

RF POWER amplifiers are key components in base stations for personal communication systems [1]. Due to its advantages in performance, cost, reliability, and power capability, laterally diffused MOS (LDMOS) transistor technology has played a predominant role in the power amplifier applications [2]. Because the device capacitances influence the input, output, and feedback capacitances, which are important in the dynamic operation, and have large impact on device high-frequency performance, the capacitance characterization and modeling of LDMOS transistors have been studied widely [3]–[7]. As compared to the conventional MOSFET, a nonuniform doping channel and a drift region in LDMOS result in the unusual behavior in capacitances [8], [9]. Since the power transistors are operated at high power densities, the device temperature is high due to self-heating effect. Therefore, we are interested to know the temperature effects on the capacitance characteristics of LDMOS transistors, which are not mentioned in previous papers. In this letter, the capacitance characteristics of LDMOS transistors with different layout structures were studied at temperatures from -25 °C to 125 °C.

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II. Experiments

The RF LDMOS transistors used in this letter are fabricated using a 40-V LDMOS process [10]. The gate oxide thickness is 135 Å. The mask channel length and drift length are 0.5 and 3.6 μm, respectively. The mask channel length is the length of the p-base region, which is overlapped by the poly-gate defined by mask. The p-type region defining the channel is implanted after the poly-gate deposition and the channel length is defined by out diffusion. The LDMOS transistors were designed with two types of layout structures [10]. In the "fishbone" structure, all the gate fingers are divided into six subcells, in each of which six gate fingers are grouped together with a finger width (L_F) of 10 μm. To achieve a lower ON-resistance, we adopted a square "ring" structure in the layout design. All the rings were arranged as a 3×3 array in one device. In each ring, the source region was surrounded by the drain region, while the gate was located between the source and the drain. The gate width of each square ring was 40 μm. The maximum oscillation frequencies of the fishbone and ring structures were 9 and 11 GHz, respectively [10]. The gate-to-source/body capacitance ($C_{\rm GS} + C_{\rm GB}$) and gate-to-drain capacitance ($C_{\rm GD}$) were extracted from the deembedded S-parameters in low-frequency range [11].

III. Results and Discussion

The extracted $C_{\rm GS} + C_{\rm GB}$ and $C_{\rm GD}$ at room temperature are shown in Fig. 1. At low drain bias ($V_{\rm DS} = 0.1$ V), both fishbone and ring have the same physical mechanism for the capacitance. The $C_{\rm GS} + C_{\rm GB}$ presents a similar behavior to the conventional MOSFET. For the lateral nonuniformly doped channel in LDMOS, the drain end will be inverted prior to the source end, resulting in a peak in $C_{\rm GD}$ [7]. Once the gate voltage ($V_{\rm GS}$) exceeds the threshold voltage ($V_{\rm TH}$), the $C_{\rm GD}$ starts to fall as the electron charge sheet is no longer connected only to the drain.

By increasing the drain voltage ($V_{\rm DS} > 0.5$ V), both $C_{\rm GS} + C_{\rm GB}$ and $C_{\rm GD}$ present peaks. Because the inversion charges may be injected from the intrinsic MOSFET to the depleted area of the drift, the $C_{\rm GD}$ and $C_{\rm GS} + C_{\rm GB}$ increase with increasing gate voltages, and the $C_{\rm GS} + C_{\rm GB}$ even rises over the limit of

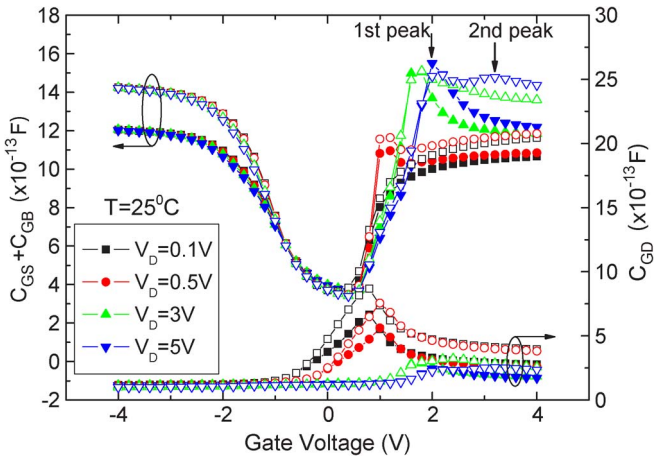

Fig. 1. Extracted $C_{\rm GS}+C_{\rm GB}$ and $C_{\rm GD}$ versus gate voltage for different drain biases. Solid symbols: Fishbone structure. Hollow symbols: Ring structure.

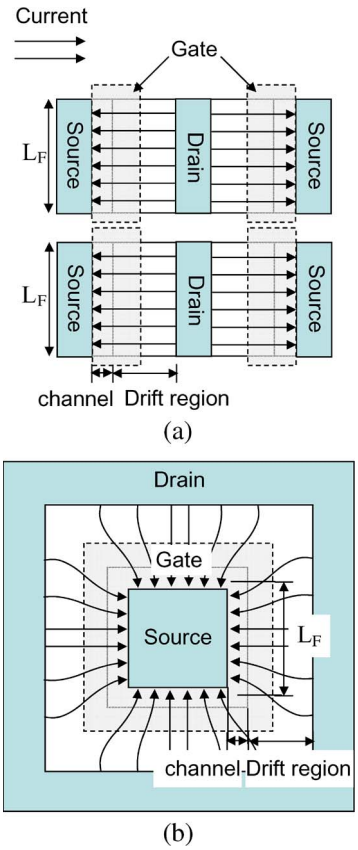

Fig. 2. Schematic view of layout structure and current distribution: (a) fishbone structure and (b) ring structure.

inversion [4]. The $C_{\rm GS}+C_{\rm GB}$ and $C_{\rm GD}$ reach maximum at the onset of quasi-saturation [12]. Because the higher drain voltage leads to a higher gate voltage at the onset of quasi-saturation, the peaks shift to higher gate voltages.

For the ring structure, however, additional peaks in $C_{\rm GS}+C_{\rm GB}$ and $C_{\rm GD}$ were observed when biasing at high drain voltage ($V_{\rm DS}=5$ V) (see Fig. 1). As shown in Fig. 2, the currents flow from drain to source with uniform distribution in the full region of the fishbone structure. However, in the ring structure, the corner region of the drift shows lower current density than

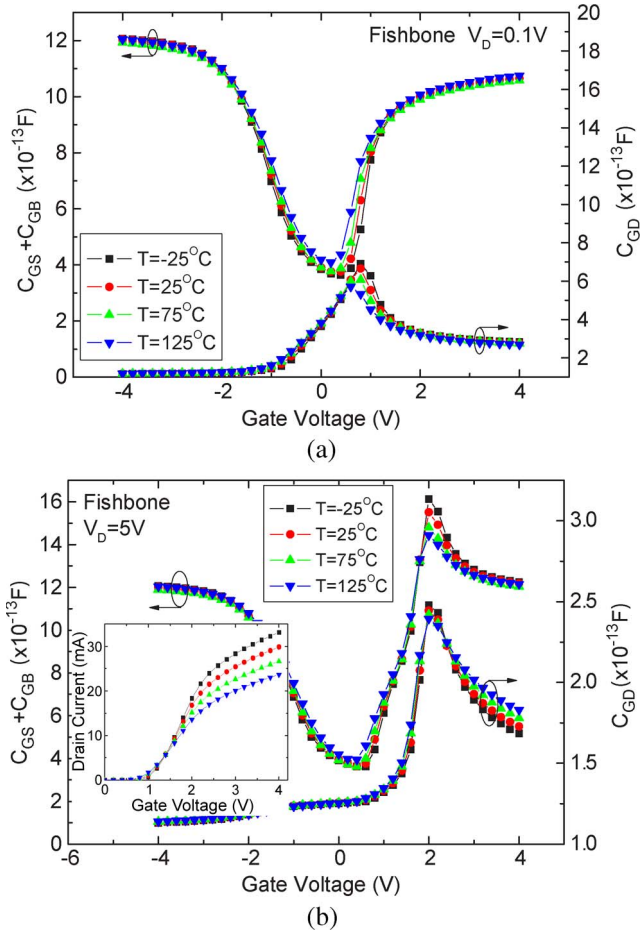

Fig. 3. Extracted $C_{\rm GS}+C_{\rm GB}$ and $C_{\rm GD}$ versus gate voltage with various temperatures (a) at drain voltage $V_{\rm DS}=0.1$ V and (b) at drain voltage $V_{\rm DS}=5$ V for a fishbone structure. The inset shows the drain current versus gate voltage with various temperatures.

the edge region [13], [14], and thus it needs higher gate voltage to enter quasi-saturation. At the first peak, although the edge of the square ring operates in quasi-saturation region, the corner is still in prequasi-saturation. By increasing the gate voltage to 3.2 V, the current in the corner region is high enough to make the velocity of electrons in the drift saturated. Therefore, the corner operates in quasi-saturation and second peaks are generated in the $C_{\rm GS}+C_{\rm GB}$ and $C_{\rm GD}$.

Fig. 3 shows the influence of temperature on $C_{\rm GS}+C_{\rm GB}$ and $C_{\rm GD}$ of the fishbone structure. At $V_{\rm DS}=0.1$ V, the transistor operates in linear region and the temperature dependence of $C_{\rm GS}+C_{\rm GB}$ is similar to the conventional MOSFET. With increasing temperature, the threshold voltage decreases and the flatband voltage increases due to higher intrinsic carrier concentration [15]. In our devices, the variation of the threshold voltage with temperature is -1.66 mV/°C, which equals the shift of the $C_{\rm GD}$ peak. In addition, the lower threshold voltage at higher temperature also indicates that the source end is inverted easier. It results in the reduction of $C_{\rm GD}$ with increasing temperature when the transistor operates in weak and moderate inversion regimes.

At $V_{\rm DS}=5$ V, the transistor operates in saturation region, and the temperature coefficients of $C_{\rm GS}+C_{\rm GB}$ and $C_{\rm GD}$ are positive in weak and moderate inversion regimes, due to the

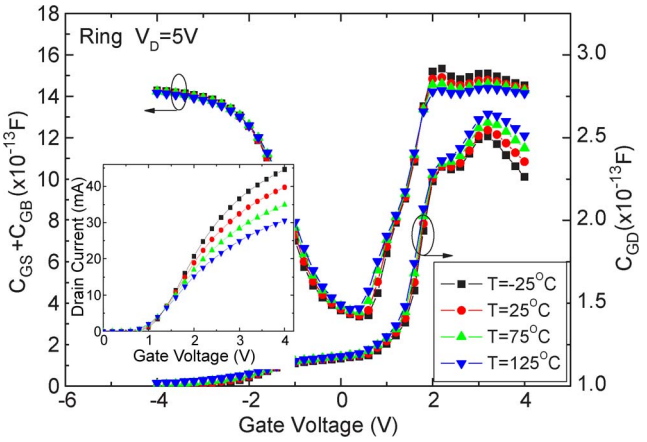

Fig. 4. Extracted $C_{\rm GS}+C_{\rm GB}$ and $C_{\rm GD}$ versus gate voltage with various temperatures at drain voltage $V_{\rm DS}=5$ V for a ring structure. The inset shows the drain current versus gate voltage with various temperatures.

reduction of threshold voltage. From Fig. 3(b), we know that the shift of the $C_{\rm GS}+C_{\rm GB}$ curve at $V_{\rm GS}=V_{\rm TH}$ is about -1.52 mV/°C, which approaches the temperature coefficient of the threshold voltage (~ -1.64 mV/°C). At higher gate voltages ($V_{\rm GS}>2$ V), the values of capacitances are determined by the onset of quasi-saturation and by the drift depleted region. Because the quasi-saturation current decreases with increasing temperature [see the inset in Fig. 3(b)], the peak value of capacitances decreases. It should be noted that the $C_{\rm GD}$ shows different behavior with temperature between low and high drain biases when the transistors operate at higher gate voltages ($V_{\rm GS}>2.5$ V). At low drain voltage, the $C_{\rm GD}$ is dominated by the accumulation charge which formed below the thin oxide in the drift region and decreases slightly with increasing temperature [see Fig. 3(a)]. At high drain voltages, the $C_{\rm GD}$ now is dominated by the drift depletion capacitance and increases with increasing temperature [see Fig. 3(b)]. Since the temperature variation of capacitance peaks is significantly affected by the drift region, device optimization could be done by changing the drift region length and drift doping concentration.

For the ring structure, the temperature dependence of capacitances is similar to that of the fishbone structure at $V_{\rm DS}=0.1$ V (not shown here). Because the capacitance behavior is mainly related to the threshold voltage at low drain biases, the influence of corners can be neglected. At $V_{\rm DS}=5$ V, the temperature coefficients of $C_{\rm GS}+C_{\rm GB}$ and $C_{\rm GD}$ are positive in weak and moderate inversion regimes, due to the reduction of threshold voltage, as shown in Fig. 4. The shift of the $C_{\rm GS}+C_{\rm GB}$ curve at $V_{\rm GS}=V_{\rm TH}$ is about -1.42 mV/°C, which approaches the temperature coefficient of the threshold voltage (~ -1.56 mV/°C). At higher gate voltage ($V_{\rm GS}>2$ V), the peaks of $C_{\rm GS}+C_{\rm GB}$ decrease with increasing temperature due to lower quasi-saturation current (see the inset in Fig. 4). However, the peaks of $C_{\rm GD}$ increase with temperature, which is contrary to the trend in a fishbone structure. At the first peak, although the edge of the square ring has been in quasi-saturation region, the corner is still in prequasi-saturation. Therefore, the increase of $C_{\rm GD}$ peak with temperature indicates that the temperature-induced variation of $C_{\rm GD}$ is dominated by the corner. At the second peak, the corner has also been in quasi-saturation region, however, the $C_{\rm GD}$ in the edge has been dominated by the drift depletion capacitance. Because the drift depletion capacitance is very sensitive to the temperature as indicated in Fig. 3(b), the temperature-induced variation of $C_{\rm GD}$ now is dominated by the edge.

IV. Conclusion

The capacitance behaviors of RF LDMOS transistors with different temperatures were investigated. At low drain voltages, the temperature coefficients of $C_{\rm GS}+C_{\rm GB}$ are positive, while the temperature coefficients of $C_{\rm GD}$ are negative. At high drain voltages, peaks in $C_{\rm GS}+C_{\rm GB}$ have also been observed and their temperature coefficients are negative. However, the temperature coefficients of $C_{\rm GD}$ peaks are negative in a fishbone structure and positive in a ring structure. These observations are important for circuit design to choose a bias condition with lower temperature sensitivity in capacitances. In addition, since the capacitances are affected mainly by the threshold voltage, quasi-saturation current, and drift depletion capacitance, temperature effects on these parameters must be considered in the LDMOS capacitance model.

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