Duty Phase Control for Single-Phase Boost-Type SMR

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***Abstract*—In this paper, a novel duty phase control (DPC) for single-phase boost-type switching-mode-rectifier (SMR) is developed and digitally implemented in DSP-based system. Compared to the conventional multiloop control structure with inner current loop and outer voltage loop, it is noted that there is only one voltage loop tuning the phase of predefined duty pattern (i.e. duty phase) in the proposed DPC. Due to no current loop, sampling inductor current and tracking current are unnecessary when SMRs are operated to shape the current waveform and regulate the output voltage. It implies that the single-loop DPC is simple and adaptable to the implementation with digital and analog integrated circuits. In this paper, first, the effect of the duty phase on the input current is analyzed and modeled. It shows that the sinusoidal current waveform can be naturally generated by the predefined duty pattern and the current amplitude is roughly proportional to the controllable duty phase. Then, a voltage controller is designed to regulate the dc output voltage by tuning this duty phase. Finally, some simulated and experimental results have been given to illustrate the performances of the proposed DPC.**

***Index Terms*—Duty phase control, power factor correction, sensorless, SMR.**

I. Introduction

THE ac–dc converter is an essential component for most power electronic systems to build up dc-link voltage source from the ac mains. The use of switching-mode-rectifier (SMR) [1]–[3] with power factor correction (PFC) function is an effective mean to perform the ac–dc conversion with high quality by shaping the input current waveform and regulating the output dc voltage. The boost-type SMRs are the most popular circuit topology among all the others to shape the current waveform for their continuous current in the front-end inductors [1].

In order to let the boost-type SMRs have good input and output performances, many types of voltage and current control approaches have been developed, such as feedforward current control [3]–[6], robust voltage and current control [3], [7], and predictive current control [8], [9]. The multiloop control is the most popular structure to coordinate the individual voltage and current control to meet the input and output specifications by controlling the single power switch.

However, there are two drawbacks in the common multiloop control for boost-type SMRs. One is that the output voltage ripple through the outer voltage loop will result in the distorted current command into the inner current loop. The other is the difficulty of deciding the current sampling instants due to the large variations in the switching duty of the boost-type SMRs. However, it is clear that the above two problems are relating to the inner current loop and, thus, if there is no current loop in the new control structure, both the problems and the cost of current sensing can be removed in the operations of boost-type SMRs. It also implies that only one voltage loop can be found in the new control structure, and thus, such single-loop control structure is very competitive for its simplicity.

The proposed duty phase control (DPC) can be seen as the single-loop structure with only one voltage loop tuning the phase of the predefined duty pattern (i.e. duty phase). Compared to the simple single-loop voltage mode control under discontinuous current mode (DCM), the proposed single-loop DPC is working in continuous current mode (CCM). Therefore, the developed DPC is easy, current sensorless and loopless.

The paper is organized as follows. Initially, the phase effect of the predefined duty pattern on input current is analyzed and modeled. The results show that the sinusoidal current waveform can be automatically generated by the predefined duty pattern and the input current amplitude is roughly proportional to the duty phase. Subsequently, based on the effect of duty phase on the input current amplitude, a voltage controller can be included to regulate the dc output voltage by means of tuning the duty phase. Finally, some simulated and experimental results have been given to illustrate the performance of the proposed DPC. The measurements also show that the drawn harmonic currents are well below the limits of the standard IEC 61000-2-3.

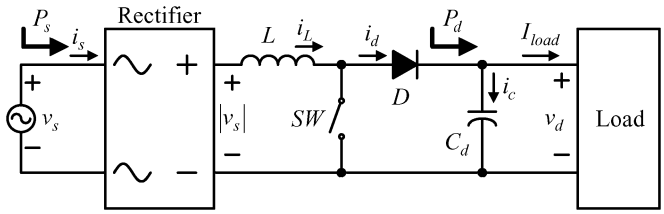

Fig. 1. Power circuit of the boost-type SMR.

II. Boost-Type SMRs

A. Modeling

As shown in Fig. 1, the power circuit of the boost-type SMR mainly consists of a diode bridge rectifier and a boost-type dc–dc converter. In order to model the behaviors of the boost-type SMR, some assumptions are initially made:

1) circuit elements are ideal and thus, lossless;

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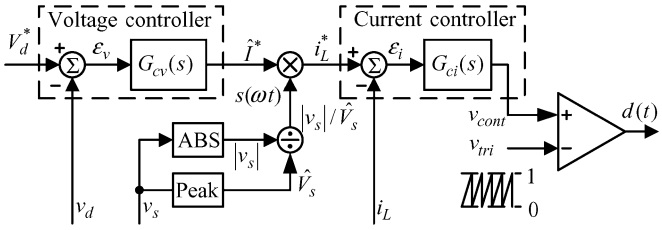

Fig. 2. Conventional multiloop control for boost-type SMRs.

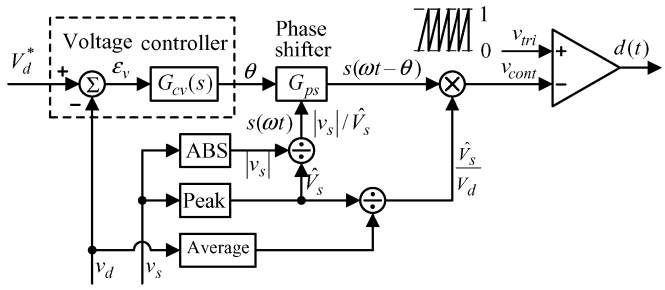

Fig. 3. Proposed DPC for boost-type SMRs.

2) power switch SW operates at a switching frequency approaching infinity;
3) a bulk capacitor C_d is included in the power circuit and thus, the output voltage v_d can be assumed to be its average value V_d.

Therefore, the above three assumptions allows the following equation on an instantaneous basis:

$$v_s(t)i_s(t) = P_s(t) = P_d(t) = v_d(t)i_d(t) \approx V_d i_d(t) \quad (1)$$

where $P_s(t)$ and $P_d(t)$ are the instantaneous input power and output power, respectively. Furthermore, when the boost-type SMR is operating in CCM with unity power factor, the drawn input power $P_s(t)$ can be expressed as the product of input current $i_s(t) = \hat{I}_s \sin(\omega t)$ and input voltage $v_s(t) = \hat{V}_s \sin(\omega t)$

$$P_s(t) = \hat{V}_s \sin(\omega t) \times \hat{I}_s \sin(\omega t) = \overline{P}_s + \overline{P}_s \cos(2\omega t) \quad (2)$$

where $\overline{P}_s = \hat{V}_s \hat{I}_s/2$ is the average input power.Therefore, from the above two equations, we can obtain the output current

$$i_d(t) = \frac{P_s(t)}{V_d} = \frac{\hat{V}_s \hat{I}_s}{2V_d} - \frac{\hat{V}_s \hat{I}_s}{2V_d} \cos(2\omega t) \triangleq I_{load} + i_c(t) \quad (3)$$

where the average value of i_d is

$$I_d = I_{load} = \frac{\hat{V}_s \hat{I}_s}{2V_d} \quad (4)$$

and the current through the capacitor is

$$i_c(t) = -\frac{\hat{V}_s \hat{I}_s}{2V_d} \cos(2\omega t) = -I_d \cos(2\omega t). \quad (5)$$

Then, the ripple $v_{d,ac}$ in v_d can be estimated from (5) as

$$v_{d,ac}(t) \approx \frac{1}{C_d} \int i_c(t) = -\frac{\hat{V}_s \hat{I}_s}{4\omega C_d V_d} \sin(2\omega t). \quad (6)$$

B. Multiloop Control

The above derivations mainly come from considering the relations between input and output waveforms and neglecting the detailed switching behavior of the boost-type SMRs. Therefore, as shown in Fig. 2, the popular multiloop control for boost-type SMRs are not based on (1)through (6) but based on the following straightforward principles of waveform tracking and power balance.

From the balance between input and output power, the adequate current amplitude can be certainly obtained to maintain the desired output voltage. Therefore, in the multiloop control shown in Fig. 2, the input current amplitude $\hat{I}^*$ can be yielded to regulate the output voltage through the outer voltage controller. By multiplying $\hat{I}^*$ with the unity rectified signal $s(\omega t) = |\sin \omega t|$, the inductor current command i_L^* for the desired load condition can be obtained. Then, the switching signal $d(t)$ in Fig. 2 is generated by comparing the current controller output signal $v_{\rm cont}$ and triangular signal $v_{\rm tri}$ at the comparator's $(+)$ terminal and $(-)$ terminal, respectively.

However, we can find two drawbacks in the above multiloop control. The first one is that significant ripple voltage on the output voltage $v_d(t)$ will result in the double line-frequency component in the current command magnitude $\hat{I}^*$ by the voltage controller. It follows that the line current waveform is regulated to trace a distorted current command [3]. The double line-frequency component can be easily reduced by increasing the output capacitance C_d or decreasing the bandwidth of voltage loop, but the dynamic response of output voltage must be slow down [7].

The second drawback is that determining a fixed instant for sampling current is difficult due to the large variation of the switching instant at each switching period. In practice, a specific strategy for sampling current is required in order to avoid sensing the switching noise.

The above two problems are related to the current loop and therefore, both drawbacks can be found if the current loopless control is developed. In this paper, the proposed DPC can be seen as one of current loopless control.

III. Proposed Duty Phase Control

The configuration of the proposed DPC is plotted in Fig. 3 where only one voltage controller is used. The DPC technique can be regarded as a current loopless control or a single-loop control. Like the conventional configuration in Fig. 2, the duty signal $d(t)$ is also generated by comparing the carrier signal $v_{\rm tri}$ and the control signal $v_{\rm cont}$. It is noted that the signal $v_{\rm tri}$ in Fig. 3 is input at the comparator's $(+)$ terminal, but the same signal in Fig. 2 is at $(-)$ terminal. Besides, the control signal $v_{\rm cont}$ in Fig. 3 is not the current controller output as in Fig. 2 but it is the product of the varying gain $\hat{V}_s/V_d$ and the shifting rectified signal $s(\omega t - \theta)$ from the signal $s(\omega t)$. The control signal $v_{\rm cont}$ and the average duty signal $\overline{d}(t)$ can be expressed in the following two equations:

$$v_{\rm cont}(t) = \frac{\hat{V}_s}{V_d} |\sin(\omega t - \theta)| \quad (7)$$

$$\overline{d}(t) = 1 - \frac{\hat{V}_s}{V_d} |\sin(\omega t - \theta)| \quad (8)$$

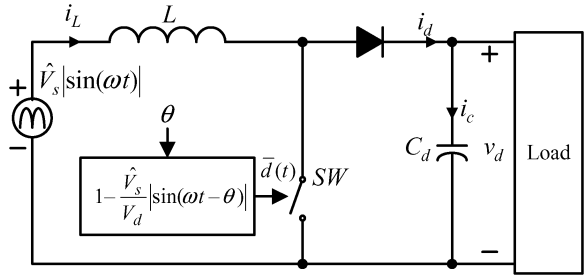

Fig. 4. Boost-type PFC SMR with DPC.

where the maximum duty is 100% and the minimum average duty is dependent on the input voltage amplitude $\hat{V}_s$ and the average output voltage V_d. From (8), we can find that the duty pattern is in fact predefined.

To simply the following analysis, the main circuit topology in Fig. 1 and the proposed DPC in Fig. 3 can be combined and redrawn in Fig. 4 where the diode rectifier is removed. Thus, the input voltage of the boost-type DC/DC converter is represented as an ideal rectified sinusoidal voltage $\hat{V}_s|\sin(\omega t)|$. In the following derivations, we will show that the inductor current will also become rectified sinusoidal waveform by the predefined duty patterns. Therefore, the SMR's current shaping function is achieved.

From the simplified circuit in Fig. 4 and KVL, the following equations can be obtained according to the conduction states of power switch SW:

$$L\frac{di_L(t)}{dt}=\hat{V}_s\left|\sin(\omega t)\right| \qquad \text{when SW is turning on} \quad (9)$$

$$L\frac{di_L(t)}{dt}=\hat{V}_s\left|\sin(\omega t)\right|-V_d \quad \text{when SW is turning off} \quad (10)$$

where the respective turning-on time and turning-off time are $\overline{d}(t)T_s$ and $(1-\overline{d}(t))T_s$, respectively, and T_s is the switching period.

Based on the state-averaging approach, the above two equations (9), (10) can be combined to become the following equation (11) through multiplying them by turning-on time $\overline{d}(t)T_s$ and turning-off time $(1-\overline{d}(t))T_s$, respectively

$$\begin{aligned}L\frac{di_L(t)}{dt}&=\hat{V}_s\left|\sin(\omega t)\right|\overline{d}(t)T_s\\&\quad+\left(\hat{V}_s\left|\sin(\omega t)\right|-V_d\right)\left(1-\overline{d}(t)\right)T_s\\&=\hat{V}_s\left|\sin(\omega t)\right|-\left(1-\overline{d}(t)\right)V_d.\end{aligned} \quad (11)$$

Therefore, by substituting the averaged duty $\overline{d}(t)$ in (8) into (11) and arranging the terms, we can obtain the following time-differential equations for inductor current:

$$L\frac{di_L(t)}{dt}=\hat{V}_s\left|\sin(\omega t)\right|-\hat{V}_s\left|\sin(\omega t-\theta)\right|. \quad (12)$$

The right term $\sin(\omega t-\theta)$ can be extracted by applying the commonly used equation $\sin(A-B)=\sin A\cos B-\sin B\cos A$. If the duty phase signal θ in radians is small and near to zero ($\theta\approx 0$), we can also uses the approximations $\sin\theta\approx\theta$ and $\cos\theta\approx 1$. Then, (12) can be rewritten as

$$\frac{di_L(t)}{dt}\approx\frac{\hat{V}_s\left|\sin(\omega t)\right|}{L}-\frac{\hat{V}_s\left|\sin(\omega t)-\theta\cos(\omega t)\right|}{L}. \quad (13)$$

Since the inductor current is repetitive with double line frequency, the current differential equation at the first cycle ($0\le\omega t<\pi$) can be simplified by removing the absolute operators in (13) and canceling the term $\sin(\omega t)$

$$\frac{di_L(t)}{dt}\approx\frac{\hat{V}_s\theta\cos(\omega t)}{L},\quad 0\le\omega t<\pi \quad (14)$$

Then, by integrating (14), we can obtain the first-cycle inductor current as

$$i_L(t)\approx\frac{\hat{V}_s\theta}{\omega L}\sin(\omega t),\quad \pi>\omega t\ge 0 \quad (15)$$

where the current magnitude is dependent on the controllable duty phase θ. That is, we can write the inductor current $i_L(t)$ in terms of the first-cycle current in (15)

$$i_L(t)\approx\frac{\hat{V}_s\theta}{\omega L}\left|\sin(\omega t)\right|,\quad \omega t\ge 0. \quad (16)$$

Noted that the inductor current waveform becomes the rectified sinusoidal waveform and the current amplitude $\hat{I}_s$ is nearly proportional to the duty phase θ. From the original circuit topology including diode bridge rectifier as shown in Fig. 1, the relation between the input current $i_s(t)$ and inductor current $i_L(t)$ can be expressed as

$$i_s(t)=\begin{cases}i_L(t) & \text{when } v_s\ge 0\\ -i_L(t) & \text{when } v_s<0\end{cases}=\frac{\hat{V}_s\theta}{\omega L}\sin(\omega t)=\hat{I}_s\sin(\omega t). \quad (17)$$

Obviously, the input current $i_s(t)$ possesses the same function $\sin(\omega t)$ as the input voltage v_s. It implies that the desired current-shaping performance including low harmonic current and high power factor can be obtained by tuning the duty phase without current feedback

Additionally, from the input current $i_s(t)$ in (17), the average input power can be represented as

$$\overline{P}_s=\frac{\hat{V}_s^2\theta}{2\omega L}\propto\theta, \quad (18)$$

It is noted the average input power is proportional to the duty phase θ. That is, we are able to regulate the input and output power with unity power factor by tuning the duty phase θ. Therefore, we include a voltage controller in DPC to automatically adjust the suitable duty phase θ to control the flow of input power in order to regulate the output voltage. By replacing current magnitude $\hat{I}_s$ from (16), the output voltage ripple in (6) can be rewritten as

$$v_{d,ac}(t)\approx-\frac{\hat{V}_s^2\theta}{4\omega^2LC_dV_d}\sin(2\omega t). \quad (19)$$

It is noted that the output voltage ripple is also proportional to the duty phase θ.

In power system, the basic circuit of power flow is that two ac voltage sources are interconnected by an inductor as shown

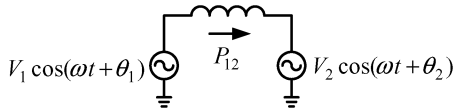

Fig. 5. Basic circuit of power flow in power system.

TABLE I
SIMULATED CIRCUIT PARAMETERS

Input line voltage (peak)	$\hat{V}_s = 170V\ (120V_{rms})$
Input line frequency	$f = 50Hz$
Smoothing capacitance	$C_d = 560\mu F$
Smoothing inductance	$L = 4.65mH$
Equivalent load resistance	$R_{load} = 200\Omega$
Carrier frequency	$f_{tri} = 25kHz$

in Fig. 5. Then, the real power P_{12} and reactive power from the terminal 1 to terminal 2 is

$$P_{12} = \frac{V_1 V_2}{2\omega L}\sin(\theta_1 - \theta_2) \tag{20}$$

$$Q_{12} = \frac{V_1}{2\omega L}\left[V_1 - V_2\cos(\theta_1 - \theta_2)\right]. \tag{21}$$

From (12), the phase shift idea of proposed DPC can be seen as the special case of the above basic circuit where both amplitudes of the two terminal voltages are equal to each other $V_1 = V_2 = \hat{V}_s$ and very little phase difference $\theta_{12} = \theta_1 - \theta_2 \approx 0$ exists between the two terminal voltages. Then, the power flow contains near zero reactive power $Q_{12} \approx 0$ and only real power $P_{12} \approx \hat{V}_s^2\theta_{12}/(2\omega L)$ which can be confirmed by (18).

By adjusting the little phase difference θ through voltage controller, we can regulate the flow of real power and maintain near zero flow of reactive power. Thus, from the point of power flow, the idea of proposed SLCSC is tuning the phase difference θ between the terminal voltages to yield sinusoidal current in phase with the input voltage and regulate the output voltage.

IV. SIMULATED RESULTS

In this section, we begin with a series of computer simulations to demonstrate the proposed DPC. Some nominal values and circuit elements are listed in Table I. It should be noted that no design optimization has been done in order to select the values in Table I. The simple plus-integral (PI) controller is used as the voltage controller in the developed DPC to adjust the duty phase.

Ideal circuit parameters are applied. The simulated waveforms for the condition $V_d^* = 300$ V and $R_{load} = 200\ \Omega$ are plotted in Fig. 6 where the average duty signal $\overline{d}(t)$ and the predefined duty pattern (i.e. zero duty phase $\theta = 0$) are the solid line and the dashed line, respectively, in the upper plots. From the simulated data, the duty phase is kept about 0.014π rads to obtain the desired output voltage v_d shown in the bottom plot. It implies that tuning the duty phase is able to regulate the output voltage.

From the middle plot of Fig. 6, we can find that input current is sinusoidal waveform in phase with the input voltage and therefore, not only the output voltage regulation but also the input current shaping can be achieved by tuning the single duty

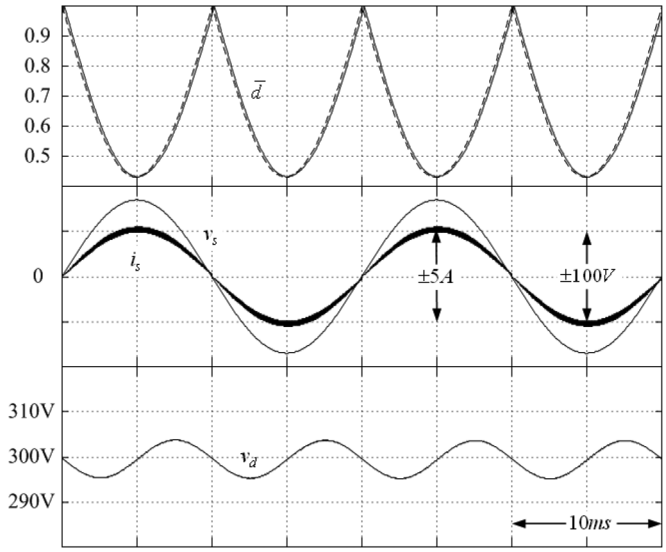

Fig. 6. Simulated waveforms for ideal circuit elements. (Top: average duty signal. Middle: input current and voltage. Bottom: output voltage.)

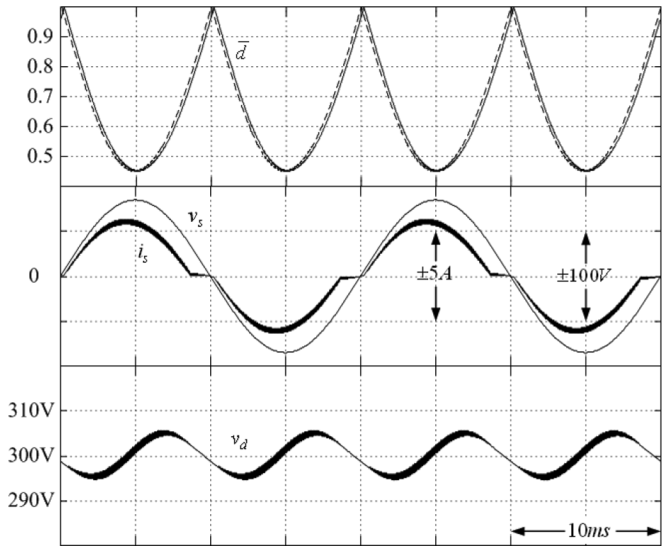

Fig. 7. Simulated waveforms for $R_{load} = 200\ \Omega$ with practical circuit elements. (Top: average duty signal. Middle: input current and voltage. Bottom: output voltage.)

phase. Furthermore, from the key derived equation in (17) and the parameters in Table I, we can calculate and find that the input current peak is about $5.12A$. From observing the simulated current amplitude $5.1A$ in the middle plot of Fig. 6, the key equation in (17) has been demonstrated. However, the above simulated waveforms in Fig. 6 are based on a strong assumption of passive and active circuit components.

In the following simulations, the equivalent resistance of the inductor L and the bulk capacitor C_d and the voltage drops of diodes and the switch are included to further evaluate the effect of practical circuit components on the performance of the proposed DPC. The simulated waveforms for the same condition $V_d^* = 300$ V and $R_{\rm load} = 200\ \Omega$ are plotted in Fig. 7. The average duty signal $\overline{d}(t)$ (solid line) and predefined duty pattern (dashed line) are plotted together in the upper plots for the sake

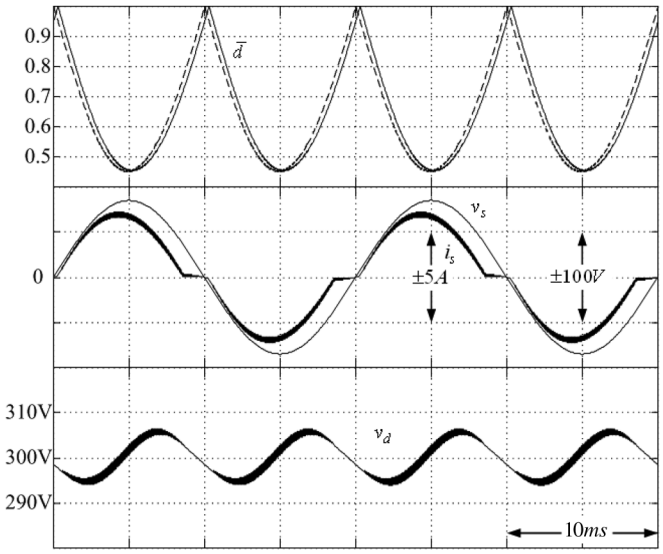

Fig. 8. Simulated waveforms for $R_{load} = 177.78\ \Omega$ with practical circuit elements. (Top: average duty signal. Middle: input current and voltage. Bottom: output voltage.)

of comparison. From the simulated data, the duty phase θ now is increasing to about 0.024π rads to regulate the output voltage found in the bottom plot of the Fig. 7. Thus, using practical circuit elements has no effect on the voltage regulation function of the proposed DPC.

From the middle plot in Fig. 7, we can find that the ideal sinusoidal current waveform in Fig. 6 has been distorted and replaced with the stagnated sinusoidal waveform. It means that practical circuit elements has great effect on the current shaping function of the proposed DPC. Since the current waveform is far from the sinusoidal one, it is reasonable that the plotted duty phase θ increases from 0.014π rads in Fig. 6 to 0.024π rads in Fig. 7 in order to provide larger current magnitude to achieve the desired output voltage. However, from the following experimental results, the harmonic currents of such distorted current waveform are still lower than the limits of standard IEC 61000-3-2.

Then, we increase the load to $R_{load} = 177.78\ \Omega$ with the same voltage command $V_d^* = 300$ V and illustrate the simulated waveform in Fig. 8. In order to yield suitable current amplitude to meet the new load condition, the duty phase is automatically tuned to about $\theta \approx 0.028\pi$ rads through the voltage loop. From (8), all the predefined duty patterns in Fig. 6–8 are the same because of the same input and output voltage level. The only differences between them are their phase which is the main originality of the proposed DPC. In addition, although the current waveforms are not pure sinusoidal ones, the proposed DPC still possess useful input and output performances.

The phenomena of stagnated current can be understood easily from considering the inductor resistance r_L. Therefore, by considering the voltage drop on resistance r_L, the result in (12) can be rewritten as

$$r_L i_L(t) + L\frac{di_L(t)}{dt} = \hat{V}_s\left|\sin(\omega t)\right| - \hat{V}_s\left|\sin(\omega t - \theta)\right|. \quad (22)$$

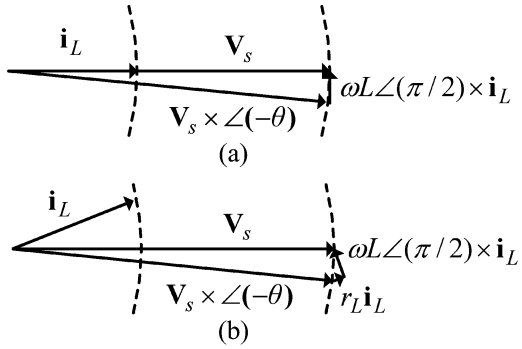

Fig. 9. Phasor diagrams in the case of: (a) pure inductor; (b) practical inductor; and its associated resistance.

In order to illustrate phase shift idea and the effect of inductor resistance r_L on the stagnated current, (12) and (22) in phasor can be plotted in Fig. 9(a) and (b), respectively, where the phase difference θ between $\mathbf{V}_s$ and $\mathbf{V}_s \times \angle(-\theta)$ is near zero.

For the case of ideal inductor shown in Fig. 9(a), the voltage drop on inductor can be approximated to $\mathbf{V_s} - \mathbf{V_s} \times \angle(-\theta) \approx \theta\mathbf{V_s} \times \angle(\pi/2)$ and thus the inductor current $\mathbf{i}_L = (\theta/\omega L)\mathbf{V_s} \times \angle(\pi/2)$ can be seen as being in phase with the rectified voltage $\mathbf{V}_s$.

For the case of pure inductor plus resistance r_L in Fig. 9(b), the sum of voltage drop on them can also be approximated to $\theta\mathbf{V}_s \times \angle(\pi/2)$. But now the inductor current $\mathbf{i}_L$ in phasor can be represented as

$$\mathbf{i}_L = \frac{\theta\mathbf{V}_s\times\angle(\pi/2)}{r_L + j\omega L} = \frac{\theta}{\sqrt{r_L^2+\omega^2L^2}}\mathbf{V}_s\times\angle\alpha \quad \text{where } \alpha = \tan^{-1}\left(\frac{r_L}{\omega L}\right). \quad (23)$$

Since α is always greater than zero, the inductor current $\mathbf{i}_L$ now leads the rectified voltage $\mathbf{V}_s$. It shows that the inductor current waveform $i_L(t)$ must return to zero earlier than the rectified voltage waveform $\hat{V}_s|\sin(\omega t)|$. Because the inductor current in boost-type SMR can not be negative, the inductor current waveform $i_L(t)$ must keep zero until the next half line cycle. Obviously, the practical inductor resistance result in the stagnated current.

V. Experimental Results

The proposed DPC has been digitally implemented in a DSP-based system using TMS320F240 where a simple and popular PI-type voltage loop is used in order to focus on the performance of tuning duty phase. Only input voltage and output voltages are sensed where the former provides the phase information of input voltage and the latter helps to regulate the output voltage. It is noted that the digital resolution of duty phase is the main challenge in the implementation of the proposed DPC. Too small phase resolution would result in the instable operation of SMRs in shaping current waveform. In my experiment, the phase resolution is set to 25 000 per cycle of line voltage. All the circuit parameters in the experimental system have been listed in Table I.

Fig. 10 shows the measured waveforms for the condition $V^* = 300$ V and $P_s \approx 520$ W ($R_L = 177.78\ \Omega$). The top plot shows the output voltage waveform varying around the desired

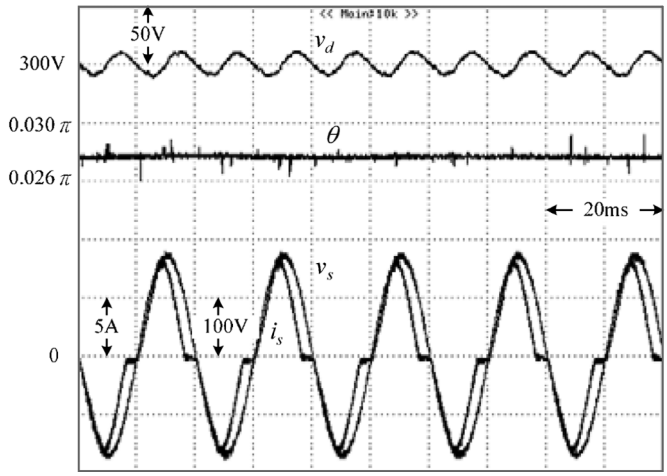

Fig. 10. Measured waveforms at $P_s = 520$ W. (Top: output voltage. Middle: duty phase. Bottom: input current and voltage.)

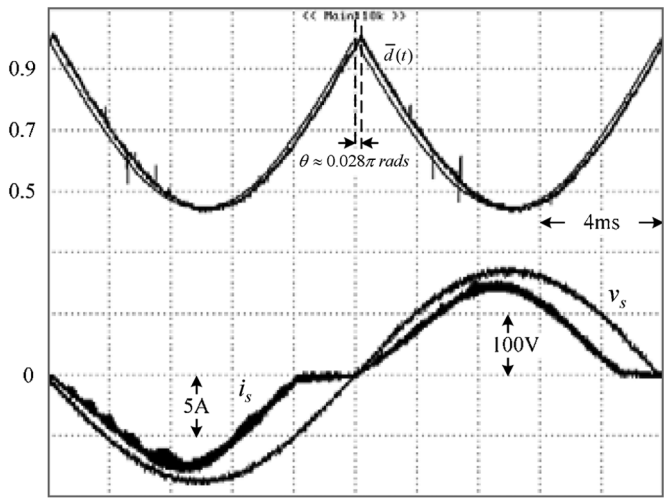

Fig. 11. Measured waveforms at $P_s = 520$ W. (Top: average duty signal. Bottom: input current and voltage.)

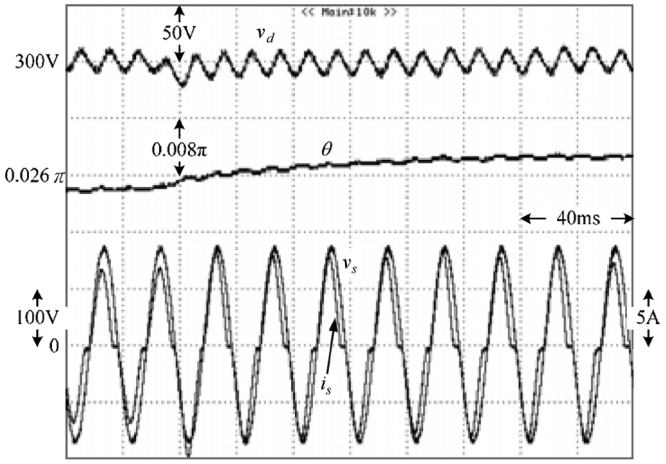

Fig. 12. Measured waveforms during the load resistance change from $R_L = 200\ \Omega$ to $R_L = 177.78\ \Omega$. (Top: output voltage. Middle: duty phase. Bottom: input current and voltage.)

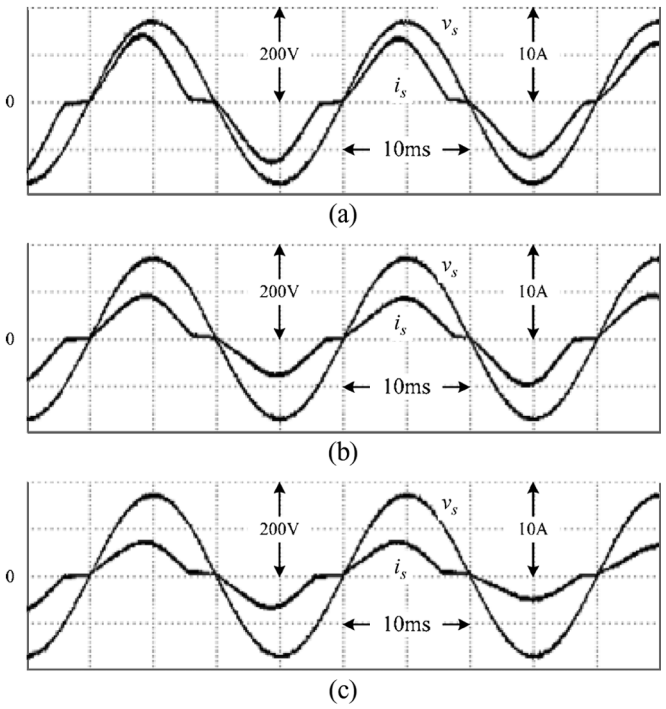

Fig. 13. Measured input current waveforms for: (a) $R_L = 200\ \Omega$; (b) $R_L = 300\ \Omega$; and (c) $_L = 400\ \Omega$.

voltage level. The duty phase signal shown in the middle plot is fixed around 0.028π rads in order to stably yield the input current shown in the bottom plot. From the bottom plots of input current and voltage, we can find that the actual current waveform is very close to the simulated one in Fig. 8 and the measured power factor now is 0.944. Obviously, input power quality has been improved and the proposed DPC has been demonstrated.

In Fig. 11, the average duty phase signal $\overline{d}(t)$ is shown and the predefined pattern signal is also plotted for comparison. We can find that the little phase difference between the top plots contributes to draw the stagnated current waveform similar to the simulated current waveform shown in Fig. 8.

To evaluate the influence of the transient disturbance in the proposed sensorless DPC, the measured waveforms during the load resistance change from $R_L = 200\ \Omega$ ($P_s = 456$ W) to $R_L = 177.78\ \Omega$ ($P_s \approx 520$ W) are plotted in Fig. 12. From Fig. 12, we can find that there is obvious voltage dip in the output voltage v_d due to load change and then, the voltage controller regulates the output voltage to the voltage command $V^* = 300$ V by increasing the duty phase signal θ. It shows that the transient operation during load change is stable.

In addition, the input current waveforms under $R_L = 200\ \Omega$, $R_L = 300\ \Omega$, and $R_L = 400\ \Omega$ are plotted in Fig. 13(a)–(c), respectively. In addition, by using digital power meter YOGOGAWA WT210, the measured power factor (PF), the total current harmonic distortion (THD_i) under various load are listed in Table II. The input currents in Fig. 13 under various R_L are close to each other except for the magnitude. It follows that in Table II, the measured PF and THD_i under various R_L have the like values. However, owing to the limitation of digital resolution of phase θ, it is hard to regulate the output voltage

TABLE II
MEASURED DATA UNDER SINUSOIDAL VOLTAGE FOR VARIOUS LOAD RESISTANCE

R_{load} (Ω)	P_s (W)	THD_i (%)	PF
177.78	520	23.22	0.944
200	450	22.56	0.947
300	303	22.51	0.942
400	241	22.37	0.941

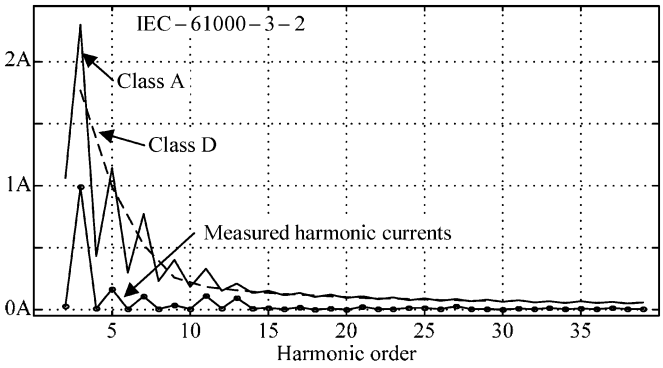

Fig. 14. Measured harmonic currents under $R_L = 177.78\ \Omega$ ($P_s = 520$ W) and the limits of IEC-61000-3-2 standard.

TABLE III
HARMONIC CURRENTS

Harmonic order	IEC-61000-3-2 Standard		R_L=177.78Ω P_s=520W
	Class A	Class D	
2	1.080 A_{rms}	##	0.0254 A_{rms}
3	2.300 A_{rms}	1.768 A_{rms}	0.9918 A_{rms}
4	0.430 A_{rms}	##	0.0102 A_{rms}
5	1.140 A_{rms}	0.988 A_{rms}	0.1642 A_{rms}
6	0.300 A_{rms}	##	0.0033 A_{rms}
7	0.770 A_{rms}	0.520 A_{rms}	0.1043 A_{rms}
8	0.230 A_{rms}	##	0.0040 A_{rms}
9	0.400 A_{rms}	0.260 A_{rms}	0.0364 A_{rms}
10	0.184 A_{rms}	##	0.0032 A_{rms}
11	0.330 A_{rms}	0.182 A_{rms}	0.1118 A_{rms}
12	0.153 A_{rms}	##	0.0087 A_{rms}
13	0.210 A_{rms}	0.154 A_{rms}	0.0930 A_{rms}
14	0.131 A_{rms}	##	0.0065 A_{rms}
15	0.150 A_{rms}	0.133 A_{rms}	0.0140 A_{rms}
16	0.115 A_{rms}	##	0.0023 A_{rms}
17	0.132 A_{rms}	0.118 A_{rms}	0.0175 A_{rms}
18	0.102 A_{rms}	##	0.0002 A_{rms}
19	0.118 A_{rms}	0.105 A_{rms}	0.0094 A_{rms}
20	0.092 A_{rms}	##	0.0009 A_{rms}
21	0.107 A_{rms}	0.095 A_{rms}	0.0210 A_{rms}
22	0.084 A_{rms}	##	0.0028 A_{rms}
23	0.098 A_{rms}	0.087 A_{rms}	0.0046 A_{rms}
24	0.077 A_{rms}	##	0.0115 A_{rms}
25	0.090 A_{rms}	0.081 A_{rms}	0.0109 A_{rms}
26	0.071 A_{rms}	##	0.0014 A_{rms}
27	0.083 A_{rms}	0.074 A_{rms}	0.0260 A_{rms}
28	0.066 A_{rms}	##	0.0030 A_{rms}
29	0.078 A_{rms}	0.069 A_{rms}	0.0046 A_{rms}
30	0.061 A_{rms}	##	0.0005 A_{rms}

under light load by DPC. Therefore, no experimental data under lighter load ($R_L > 400\ \Omega$) can be provided in this paper.

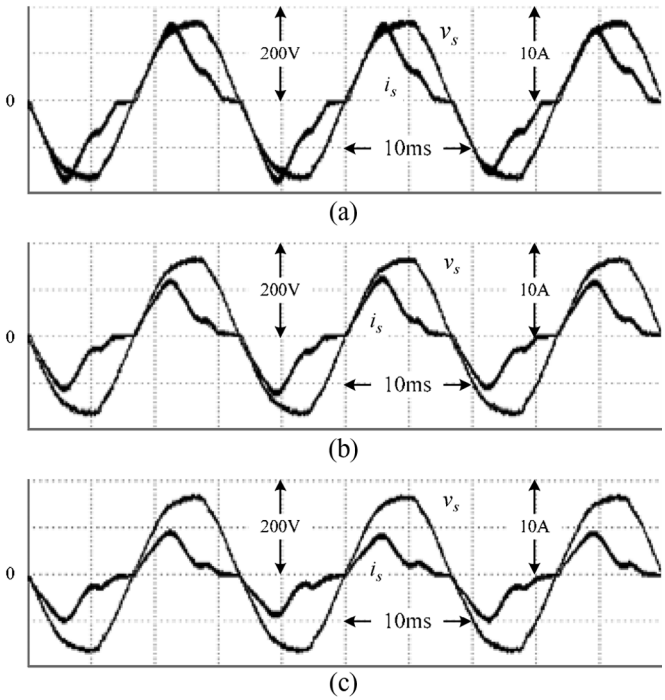

Fig. 15. Measured input current waveforms with distorted input voltage (60 Hz) for: (a) $R_L = 200\ \Omega$; (b) $R_L = 300\ \Omega$; and (c) $R_L = 400\ \Omega$.

TABLE IV
MEASURED DATA UNDER DISTORTED VOLTAGE FOR VARIOUS LOAD RESISTANCE

R_{load} (Ω)	P_s (W)	THD_i (%)	PF	THD_v(%)
200	462	29.29	0.884	4.10
300	307	30.42	0.841	4.02
400	241	33.41	0.819	3.77

The measured harmonic currents under $R_L = 177.78\ \Omega$ are plotted in Fig. 14, and tabulated in Table III where the limits of IEC-61000-3-2 class A and class D are also provided for the sake of comparison. From Fig. 14 and Table III, we can find that the delivered input harmonic currents by the proposed DPC are well below the limits of IEC-61000-3-2 standard even though no current control loop is included in the proposed DPC. This illustrates the advantages of the developed control technique—the proposed DPC is very simple as it avoids inner current loop, and the technique is robust as it has an inherent ability to shape current waveform in CCM.

To understand the performance of proposed DPC under the distorted input voltage (60 Hz), some measured waveforms for various load resistances are shown in Fig. 15(a)–(c), respectively. The measured total harmonic voltage distortion THD_v, THD_i and PF are tabulated in Table IV. Due to the distorted input voltage, the measured THD_i are higher than those in Table II. However, from the experimental data, the proposed DPC also can operate normally to obtain PFC function under distorted input voltage.

VI. CONCLUSION

A new DPC for boost-type SMRs has been developed and implemented in this paper. The control structure is single-loop with

only voltage loop. By sensing the input and output voltage, we can obtain predefined duty pattern, and then, adjust it according to the output phase signal from the voltage loop. From the simulated and experimental results, the proposed DPC can regulate the output voltage and meet the requirements of IEC-61000-3-2 standard even though the input current returns zero ahead of the end of half cycle and keep zero current until the next half cycle.

Due to the stagnated current, the input quality of the proposed DPC is not as good as the conventional multiloop controlled PFC. However, the proposed scheme can operate without current feedback and A/D conversion, and the idea of tuning the phase difference between terminal voltages is not sensitive to parameter accuracy. Therefore, the proposed DPC has the high potential for the implementation of mixed-mode PFC ICs.

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