Analysis and Modeling of On-Chip Charge Pump Designs Based on Pumping Gain Increase Circuits With a Resistive Load

Chih-Huei Hu, *Student Member, IEEE*, and Lon-Kou Chang, *Member, IEEE*

***Abstract*—A complete equivalent model and analysis of high-efficiency charge-pump gain-increase (PGI) circuits with resistive loads are proposed. Based on this simple analytical model, the characteristics of PGI circuits can be approximately predicted and several handy equations, which are useful for pencil-and-paper design, can also be found for planning the desired circuit to achieve good enough performance with an acceptable accuracy tolerance in the steady state. In addition, an optimized design method for PGI circuits with resistive loads is developed in terms of the total number of gain stages in the design and the ratio between pump capacitors. For 1.5 V supply voltage operation, reliability and accuracy are demonstrated by comparisons between SPICE simulations of the PGI circuit and the results from the equivalent model. The model also has been validated by means of measurements taken from a test chip and typically shows relative open-loop output voltage errors lower than 8%. Finally, although the derivation of the model was based on a PGI circuit, it is shown that the design strategy can also be applied to other charge pump designs that have no voltage drop between the inner stages and the output stage.**

***Index Terms*—Charge pump, dc–dc converter, equivalent model, high-voltage generator, voltage multiplier.**

I. Introduction

In modern mixed-mode circuit designs, low-voltage and small-size dc–dc converters have been extensively required. Charge pump circuits (CPCs) can provide the solutions necessary to meet these demands to convert an input voltage upward to a higher one with either a positive or a reverse polarity. Since CPCs use capacitors as energy storage devices instead of magnetic components, the converter has no electromagnetic interference (EMI) problems. For low-power designs, the capacitors required by CPCs can be small enough to be fabricated in integrated circuits.

CPCs have been widely used in nonvolatile memories for many years, such as EEPROM and Flash memories [1]–[4]. More and more applications of CPCs can be found in power integrated circuits (ICs), low-supply-voltage switched-capacitor systems, continuous time filters [5], adaptive voltage-scaling power management [6], and so on. Most of the conventional CPCs are based on the circuit proposed by Dickson [7] as shown in Fig. 1(a). It uses diode-connected transistors as charge-transfer devices. Neglecting the body effect and using the steady-state analysis from the simple model of the Dickson charge pump [7]–[9], the voltage increment, ΔV_b, in each stage associated with the voltage division resulting from a clock-coupling capacitance C and a stray capacitance C_s can be expressed as

$$\Delta V_b = \left(\frac{C}{C+C_s}\right)\cdot V_{\rm clk} - \frac{I_{\rm out}}{f\cdot(C+C_s)} - V_d \qquad (1)$$

where $V_{\rm clk}$ is the pumping clock amplitude, f is the clock frequency, $I_{\rm out}$ is the output current, and V_d is the voltage drop across each MOS diode. In (1), the first term is the common expression for the voltage increase occurring at each pumping node contributed by the clock source, clk or $\overline{\rm clk}$, through the associated capacitor C. The second term is the voltage drop due to $I_{\rm out}$. In each stage, the necessary condition for the boost function of the CPC is that ΔV_b must be larger than zero. With the condition that V_d and ΔV_b are constants, the final output voltage in an N-stage CPC with a resistive load can be obtained as

$$V_{\rm out} = (V_{\rm in} - V_d) + N\cdot\Delta V_b \qquad (2)$$

where $V_{\rm in}$ is the input voltage. From (1) and (2), an extremely simple equivalent circuit for the Dickson charge pump is shown in Fig. 1(b) and the output voltage can be derived as

$$V_{\rm out} = V_{\rm eq} - R_{\rm eq}\cdot I_{\rm out} \qquad (3)$$

where $V_{\rm eq} = V_{\rm in} - V_d + N\cdot[(C/(C+C_s))\cdot V_{\rm clk} - V_d]$ and $R_{\rm eq} = N/(f\cdot(C+C_s))$. In (3), $V_{\rm eq}$ and $R_{\rm eq}$ are the equivalent open-circuit output voltage and the equivalent output series resistance, respectively.

However, ΔV_b is not a constant because V_d is enlarged by the body effect, which increases as more pump stages are used. The body effect increases the threshold voltage, $V_{\rm tn}$, and results in the degradation of ΔV_b. Thus, the pumping efficiency of the succeeding stage will be less than that of the forestages. When ΔV_b in the last stage reduces to zero, $V_{\rm out}$ will start to saturate even if more cascaded pump stages are added. Another voltage drop problem exists at the output stage, because the most serious body effect occurs on M_{DO} due to a large build up of V_{sb}. The loss of pumping gain also results in an increased power loss. This low efficiency restricts the application of the Dickson charge pump structure to low-supply voltage dc–dc converters.

In recent years, much effort has been made in the analysis and optimization of the Dickson structure [10], [11], and many approaches for improving the pumping efficiency have focused on solving the threshold voltage augmentation problem [12]–[16]. Some of them offer a high pumping gain in the inner stage and a very low voltage drop at the output stage. Thus, the voltage gain of these circuits can be maintained to keep the output voltage proportional to the number of pump stages. In this article, in

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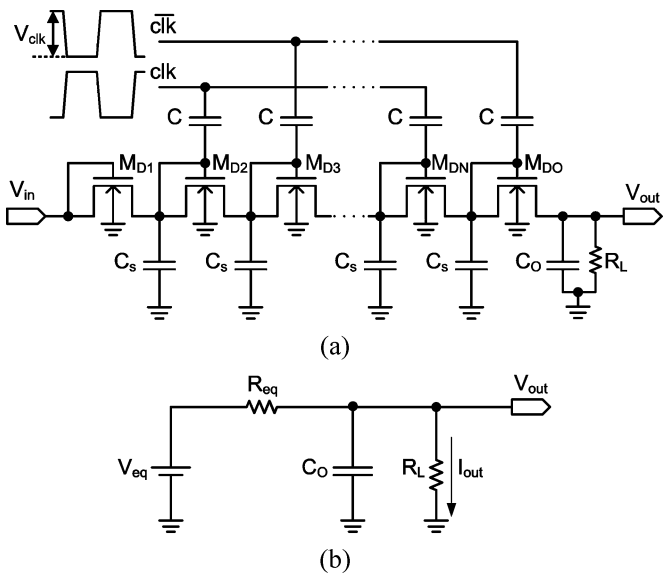

Fig. 1. (a) Dickson charge pump circuit. (b) Equivalent model of the Dickson charge pump.

order to support a convenient and rapid design scheme, a thorough analysis and a complete model of the pumping gain increase (PGI) circuit [16], which is a type of improved CPC, has been presented. In Section II, a general model based on PGI circuits is described. Analyses based on the charge balance and average conceptions are presented. By using this simple analytical model, characterization of PGI circuits can be performed in a pencil-and-paper manner and the output behavior can be approximately predicted. An optimization design method for minimizing the die area of an N-stage PGI circuit in terms of the total number of pump stages and the pump capacitors ratio is also presented. This design strategy can also be applied to other improved CPC designs that have no voltage drop between inner stages and the output stage. In Section III, simulation results are presented to verify this equivalent model for designing PGI circuits. In Section IV, experimental results measured from a test chip that was fabricated with a TSMC 0.35-μm mixed-mode technology demonstrate the validity of the proposed model. Conclusions are given in Section V.

II. Equivalent Model for the Voltage Multiplier

PGI circuits provide a method of using NMOS and PMOS charge transfer switches (CTSs) to eliminate the voltage drop, V_d, across each pump stage and allow the output voltage to increase linearly as the cascade number of the pump stage increases. The schematic diagrams of one-stage PGI circuits, which approximately double their supply voltage, are shown in Fig. 2. It is notable that in PGI-3, there is no output saturation limitation, no matter how many pump stages are used. Ignoring non-ideal characteristics such as switching losses and parasitic capacitances, an analytically ideal model can be constructed based on the identity of an N-stage PGI circuit.

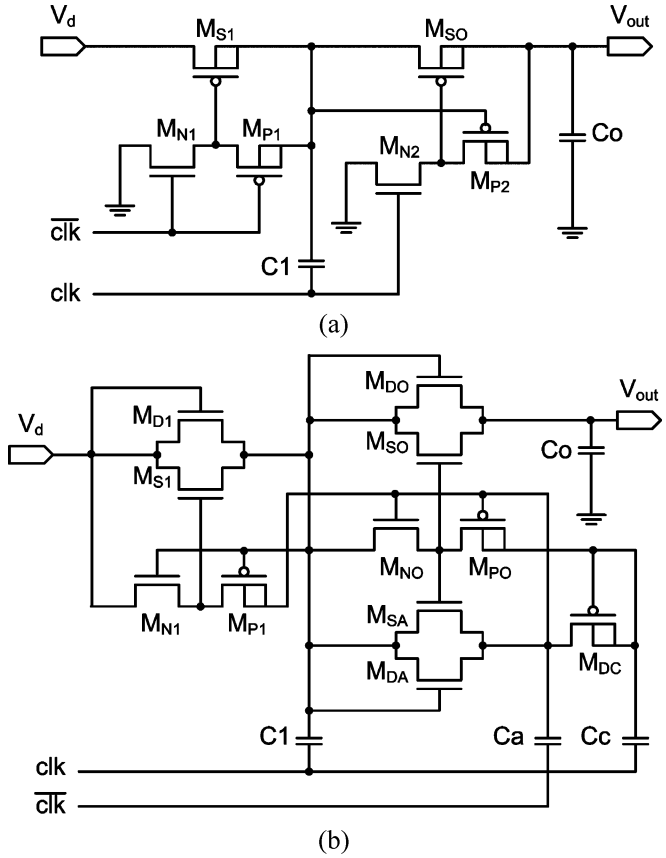

Fig. 2. Voltage doubling PGI circuits. (a) PGI-3 circuit. (b) PGI-1 circuit [16].

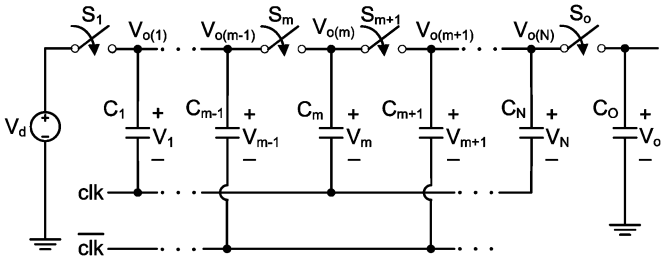

Fig. 3. Conceptual diagram of an N-stage PGI circuit.

A. Behavioral Model of Intermediate Stages

From the characteristics of an N-stage PGI circuit, the equivalent circuit can be simplified as shown in Fig. 3, where clk and $\overline{\text{clk}}$ are two anti-phase clocks with the same amplitude, V_s, C_m is the pump capacitor of the mth pump stage, V_m is a time-variant voltage across C_m, $V_{o(m)}$ is the voltage at node m connecting to the positive branch of C_m, and S_m is the mth equivalent ideal transfer switch between C_{m-1} and C_m. Each stage has two operating modes, the charging mode operating with DT_s duration and the discharging mode with $(1-D)T_s$ duration, where D is the duty ratio and T_s is the switching period. The corresponding waveforms of $V_{o(m-1)}$, $V_{o(m)}$, and $V_{o(m+1)}$ are shown in Fig. 4.

In order to find a general model, the charge balance and the average of V_m are used to calculate the transfer charge and the average current between pump capacitors. In Fig. 4, V_m increases from the lowest level, $V_{m,L}$, to the highest level, $V_{m,H}$, in the charging mode of C_m and decreases back to $V_{m,L}$ in the

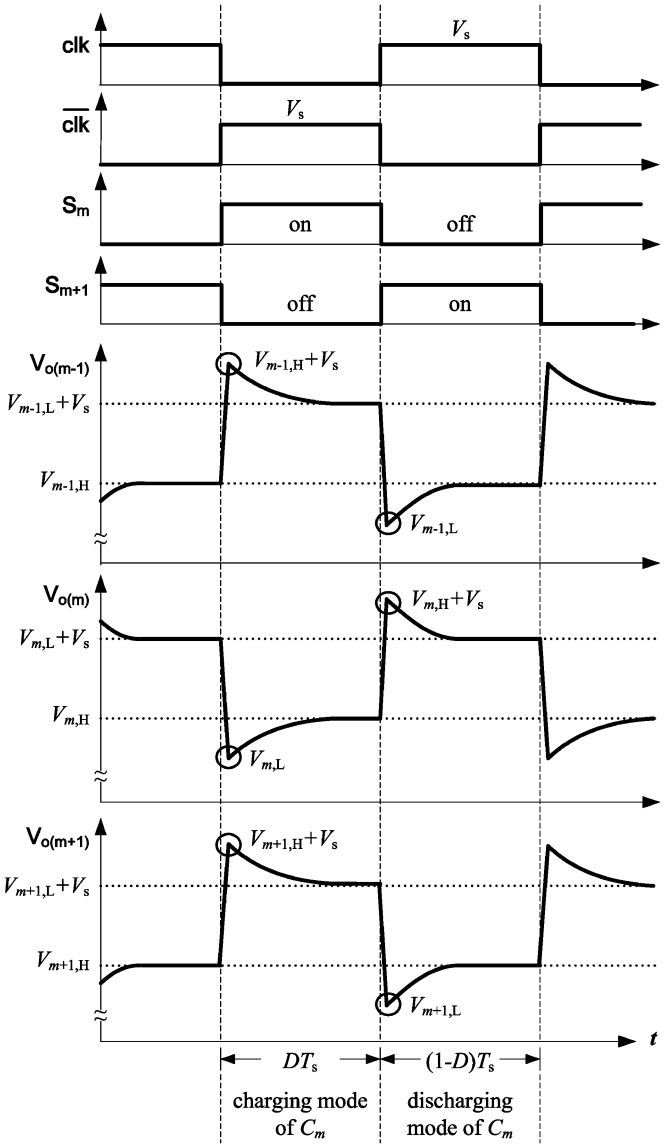

Fig. 4. Clock signal, states of switches, and the steady-state waveforms of $V_{o(m-1)}$, $V_{o(m)}$, and $V_{o(m+1)}$.

discharging mode. Let $V_{m,\text{avg}}$ denote the arithmetic average of $V_{m,L}$ and $V_{m,H}$ and be given as

$$V_{m,\text{avg}} = (V_{m,H} + V_{m,L})/2. \tag{4}$$

Similar notations are also applied to all the voltages across the pump capacitors. From Fig. 4, in time DT_s, $V_{o(m-1)}$ is raised by $\overline{\text{clk}}$, and part of the charge ΔQ_m stored in C_{m-1} will transfer to C_m. Thus, V_m will increase from $V_{m,L}$ to $V_{m,H}$, and V_{m-1} will decrease from $V_{m-1,H}$ to $V_{m-1,L}$. By using charge conservation, ΔQ_m can be expressed as

$$\Delta Q_m = C_{m-1}\times(V_{m-1,H}-V_{m-1,L}) = C_m\times(V_{m,H}-V_{m,L}). \tag{5}$$

If DT_s is sufficiently large to complete the charge transfer in time, the following expressions can be obtained:

$$V_s + V_{m-1,L} = V_{m,H} \tag{6}$$

or

$$V_s + V_{m-1,H} - \Delta V_{m-1} = V_{m,L} + \Delta V_{m,\text{charge}} \tag{7}$$

where $\Delta V_{m-1} = V_{m-1,H} - V_{m-1,L}$, and $\Delta V_{m,\text{charge}} = V_{m,H} - V_{m,L}$. From (4)–(7), the transferred charge ΔQ_m can be obtained as

$$\Delta Q_m = \frac{C_{m-1}\times C_m}{C_{m-1}+C_m}\cdot 2(V_s + V_{m-1,\text{avg}} - V_{m,\text{avg}}). \tag{8}$$

From (8), the average charging current $I_{m,\text{avg}}$ of C_m can be found by

$$I_{m,\text{avg}} = \frac{\Delta Q_m}{T_s} = \frac{C_{m-1}\times C_m}{C_{m-1}+C_m}\cdot\frac{2}{T_s}(V_s + V_{m-1,\text{avg}} - V_{m,\text{avg}}). \tag{9}$$

Equation (9) shows that $I_{m,\text{avg}}$ is a linear function of the difference between $(V_s + V_{m-1,\text{avg}})$ and $V_{m,\text{avg}}$. From (9), the equivalent resistance between the nodes $(m-1)$ and m can be obtained as

$$R_m \equiv \frac{T_s}{2C_{m-1}\times C_m/(C_{m-1}+C_m)}. \tag{10}$$

The pumping operation between C_m and C_{m+1} behaves in a similar manner as the operation between C_{m-1} and C_m, except that clk changes to high and $\overline{\text{clk}}$ changes to low. Therefore, in a $(1-D)T_s$ duration, the average discharging current $I_{m+1,\text{avg}}$ of C_m and the equivalent resistance between nodes m and $(m+1)$ are given as

$$\begin{aligned} I_{m+1,\text{avg}} &= \frac{\Delta Q_{m+1}}{T_s} \\ &= \frac{C_m\times C_{m+1}}{C_m+C_{m+1}} \\ &\quad\cdot\frac{2}{T_s}(V_s + V_{m,\text{avg}} - V_{m+1,\text{avg}}) \end{aligned} \tag{11}$$

$$\text{and}\quad R_{m+1} \equiv \frac{T_s}{2C_m\times C_{m+1}/(C_m+C_{m+1})}. \tag{12}$$

Since (9)–(12) shows a simple and regular modular structure, the equivalent model of each intermediate stage of PGI circuits can be deduced as the mth pump stage model shown in Fig. 5.

B. Behavioral Model of the Input Stage

In the first stage, since C_1 is connected to a voltage source V_d, the average voltage of V_1 can be given as

$$V_{1,\text{avg}} = (V_d + V_{1,L})/2. \tag{13}$$

In the charging mode of C_1, V_1 increases from the lowest level $V_{1,L}$ to V_d. From (13), the transferred charge ΔQ_1 can be expressed by $V_{1,\text{avg}}$ and V_d. The corresponding average charging current $I_{1,\text{avg}}$ of C_1 and the resultant equivalent resistor R_1 are given as

$$I_{1,\text{avg}} = \frac{\Delta Q_1}{T_s} = \frac{2C_1}{T_s}(V_d - V_{1,\text{avg}}) = \frac{V_d - V_{1,\text{avg}}}{R_1} \tag{14}$$

and

$$R_1 \equiv \frac{T_s}{2C_1}. \tag{15}$$

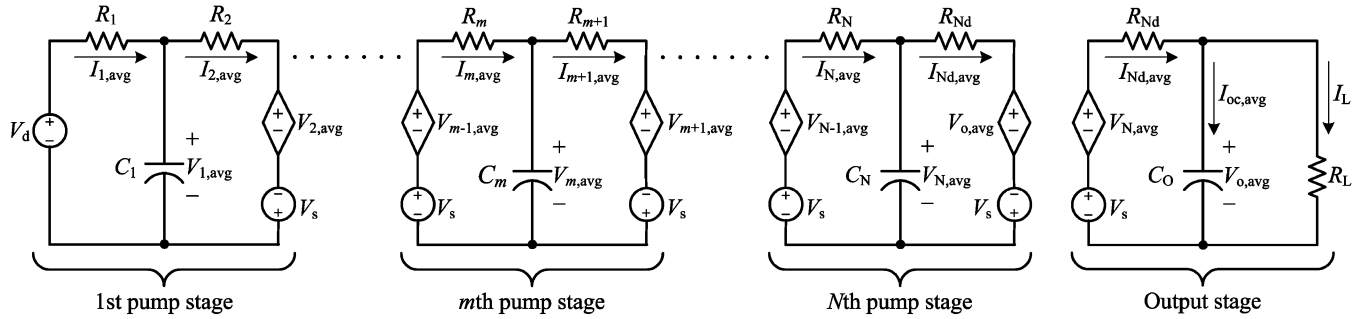

Fig. 5. Equivalent model for an N-stage PGI circuit.

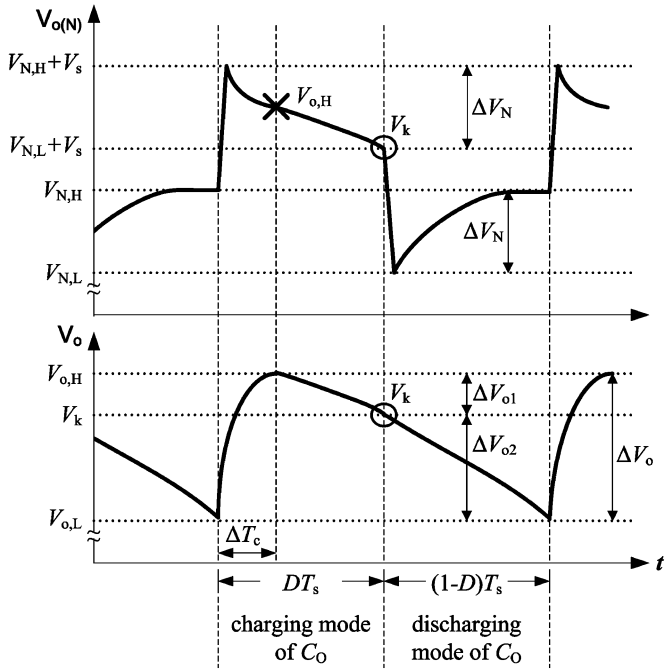

Fig. 6. Steady-state waveforms of $V_{o(N)}$ and V_o.

The operation of C_1 in its discharging mode is the same as that of the inner pump capacitor. Thus, employing (11)–(15), the equivalent model of the first pump stage in the PGI circuit can be depicted as shown in Fig. 5.

C. Behavioral Model of the Output Stage

The load can be generally represented by a resistor, R_L, connected in parallel to the output capacitor, C_O. Thus, the behavior of the charge transmitted to R_L during each cycle period must be included in the model operation. According to Fig. 3, the waveforms of $V_{o(N)}$ and the output voltage, V_o, are given in Fig. 6. In the charging period DT_s of C_O, S_o is turned on and the charge is quickly delivered from C_N to C_O in a very short period, ΔT_c. This causes V_o to increase from $V_{o,L}$ to $V_{o,H}$. After ΔT_c, C_N and C_O discharge through R_L as a parallel capacitance $C_N \| C_O$. At the end of the DT_s, both V_o and $V_{o(N)}$ will decrease from their high level to a voltage V_k as follows:

$$V_k = V_{o,H} - \Delta V_{o1} = V_{o,L} + \Delta V_{o2} = V_{N,H} + V_s - \Delta V_N, \quad (16)$$

where $\Delta V_N = V_{N,H} - V_{N,L}$, and ΔV_{o1} and ΔV_{o2} are the voltage drop values in the periods of $(DT_s - \Delta T_c)$ and $(1 - D)T_s$, as shown in Fig. 6. When the discharging period $(1 - D)T_s$ of C_O starts, S_o is turned off and the consumed charge of R_L is provided only by C_O. By employing the average definition of $V_{o,\mathrm{avg}}$ as (6) in a cycle time, ΔV_{o1} and ΔV_{o2} can be derived as

$$\Delta V_{o1} = \frac{C_O \cdot D}{C_N(1-D) + C_O} \cdot \Delta V_o \quad (17a)$$

$$\text{and} \quad \Delta V_{o2} = \frac{(C_O + C_N)(1-D)}{C_N(1-D) + C_O} \cdot \Delta V_o \quad (17b)$$

where $\Delta T_c \ll DT_s$ and $\Delta V_o = V_{o,H} - V_{o,L}$. From (17), ΔV_{o1} is smaller than ΔV_{o2} because ΔV_{o1} is produced from the discharge of $C_N \| C_O$ and ΔV_{o2} is produced only from the discharge of C_O.

Employing (16), (17), and the charge conservation within C_N, C_O, and R_L, the voltage variations ΔV_N, ΔV_o, ΔV_{o1}, and ΔV_{o2} can be found. Using these voltage variations to derive the charge transfer rate, the average discharging current $I_{Nd,\mathrm{avg}}$ of C_N corresponding to $\Delta Q_{N,d}$, which is the charge delivered from C_N to C_O, can be simply obtained as

$$I_{Nd,\mathrm{avg}} = \frac{2}{T_s} \cdot \frac{C_N C_O (C_N + C_O)(1-D)}{(C_N + C_O)^2(1-D) - C_N C_O D} \times (V_s + V_{\mathrm{N,avg}} - V_{o,\mathrm{avg}}) + \frac{C_N^2(1-D) + C_N C_O (1-2D)}{(C_N + C_O)^2(1-D) - C_N C_O D} \cdot \frac{V_{o,\mathrm{avg}}}{R_L} \cdot D. \quad (18)$$

Comparing (18) with (11), $I_{Nd,\mathrm{avg}}$ is different from all the average discharging currents of the inner pump stages. Similarly to (18), the average charging current $I_{\mathrm{oc,avg}}$ of C_O can be derived as

$$I_{\mathrm{oc,avg}} = \frac{2}{T_s} \cdot \frac{C_N C_O (C_N + C_O)(1-D)}{(C_N + C_O)^2(1-D) - C_N C_O D} \times (V_s + V_{\mathrm{N,avg}} - V_{o,\mathrm{avg}}) - \frac{C_O (C_N + C_O)(1-D)}{(C_N + C_O)^2(1-D) - C_N C_O D} \cdot \frac{V_{o,\mathrm{avg}}}{R_L} \cdot D. \quad (19)$$

The equivalent circuit model provided by (18) and (19) can be simplified greatly if ΔV_{o1} is equal to ΔV_{o2}. This condition can be met by choosing C_N and C_O such that

$$\frac{D}{1-D} = \frac{C_N + C_O}{C_O}. \quad (20)$$

The substitution of (20) into (18) and (19) yields

$$I_{Nd,\text{avg}} = \frac{2C_N}{T_s}(V_s + V_{\text{N,avg}} - V_{o,\text{avg}}) \tag{21}$$

$$I_{\text{oc,avg}} = \frac{2C_N}{T_s}(V_s + V_{\text{N,avg}} - V_{o,\text{avg}}) - \frac{V_{o,\text{avg}}}{R_L}D. \tag{22}$$

From (21), the equivalent discharging resistance R_{Nd} of C_N is obtained as

$$R_{Nd} = \frac{T_s}{2C_N}. \tag{23}$$

By using (21)–(23), the equivalent model of the last pump stage and the output stage can be obtained as shown in Fig. 5. In the complete circuit model, all labeled voltages are averages and each dependent voltage source is controlled by its corresponding voltage across a capacitor. Based on this regular and simplified model, the behavior of a multistage PGI circuit with a resistive load can be easily controlled and designed.

D. Results Obtained From Equivalent Model

In Fig. 5, all capacitors can be considered open when the PGI circuit reaches the steady state. Although the model of each stage contains four voltage sources, for an N-stage PGI circuit, the average output $V_{o,\text{avg}}$ can be found and expressed simply by

$$V_{o,\text{avg}} = \frac{R_L}{\left(\sum_{m=1}^{N} R_m\right) + R_{Nd} + R_L}(V_d + N \cdot V_s). \tag{24}$$

Replacing R_L by an approximate value of $(V_{o,\text{avg}} \times T_s)/(C_O \times \Delta V_o)$, (24) can be rewritten as

$$V_{o,\text{avg}} = \frac{V_d + NV_s}{\left[1 + \frac{T_s}{R_L}\left(\sum_{m=1}^{N} \frac{1}{C_m}\right)\right]} = \frac{V_d + NV_s}{\left[1 + \frac{T_s}{R_L C_{\text{series}}}\right]}, \tag{25}$$

where C_{series} represents the total capacitance of all the pump capacitances connected in series. The result expressed by (25) shows that $V_{o,\text{avg}}$ is determined by the ratio of T_s to the constant $R_L \times C_{\text{series}}$. Thus, if the time constant $R_L \times C_{\text{series}}$ is smaller than T_s, $V_{o,\text{avg}}$ can be effectively regulated by tuning the switching period T_s. From (25) an alternative expression of $V_{o,\text{avg}}$ in terms of the load current I_L can be obtained as

$$V_{o,\text{avg}} = (V_d + NV_s) - \frac{T_s}{C_{\text{series}}} \times I_L. \tag{26}$$

In (26), the highest ideal output voltage $(V_d + NV_s)$ will occur with the condition of $I_L = 0$. As the load current increases, the output voltage will decrease at a rate of (T_s/C_{series}) [17]. Moreover, if pump capacitors are all the same value, it can be seen that the derived result (26) would match Dickson's result (3) with $C_s = 0$ and $V_d = 0$. This comparison proves that the proposed model deduced from PGI circuits is an ideal case of the Dickson structure. Consequently, even though the model and the derivation were based on PGI circuits, the same design strategy can be applied, as an ideal case, to any charge-pump design which is able to eliminate voltage drop between the inner stages and the output stage.

Considering chip size and therefore cost, decreasing the sum of pump capacitances C_{TP} will greatly decrease the die area.

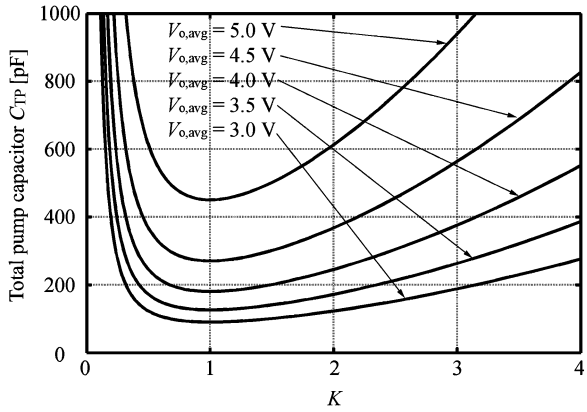

Fig. 7. Total pump capacitances C_{TP} calculated from the three-stage model versus the value of K under various desired $V_{o,\text{avg}}$, where $V_d = V_s = 1.5$ V, $R_L = 100$ kΩ, and $f_s = 1$ MHz.

Assuming that the pump capacitances are designed proportionally as $C_{m-1}/C_m = K$, where K is a regulative constant, C_{TP} of an N-stage PGI circuit can be obtained from (25) and expressed as

$$C_{\text{TP}} = \sum_{m=1}^{N} C_m = \sum_{m=1}^{N} K^{(N-m)} \times C_N = \frac{\left(\sum_{i=1}^{N} K^{(i-1)}\right)^2 V_{o,\text{avg}} \cdot T_s}{K^{(N-1)}\left[(V_d + NV_s) - V_{o,\text{avg}}\right] R_L}. \tag{27}$$

From (27), the minimum C_{TP} can be found by making $dC_{\text{TP}}/dK = 0$. This derivation has a reasonable solution which is $K = 1$. Thus, the minimum value of each pump capacitance referred as $C_{m,\min}$ is given by

$$C_{m,\min} = \frac{N \cdot V_{o,\text{avg}} \cdot T_s}{\left[(V_d + NV_s) - V_{o,\text{avg}}\right] \cdot R_L}. \tag{28}$$

Fig. 7 shows the relation between C_{TP} and K for various selected $V_{o,\text{avg}}$ in the three-stage example. It can be seen that the minimum C_{TP} occurs at $K = 1$. In addition, by solving $dC_{\text{TP}}/dN = 0$ for a fixed $V_{o,\text{avg}}$, the optimum number of stages N associated with the minimum C_{TP} can be found. The solution is given as

$$N = 2(V_{o,\text{avg}} - V_d)/V_s. \tag{29}$$

The optimum value of N must be an integer near the result of (29). Fig. 8 provides the information needed to find the value of N for generating a specified $V_{o,\text{avg}}$ with minimum C_{TP}. As an example, by using the results from Fig. 7 and Fig. 8, a PGI circuit with an output voltage of 4 V across a resistive load of 100 kΩ can be designed for a minimum C_{TP} with $N = 3$ and $C_m = 60$ pF.

III. Model Validation

In order to validate the accuracy of the derived model, SPICE simulations are performed for both the equivalent three-stage PGI circuit shown in Fig. 3 and the corresponding model, where $V_d = V_s = 1.5$ V, $R_L = 100$ kΩ, $f_s = 1$ mHz, and D was determined by employing the relation between C_3 and C_O from (20).

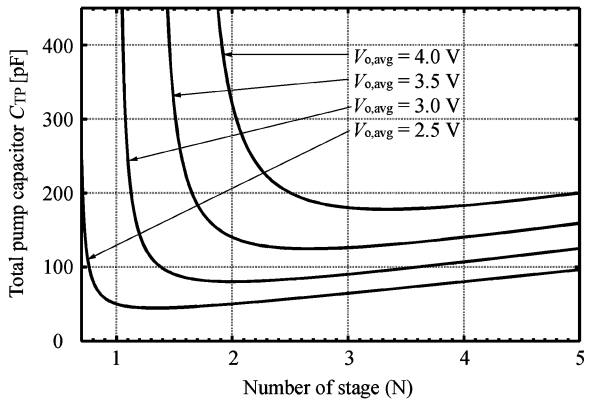

Fig. 8. Total pump capacitances $C_{\rm TP}$ versus the stage number N over various desired $V_{o,\rm avg}$, where $V_d = V_s = 1.5$ V, $R_L = 100$ kΩ, and $f_s = 1$ MHz.

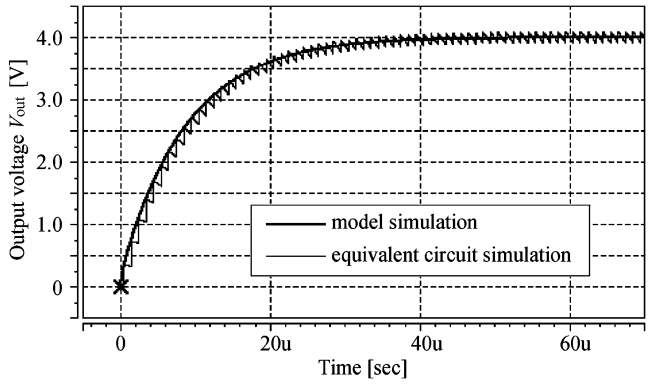

Fig. 9. Comparison between the simulated output waveforms of the equivalent three-stage PGI circuit and the corresponding model.

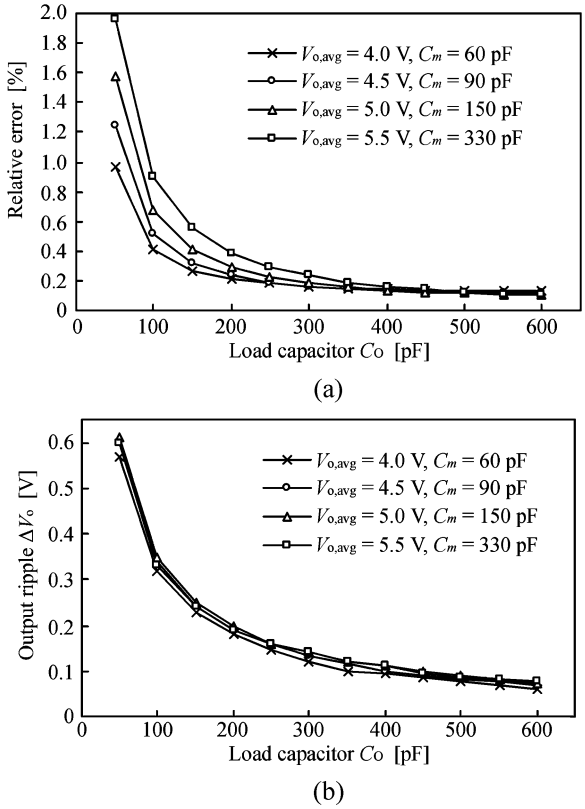

Fig. 10. (a) Relative errors between the model and the three-stage PGI circuit for different desired $V_{o,\rm avg}$ with $V_d = V_s = 1.5$ V, $R_L = 100$ kΩ, $f_s = 1$ MHz, and $D = 0.5$. (b) Corresponding output ripple ΔV_o.

Fig. 9 shows the output simulation waveforms of the equivalent three-stage circuit and the model, respectively, where the simulation conditions are $C_m = 60$ pF ($m = 1, 2, 3$), $C_O = 200$ pF, $I_L = 40$ μA, and $D = 0.57$. Under these design conditions, the output ripple ΔV_o is limited to 0.2 V, and the mean of the undulated output voltage is 4 V, which is equal to $V_{o,\rm avg}$ of the model in steady state. A satisfactory agreement between the two simulations can be observed during the procedure of boosting. From additional simulation data with different C_m values and various numbers of pump stages, the output values of the models always follow the undulated output waveforms of the equivalent PGI circuits. Consequently, these simulation results show that the presented model can predict the output behavior of a multistage PGI circuit with a resistive load.

In common uses, the duty ratio of CPCs is usually set to $D = 0.5$. However with this configuration, (20) is ineffective in finding a suitable value of C_O/C_N for equating V_k to $V_{o,\rm avg}$ shown in Fig. 6. If $C_O \gg C_N$, ΔV_{o1} will be close to ΔV_{o2} and the difference between $V_{o,\rm avg}$ and V_k can be reduced. Otherwise, a slightly greater error will exist. Fig. 10(a) shows the difference error of $V_{o,\rm avg}$ and the mean of the undulated output voltage of the equivalent three-stage PGI circuit obtained from the SPICE simulation results when a square clock waveform $(D = 0.5)$ is employed. In addition, the corresponding value of ΔV_o is shown in Fig. 10(b). From Fig. 10, it can be seen that the larger the value of C_O, the smaller the relative error and output ripple ΔV_o. If C_O is larger than 200 pF, it appears that the error and ΔV_o are less than 0.4% and 0.2 V, respectively.

A practical embodiment of a three-stage PGI-3 circuit, which is built by the circuit shown in Fig. 2(a), was simulated in the MOS level by using parameters of a TSMC 0.35-μm mixed-mode model and general clocks $(D = 0.5)$. With the same simulated conditions used in Fig. 9, except that the duty ratio $D = 0.5$, the transient simulation waveforms are shown in Fig. 11. From the simulation results, the final mean value of the practical circuit is about 3.95 V, and the error between this mean value and the final value of $V_{o,\rm avg}$ from the model is about 1.25%. Besides the influence of D, this small error is most likely due to the fact that switching losses and parasitic capacitances of the practical circuit are taken into account in the SPICE simulation but not included in the model. In addition, the full practical circuit simulation waveform lags slightly behind that of the model. This waveform lag is due to the fact that gate control voltages of the transfer switches generated by CTSs in the PGI circuit would not be pumped to the levels for turning on the switches completely in the initial few cycles. In summary, the output behavior and the final $V_{o,\rm avg}$ of the model closely match the simulation results of the practical PGI circuit.

IV. Measurement Results

In order to validate results of the analysis and design considerations, several PGI circuits with different numbers of stages were fabricated in a TSMC 0.35-μm mixed-mode process. To increase the flexibility of measurements, pump capacitors were

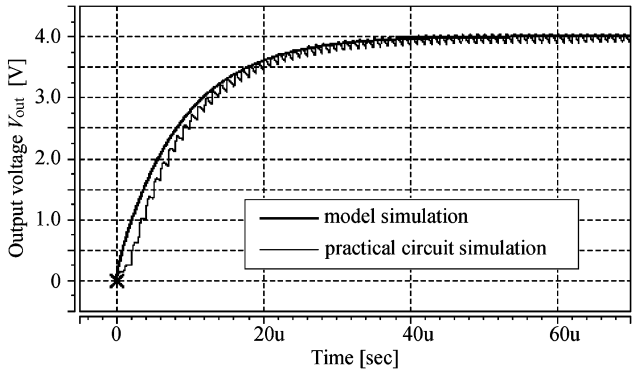

Fig. 11. Comparison between the simulated output waveforms of the practical three-stage PGI circuit and the corresponding model.

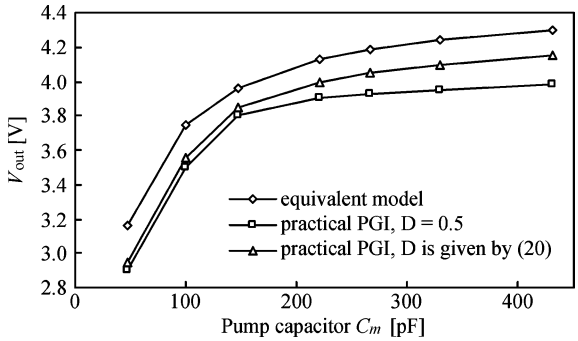

Fig. 12. Measured output voltages of a two-stage PGI-3 circuit under different values of C_m.

connected externally. A two-stage PGI circuit was tested under $V_d = V_s = 1.5$, $R_L = 100$ kΩ, $C_O = 330$ pF, $f_s = 1$ MHz, and $C_1 = C_2 = C_m$. Three kinds of output voltage data are plotted in Fig. 12 for the comparison. Two are obtained from the measured output voltages for $D = 0.5$ and the value calculated from (20). The third is obtained from the simulation results of the presented model. The performance data and the corresponding errors are summarized in Table I. For this typical example, the measured output voltages are close to $V_{o,\text{avg}}$ of the model, e.g., for $C_m = 100$ pF, the mean of the measured output voltages V_{out} are 3.5 and 3.55 V when $D = 0.5$ and 0.57 calculated from (20), respectively, and $V_{o,\text{avg}}$ is 3.75 V when using the model simulation. It can be seen from Table I that the error voltages in this case are lower than 0.25 V, and all the relative errors of the measurements are less than 8%. The measured output voltages are smaller than the model simulation output voltage $V_{o,\text{avg}}$, due to additional parasitic capacitors, parasitic resistors, and extra switching losses. In the case of C_m above 150 pF, where C_m/C_O is above 0.45, Fig. 12 also shows that the V_{out} measured as D obtained from (20) is more accurate than that measured as $D = 0.5$. However, even though the ratio of C_m/C_O is increased, the relative errors in the case of $D = 0.5$ only increase slightly. This agrees with the theoretical results depicted in Fig. 10.

Further experiments of the two-stage PGI circuit at $D = 0.5$ were also taken by changing the ratio of C_1 to C_2. The measured data are shown in Fig. 13. The curves of V_{out}-to-K and

TABLE I
SIMULATED RESULTS OF THE PRESENTED MODEL AND MEASURED RESULTS OF THE TWO-STAGE PGI DESIGN

Pump Capacitor C_m (pF)	Equivalent Model $V_{o,\text{avg}}$ (V)	Practical 2-stage PGI-3 Design				
		D = 0.5		D is given by (20)		
		V_{out} (V)	Err	duty, D	V_{out} (V)	Err
47	3.16	2.9	8.2%	0.53	2.95	6.6%
100	3.75	3.5	6.7%	0.57	3.55	5.3%
147	3.96	3.8	4.0%	0.59	3.85	2.7%
220	4.13	3.9	5.6%	0.63	4.0	3.1%
267	4.19	3.93	6.2%	0.64	4.05	3.3%
330	4.24	3.95	6.8%	0.67	4.1	3.3%
430	4.30	3.98	7.4%	0.70	4.15	3.5%

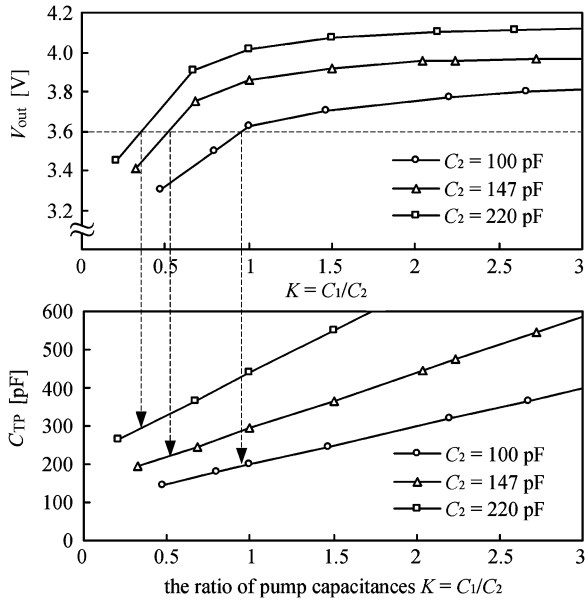

Fig. 13. Measured output voltages of a two-stage PGI-3 circuit with a different ratio of C_1 and C_2.

C_{TP}-to-K give information that $K = 1$ is the optimum selection to generate a desired dc output voltage. For instance, when $V_{\text{out}} = 3.6$ V is considered, Fig. 13 shows that $K = 1$ gives the minimum C_{TP}. This observation is in accordance with the prediction of (28).

V. CONCLUSION

An analysis and modeling technique of on-chip charge pumps with a resistive load based on PGI circuits has been proposed. The equations of the model also have been deduced for design within an acceptable accuracy tolerance. By using the presented model and equations, the output behavior can be approximately predicted and the capacitances and the switching period can be determined while satisfying the requirement of a desired final output voltage with a ripple ΔV_o. Based on the analysis presented, with a given resistive load and a desired output voltage across it, an optimal number of pump stages and equalized pump capacitors have been proved for the objective of minimum total pump capacitance, which represents minimum chip size. In addition, the influence of the duty ratio D on the output voltage and the accuracy of the model under general clocks $(D = 0.5)$ have been discussed. The simulation results of the presented model and the SPICE simulations of PGI circuits exhibit satisfactory

agreement on transient behavior and the final value of the output voltage. Analysis of the measurement results for an integrated two-stage PGI-3 circuit at light loading also has validated the model. A comparison of data shows that the relative errors are lower than 8%. Furthermore, since the structure of each pump stage model is simple and regular, it is easy to construct the complete model of a multistage PGI circuit.

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