ELSEVIER

Thin Solid Films 290-291 (1996) 458-463

Effects of mechanical characteristics on the chemical–mechanical polishing of dielectric thin films

Wei-Tsu Tseng [a,*], Chi-Wen Liu [b], Bau-Tong Dai [a], Ching-Fa Yeh [c]

[a] National Nano Device Laboratories, 1001-1, Ta-Hsueh Road, Hsinchu 300, Taiwan

[b] Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan

[c] Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, 1001, Ta-Hsueh Road, Hsinchu, Taiwan

Abstract

The effects of as-deposited (intrinsic) stress, externally applied (extrinsic) stresses, hardness, and modulus of various dielectric films on chemical–mechanical polishing (CMP) removal and post-CMP cleaning processes are studied in this article. Intrinsic stresses of the polished dielectrics do not contribute directly to the CMP removal rate. Extrinsic stresses including normal and shear components are calculated using principles of elasticity and fluid mechanics respectively and their roles in the material removal process are discussed. Theoretical evaluation and experimental results both suggest that hardness and modulus are the two most important material characteristics affecting the CMP process. Efficiency of post-CMP particle extraction can be monitored using an adhesion probability which is related to the hardness of wafer and pad. In addition, particle removal rate can be remarkably enhanced by increasing pressure (normal stress) while increasing pad rotation speed (shear stress) contributes little to reduce the particle count.

Keywords: Chemical–mechanical polishing; Hardness; Stress; Dielectrics

1. Introduction

The shrinking dimensions of devices to increase packing density for the IC technologies of future generations (0.35 μm or less) impose greater demands on the planarization process. This results from the lithographic need for steppers with reduced depth of focus which inherently enforces a more stringent requirement for flat and planarized surfaces. Among the newly developed planarization technologies for ULSI metallizations, chemical–mechanical polishing (CMP) has been shown to be the most promising because of its demonstrated capability to provide better local and global planarization of wafer surfaces in multilevel metallization interconnect structures for advanced IC devices [1,2].

During CMP of dielectrics, material removal was achieved by the relative motion of the wafer and the pad on which a proper slurry is dispersed. The roles of the slurry are both to chemically attack the dielectrics and to mechanically deform the polishing surface. Hence, the surface mechanical properties of polished films have great influence on the wear mechanism during CMP processes. In addition, the particle removal process through rubbing or scrubbing actions during post-CMP cleaning depends much upon the adhesion forces between particles and wafer surface and hence the mechanical nature of surface of the dielectrics [3]. Thus, there is a need to study the correlation between the mechanical characteristics of the dielectric films and the variations in the material removal rate during CMP and in the particle removal efficiency during post-CMP cleaning.

The goal of this study is to elucidate the roles of common mechanical characteristics in the material removal and the post-CMP particle cleaning processes. Emphasis on the evaluation of the contribution of and correlation between stresses, both intrinsic and extrinsic, hardness and modulus in a dielectric CMP process. Since, for most of the covalent-bonded materials, a tensile stress corresponds to bond stretching whereas a compressive stress translates to bond contraction in the structure, the surface of the dielectric materials being polished may have been weakened or strengthened depending on the state of their intrinsic stresses. In fact, silicon dioxide has been found to relax its tensile stress by cracking [4]. Thus the existence of such intrinsic stresses may assist or retard the material cutting process to certain extent. On the other hand, during a CMP operation, the imposition of a down force and a pad rotation exerts on the wafer additional normal and shear stresses respectively. These stress components are directly related to the CMP removal rate as Preston's law

* Corresponding author. Tel: +886-35-726100 ext. 7717. Fax: +886-35-713403. E-mail: Wttsen@ndl.nctu.edu.tw.

0040-6090/96/$15.00
PII S0040-6090(96)09020-7

prescribes [5,6]. Nevertheless, how these extrinsic stresses, combined with the aforementioned intrinsic stresses, interact in a way to manipulate the CMP removal process remains obscure and is worth investigating.

From another perspective, hardness is the resistance of a material to plastic deformation which consistently gives an index of strength and structural coherence. The modulus of elasticity quantifies the elastic response of a material under static loading. Both of these quantities reveal the material's response to external mechanical perturbation and would be more infallible material indicators for CMP process control. Our previous work [7] found experimentally a linear relationship between the surface hardness and the removal rate of oxide films. Theoretical assessment on this observation is still lacking however and further work is needed to justify that point. Finally, the effects of the above mechanical characteristics on post-CMP cleaning process have rarely been addressed in the literature and deserve further investigation. We will investigate the above issues based on existing models and our own experiments.

2. Experimental

All test samples in the present study were grown on P-type (100), 150 mm silicon wafers. Thermally grown films of silicon dioxide were accomplished by wet oxidation, in which the silicon was exposed to the oxidizing ambient H_2, O_2 at 980 °C. Films of atmospheric pressure chemical vapor deposition (APCVD) and plasma-enhanced chemical vapor deposition (PECVD) oxide were deposited by reacting SiH_4 and O_2 at a temperature of 400 °C. TEOS and O_2 at 390 °C were used as reactant gases for TEOS-PECVD films while SiH_4, N_2 and NH_3 were used for deposition of Si_3N_4-PECVD films. Silicon-rich oxide films (SRO-PECVD) films were obtained in ambient SiH_4, N_2 and N_2O gases.

All experiments were carried out on a Westech 372M polisher with an IC 1000/Suba IV pad pre-wetted with CAB-O-SPERSE SC-1 slurry consisting of fumed silica particles suspended in alkali solution. Upon the completion of each polish, pad conditioning was performed to clean the pad of residual slurry and to lift the pad surface fibers for further processing. The thickness of dielectric films was measured with Nanometrics 2100XP at nine different spots across the wafer. The polish rate is defined as the removal rate averaged over the nine locations. The cross-wafer polish non-uniformity was less than 10%. In order to eliminate the run-to-run removal rate variation, the removal rate ratio (RR ratio) is defined as:

$$\text{RR ratio} = (\text{removal rate of dielectric film}) / (\text{removal rate of thermal oxide})$$

Intrinsic stresses of dielectric films were monitored from measured curvature change. The intrinsic stresses of most dielectric films are compressive while that of SiH_4-APCVD is tensile. A NANOTEST 500 indentation system with a Berkovich indenter was used to measure nanoscale hardness. All tests were performed at a nominal constant loading rate of 1.18 mN s^{-1} until a maximum displacement 300 nm reached. The pH of the dip solution for post-cleaning was adjusted by adding NH_4OH and HCL to D.I. water. The number of particles (≥0.2 μm) on the post-CMP wafer surface was counted with a TENCOR-4500 surface scan.

3. Results and discussion

3.1. The correlation between mechanical characteristics and CMP removal rate

The dielectric CMP process has much in common with glass polishing. Cook [5] reviewed the mechanics of glass polishing and proposed that removal rate is inversely proportional to the modulus, E, of glass. The theoretical work by Liu et al. [8] also deduced that the removal rate depends on the moduli of both abrasive particles and the film itself. Nanohardness of dielectric oxide films has been found to scale down with CMP removal rate [8] whereas the exact mechanism remains obscure. Correlation between film residual stress and removal rate have been reported [9,10] although proper explanations are still lacking.

In this section, an attempt will be made to clarify the roles of stresses (both extrinsic and intrinsic), modulus, and hardness in CMP removal process based on theoretical calculations as well as experimental data.

3.1.1. Extrinsic stresses of the dielectric films during CMP

Runnels and Eyman [6] considered a more general removal model analogous to Preston's equation:

$$\text{RR} = \hat{k} \times \sigma_n \times \tau \tag{1}$$

where $\hat{k}$ is the proportionality parameter and σ_n and τ are the normal and shear stresses on the wafer surface respectively. The normal stress originates from the down force imposed by the polish arm onto the wafer carrier while the shear stress arises from slurry flow generated by the relative rotational motion of platen and wafer carrier. In this article, σ_n and τ are termed extrinsic stresses while the as-deposited stresses of the thin films are called intrinsic stresses.

Under a CMP down force P, the pad is deformed and the size of the pad surface features (or "valleys") become smaller; therefore, more silica particles can effectively abrade the film surface. This process apparently has contribution to the modified Preston equation presented above. Consequently, the normal stress is actually applied to the wafer through direct contact between the polished wafer surface and the abrasive particles. Cook [5] reviewed the mechanics during glass polishing which can be applied to the case of CMP. In his model, impingement of abrasive particles transported by the slurry leads to Hertzian penetration of the surface. The CMP process can be perceived as a travelling indenter whose interaction (contact) with the wafer surface gives rise to bond weakening and hence atomic removal. The force F acting on a particle of diameter d in the particle/wafer contact is expressed as:

$$F=\frac{\sqrt{3}Pd^2}{2K} \tag{2}$$

where K is the abrasive fill fraction which is unity for a fully-filled closed packing. Assuming spherical particles, the contact area between the polishing particle and the polished material surface is πr_c^2, where the radius of contact is given by:

$$r_c=\left\{\frac{3}{4}F(d/2)\left[(1-\nu^2)/E+(1-\nu^{2\prime})/E'\right]\right\}^{1/3} \tag{3}$$

where ν' and E' are the Poisson's ratio and elastic modulus of the polishing particle respectively. Given Eqs. (2) and (3), the normal stress σ_n can be calculated:

$$\sigma_n=\frac{F}{\pi r_c^2} \tag{4}$$

The basic specifications of the SC-1 slurry used for this study is listed in Table 1. The solid concentration of the slurry is reduced to 11.25 wt.% after being diluted by two (volume) parts of D.I. water. Assuming $K=0.5$, $\nu=\nu'=0.03$, $E=E'=70$ GPa [5] and a down force of 7 psi (48 260 Pa), the calculated normal stress based on Eq. (4) is about 46 MPa.

Runnels [11] relates the feature-scale erosion rate to Preston's equation by simulating the stresses due to slurry flow. In his model, the shear stress τ can be approximated as:

$$\tau=\left(\mu\frac{V}{\sqrt{\mu V/PA}}\right)=\sqrt{\mu VPA} \tag{5}$$

where μ is the dynamic viscosity, V is the pad velocity and A the wafer surface area. The calculated shear stress based on Eq. (5) and the parameters in Table 1 is about 170 Pa, or five orders of magnitude lower than the normal stress!

The large disparity between the normal and shear stresses seems surprising at first given the modified Preston's equation that the removal rate is proportional to both of them as indicated in Eq. (1). The roles of the two stress components in the removal process are different however and may not be compared on the basis of their magnitude. The normal stress acting on the travelling indenter (particle) gives rise to a compressive zone extending from the leading edge and a corresponding tensile zone extending from the trailing edge, hence contributes directly to the bond breaking of the polished material. While, on the other hand, the shear stress signifies the speed at which the removed material gets carried away by the flowing slurry. Both of the processes combined contribute to the effective removal of material during CMP operation.

Table 1
Specifications of SC-1 slurry

pH (adjusted with KOH)	10.0 ~ 10.3
Specific gravity	1.198 ± 0.012
Viscosity	< 150 cps
Weight per gallon	10.0 ± 0.1
Wt.% solids	30.0 ± 0.3
Nominal particle size	30 nm

3.1.2. *Effects of intrinsic stresses*

The intrinsic stresses for various dielectric films and their effects on the CMP removal rate are presented in Fig. 1. For all the SiO_2-based dielectrics, no distinct correlation between the intrinsic stress and removal rate can be identified. The bond stretching or contraction due to tensile or compressive stresses respectively in the oxide network apparently contributes little to assist or to impede the material removal process during CMP. However, one study [9] found a corresponding increase in CMP removal rate with increasing compressive stress in SiN_x films as the films become more silicon-rich. Another recent investigation [10] identified a linear relationship existing between the intrinsic stress (from high compressive to low tensile) and CMP removal rate for fluorinated oxide (SiOF) films.

The above contradiction may be rationalized on the basis of the enhanced chemical effects during CMP. In the present study, the stoichiometry for the various oxides does not alter and the O–Si–O bonding configuration remains essentially the same except for a few impurity species embedded in the network due to different processing gases. For the silicon nitrides however, the films become silicon rich as stress increases. The variation in stoichiometry may have altered the bonding and the chemical etching rate of the nitride therefore the chemical erosion rate during CMP is enhanced. The same reasoning can be applied to account for the CMP rate increase in fluorinated oxides. The shift in stress towards the tensile side also corresponds to increases in wet etching rate and fluorine concentration [10]. The presence of the highly electronegative fluorine not only changes the configuration of the oxide network but also increases the hydrophicility of the films. The intensified water permeation combined with

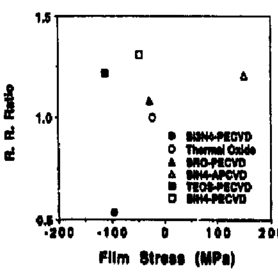

Fig. 1. CMP removal rate versus intrinsic stress for various dielectrics.

the formation of the corrosive HF radicals are directly responsible for the enhanced CMP removal rate [12] which coincides with the stress changes in the fluorinated oxide films.

The magnitude of the intrinsic stress for most oxide films resides in the range of 100 ~ 300 MPa which is far less than their tensile strength (5000 ~ 7000 MPa). Therefore, assuming minimum cracks or other stress raisers in the oxides, the intrinsic stress would contribute little, if any, to the breaking of the bonds. Also worth noting here is that the calculated normal stress (46 MPa) is about two orders of magnitude lower the tensile strength. In Cook's model [5], the maximum tensile stress in the tensile zone trailing behind the moving particle is only around 200 ~ 300 MPa to the best of approximation. How these stresses surmount the tensile strength to break the materials away hence becomes an intriguing question. The formation of a soft surface layer, possibly in hydrated form, due to chemical attack by the slurry may provide an explanation to the above scenario. The exact mechanism would not be clear however until knowledge on the chemical aspect of the CMP process improves.

3.2. Effects of hardness and modulus on removal rate

While stress provides only static-state information of a material, hardness reflects the resistance of a material to plastic deformation and hence provides more information on the deformation and wearing of the materials themselves. The analogy of a moving particle to a traveling indenter adopted by Cook in his model suggests that hardness may be a more useful material index to monitor CMP removal rate. On the other hand, the application of elasticity theory to model polish mechanics as presented by several previous studies [6,13] implies that elastic modulus may play certain role in the polishing operation. Since most of the dielectric materials undergo only elastic deformation before fracture, the magnitude of their elastic modulus may have some correlation with their CMP removal rate.

Our previous work [7] found that the polishing rate of the various dielectric materials is inversely proportional to their hardness except for PECVD Si_3N_4 whose removal rate rests above the fitted RR vs. hardness line (Fig. 2). This discrepancy can be explained on the basis of the different mechanical characteristics between the abrasive particles and wafer during polishing as discussed below. Cook's theory [5] and the wear model by Liu et al. [8] have both correlated the removal rate with mechanical properties of the wafer surface and abrasive particles:

$$RR = C \times (1/E_a + 1/E_w) \times P \times V \quad (6)$$

where E_a and E_w are the elastic moduli of the abrasive particles and the wafer surface, respectively. C is a constant relating chemistry to material removal process.

Gilman [14] has shown that the microhardness of structural materials increases linearly with an increasing modulus, and the hardness-to-modulus (H/E) ratio is about 1/10 for

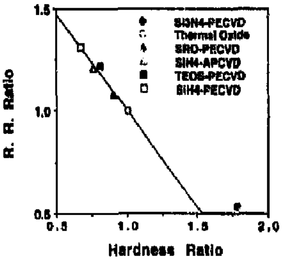

Fig. 2. Effects of film hardness on CMP removal rate for various dielectrics.

most covalently bonded solids. Thus Eq. (6) can be transformed into

$$RR = C' \times (1/H_a + 1/H_w) \times P \times V \quad (7)$$

where H_a and H_w are hardness of the abrasive particles and the wafer surface, respectively. C' is a constant. Therefore, as Eq. (7) indicates, a linear relationship exists between the surface hardness and the removal rate of oxide films under well-controlled CMP processes.

On the other hand, the basic structure of silicon nitride consists of a SiN_4 tetrahedron shared by three other SiN_4 tetrahedra to form a three-dimensional network. This creates the exceptionally strong bonding in SiN, producing a very rigid structure with a Young's modulus greater than three times that of quartz, in which the oxygen atom in SiO forming a silicate network share only two tetrahedra [15]. In addition, the chemical nature and corrosion susceptibility of nitride and oxide are different. Thus, the combined mechanical and chemical differences gives rise to the removal rate deviation of nitride from those for oxides in Fig. 2.

3.3. Effects of mechanical properties of dielectric films on particle removal

Particle contamination on a wafer surface often causes a dramatic decrease in device yield. Much work has been done to describe the particle deposition mechanism with the intention to minimize the number of metal contaminants, residual chemicals and other foreign particles remained on wafer surface [16]. Post-CMP cleaning is often achieved through mechanical brushing or scrubbing actions aided with proper chemicals to "dissolve" the particles away. It has been reported that the sign and magnitude of the zeta potentials between slurry, wafer surface and pad play critical roles in the particle deposition/extraction processes on the wafer surface [17]. However, measurements of the zeta potential on the wafer surface exhibit complex dependence on pH, type of chemical, method of post-CMP cleaning, wafer rotation speed, water flow rate, and other machine parameters, and therefore is not considered a quick and efficient way for process control.

Since particle removal by mechanical brushing and scrubbing actions resembles much of the material removal process

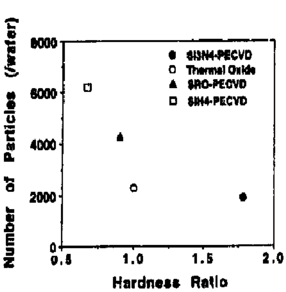

Fig. 3. The number of particles remaining on the post-CMP wafer surface versus film hardness after 30 min dip at solution with pH = 10.

in CMP, the mechanism of post-CMP cleaning may exhibit similar dependence on the mechanical characteristics as discussed in the previous sections. In fact, the adhesion force [18] between particles of polished dielectrics and the cleaning pad is related to their hardness and hence can be an important indicative for the ease of particle removal. This point will be elaborated in this section. In addition, extrinsic stresses which are found to dominate the CMP removal process will be investigated again with the intention to clarify their roles in the post-CMP buff cleaning process.

3.3.1. The effects of hardness on particle removal process

In order to examine the effects of film hardness on particle removal for polished wafers, post-CMP wafers are directly transported from the unload cassette to a tub with dip solution. Fig. 3 indicates that less particles would remain on the harder (nitride) wafer surface after 30 min dip at the solution with pH = 10. This phenomenon can be justified from the standpoint of "adhesion force" since the probability of adherence of particles on polished film (Ω) is related to the hardness of the pad surface (H_p) and of the polished film (H_f) [18]:

$$\Omega = H_p/(H_p + H_f) \tag{8}$$

For dielectric materials, the wafer surface is hard and brittle, while the pad, typically polyurethane-based materials, is much softer. Hence, Eq. (8) can be simplified as:

$$\Omega = H_p/H_f \tag{9}$$

Eq. (9) suggests that the probability of particles physically embedded on the wafer surface is inversely proportional to the hardness of the polished film, i.e. particles can be removed more easily from the harder surface. The existence of hardness terms in the expression for adhesion probability implies that particles are indented into the wafer surface. Thus the mechanism of its removal would bear the similar dependence on material characteristics discussed in Section 3.2.

Eqs. (8) and (9) give qualitatively the relative ease of particle removal and should be applied with caution. Hardness alone may not be enough to monitor the particle removal process. For further study, additional material characteristics such as surface roughness (of wafer and pad) would be needed to modify Eq. (8).

3.3.2. Effects of extrinsic stresses on particle removal

In-situ removal of particles on the post-CMP wafer surface via an applied pressure was carried out on the cleaning platen. Each polished wafer was subjected to 30 s of mechanical buffing with a Rodel finishing pad (Politex Supreme Regular Nap). Deionized water was applied during buffing, and both carrier and platen were rotated at 60 rpm. As Fig. 4 indicates, the final particle counts can be reduced significantly by increasing pressure. Based on the experimental results, the particle removal efficiency is found to be greatly improved by increasing pressure to 3 psi for undoped oxide and 10 psi for PECVD-nitride film, respectively. In contrast, post-buffing particle count is plotted against pad rotation speed in Fig. 5 with pressure and carrier speed set at 3 psi and 60 rpm, respectively. Unlike the polishing process, the particle level the on wafer surface is almost independent of pad speed. The above results clearly indicate that normal stress related to pressure plays a much more important role in particle removal than shear stress related to platen and carrier rotation speeds. While the concept of indentation can be applied to both material polishing and particle removal processes, the latter does not involve material cutting actions however and this may provide an explanation to the different behaviors between the

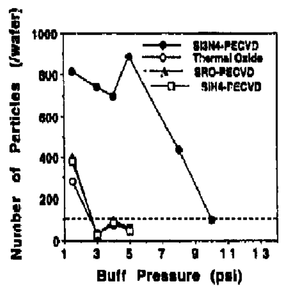

Fig. 4. Effects of buff pressure on the number of particles remaining on the post-CMP wafer surface. Particle count less than 100 per wafer is considered a viable cleaning process.

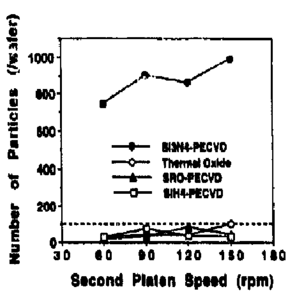

Fig. 5. Post-CMP particle count versus platen speed for various dielectrics.

two processes. During polishing, a shearing action is needed to peel off the indented material whereas during particle removal process a large enough applied pressure overcomes the adhesion and electrochemical forces, plowing the particles off from the wafer surface without physically tearing apart the adjacent materials.

4. Conclusion

The effects of extrinsic stresses, intrinsic stresses, hardness and modulus of various dielectric films on the CMP removal process are examined theoretically and experimentally. The calculated extrinsic normal stress is about five orders of magnitude higher than extrinsic shear stress and it would be expected that both of them contribute remarkably to the material removal during CMP. On the contrary, intrinsic stress plays little role in the polishing process. Correlation between intrinsic stress and CMP removal rate identified in other studies may arise from chemical interactions between slurries and wafers. The material removal process during CMP can be perceived as a moving indenter across wafer surface. Removal rate of dielectrics is inversely proportional to the combined hardness of dielectrics and abrasive particles. An adhesion probability related to material hardness can be used to indicate the relative efficiency in post-CMP particle removal. Finally, normal stress (pressure) is found to dominate over shear stress (rotation speed) in the particle reduction on the wafer surface.

Acknowledgements

This work is financially supported by TSMC, and National Science Council (NSC84-2622-E009-007) of Taiwan.

References

[1] W.J. Patrick, W.L. Guthrie, C.L. Standley and P.M. Schiable, *J. Electrochem. Soc., 138* (1991) 1778.

[2] W.L. Guthrie, W.J. Patrick, E. Levine, H.C. Jones, E.A. Mehter, T.F. Houghton, G.T. Chiu and M.A. Fury, *IBM J. Res. Develop., 36* (1992) 845.

[3] D. Heatherington, P. Resnick, R. Timon, B. Braper, M. Ravkin, J. DeLarios, W. Krusell and A. Madhani, *Proc. Dielectrics for VLSI/ULSI Multilevel Interconnect Conf.*, VMIC, Tampa, FL, USA, 1995, p. 156.

[4] A.K. Sinha, H.J. Levinstein and T.E. Smith, *J. Appl. Phys., 49* (1978) 2423.

[5] L.M. Cook, *J. Non-Cryst. Solids, 120* (1990) 152.

[6] S.R. Runnels and L.M. Eyman, *J. Electrochem. Soc., 141* (1994) 1698.

[7] C.-W. Liu, B.-T. Dai and C.-F. Yeh, *J. Electrochem. Soc., 142* (1995) 3098.

[8] C.-W. Liu, B.-T. Dai, W.-T. Tseng and C.-F. Yeh, *J. Electrochem. Soc., 143* (1996) 716.

[9] B.-T. Dai, W.-T. Tseng, C.-H. Liu and C.-F. Yeh, *Proc. SEMI Taiwan Technical Symp.*, SEMI, Mountain View, CA, USA, 1995, p. 105.

[10] C.-P. Chen, C.-T. Lee, C.-F. Lin, H.-C. Yung and L. Fang, *Proc. 1st. Int. CMP Planarization for VLSI/ULSI Multilevel Interconnection Conf.*, VMIC, Tampa, FL, USA, 1996, p. 82.

[11] S.R. Runnels, *J. Electrochem. Soc., 141* (1994) 1900.

[12] Y.-T. Hsieh, W.-T. Tseng, B.-T. Dai, T.-C. Chang, Y.-J. Mei, J.-D. Sheu, C.-F. Lin and M.-S. Feng, *Proc. 2nd. Int. Dielectrics for VLSI/ULSI Multilevel Interconnect Conf.*, VMIC, Tampa, FL, USA, 1996, p. 287.

[13] T. Izumitani, in M. Tomozawa and R. Doremus (eds.), *Treatise on Materials Science and Technology*, Vol. 17, Academic Press, New York, 1979, p. 115.

[14] J.J. Gilman, *Mechanical Behavior of Crystalline Solids*, National Bureau of Standards Monograph, Vol. 59, Gaithersburg, MD, USA, 1963, p. 79.

[15] J.A. Taylor, *J. Vac. Sci. Technol., A9* (1991) 2464.

[16] W.C. Krusell, J.M. de Larios and J. Zhang, *Solid State Technol., 38* (6) (1995) 109.

[17] T.L. Myers, M.A. Fury and W.C. Krusell, *Solid State Technol., 38* (10) (1995) 59.

[18] I.V. Kragelsky, M.N. Dobychin and V.S. Kombalov, *Friction and Wear, Calculation Methods*, Pergamon Press, New York, 1982, p. 352.