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A High Performance Spread Spectrum Clock Generator Using Two-Point Modulation Scheme

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SUMMARY A new spread spectrum clock generator (SSCG) using two-point delta-sigma modulation is presented in this paper. Not only the divider is varied, but also the voltage controlled oscillator is modulated. This technique can enhance the modulation bandwidth so that the effect of EMI suppression is improved with lower order ΣΔ modulator and can simultaneously optimize the jitter and the modulation profile. In addition, the method of two-path is applied to the loop filter to reduce the capacitance value such that the total integration can be achieved. The proposed SSCG has been fabricated in a 0.35 μm CMOS process. The clock of 400 MHz with center spread ratios of 1.25% and 2.5% are verified. The peak EMI reduction is 19.73 dB for the case of 2.5%. The size of chip area is $0.90 \times 0.89\,\mathrm{mm}^2$.

key words: *phase-locked loops (PLLs), spread spectrum, and two-point, fractional-N*

1. Introduction

Spread-spectrum clock generators (SSCG) have been widely employed as high-speed sources with reduced EMI levels [1]–[10]. Basically, SSCG is a phase locked loop (PLL) with special case of frequency modulation. There are two common modulation techniques employed within PLL loops. One is to control the variation of the divider [1]–[7] and the other is to modulate the VCO directly [8]. In the former case, a fractional-N PLL with a ΣΔ modulator is mostly used [1]–[7]. It has the advantage of being fully digital controlled. The modulator is controlled by a triangular waveform generator. The loop bandwidth is traded off between the modulation profile and jitter caused by the ΣΔ modulator. As the loop bandwidth is not wide enough, the modulation profile is distorted and the effect of EMI suppression is degraded. The method of using pre-distorted triangular waveform has been presented to improve the modulation profile [10]. Here, an alternative method of a two-point modulation is presented to enhance the bandwidth and to save the power, in the meantime, maintain the linear sawtooth waveform.

It is noted that the two-point modulation in PLL has been used in the frequency generator with DC-FM feature. Its transfer function appears as all-pass behavior. Recently, this technique is employed in a frequency hopping transmitter to gain the high data rate modulation [11]. The block diagram of the two-point modulation [11] is shown in Fig. 1 with one point at the input of the multi-modulus divider and the other at the input of the VCO. Usually a high resolution DAC is needed to achieve better performance due to the high VCO gain. It leads to high power consumption and large area penalty. In the mean time, an adder is needed to combine the two path signals. The two modulation paths suffer from the gain and delay mismatch [11]. This will make the design more complicated.

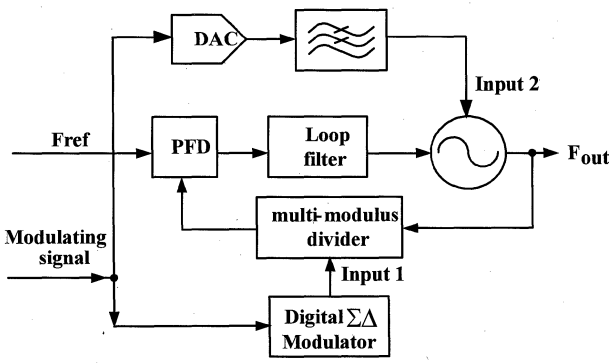

Fig. 1 The Traditional TPDSM architecture [9].

The spread spectrum clock generator is also a kind of frequency modulation. Therefore, the two point modulation can be applied. In this study, a modified SSCG with the two-point modulation and a dual-path loop filter (TPDL) is presented to achieve wide bandwidth and total integration.

Section 2 describes the proposed SSCG and the linear model analysis, the design consideration for the ΣΔ modulator and simulation results. CMOS circuits are described in Sect. 3. The measurement results are verified in Sect. 4. Conclusions are given in the last section.

2. Proposed TPDL-SSCG

For a typical PLL, the transfer function from the feedback divider to the VCO output behaves as a low-pass function. On the contrary, the transfer function from the VCO input to VCO output behaves as a high pass function. An all-pass function can be obtained hopefully when the loop is excited simultaneously through these two points. The modulation speed is independent of the loop bandwidth. The block diagram of the proposed TPDL-SSCG is shown in Fig. 2 with a phase-frequency detector (PFD), a dual path loop filter, a VCO, an 8-bit programmable counter (PGC), a digital ΣΔ modulator, a modulation profile generator, and a digital to

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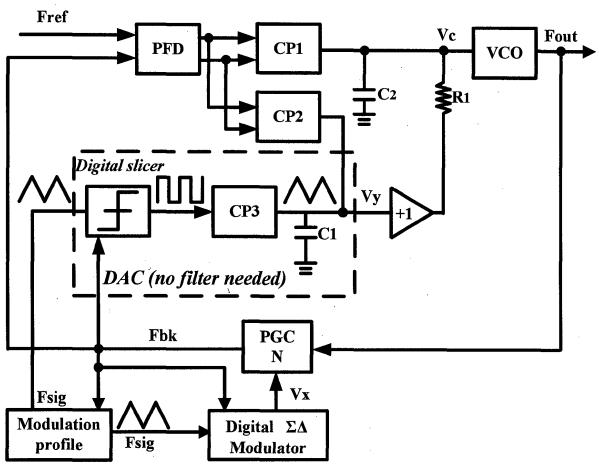


Fig. 2 The block diagram of the proposed TPDL-SSCG.

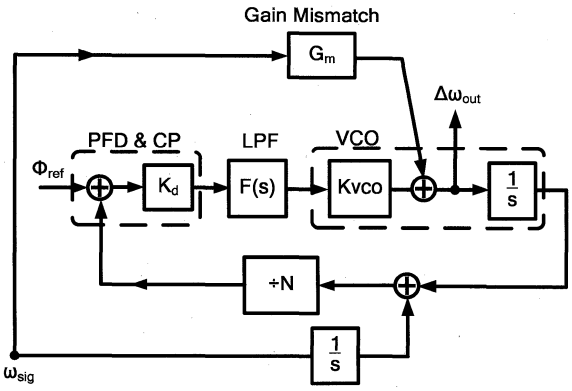


Fig. 3 Linear model of the TPDL-SSCG.

analog converter (DAC). The dual-path loop filter [12] consists of charge pumps CP_1, CP_2, capacitors C_1, C_2, and a resistor R_1, and a unity-gain amplifier. The benefit of the dual-path loop filter is to diminish the capacitance area C_1. The area of C_1 could be reduced while the current CP_2 is smaller than the current CP_1. The profile generator is used to generate the triangular waveform to be fed into the digital $\Sigma\Delta$ modulator and the DAC, simultaneously. The two modulation points are denotes by V_x and V_y. Point V_x is at the input of the PGC through the $\Sigma\Delta$ modulator and point V_y is at the input of the VCO through the DAC. The overall modulation behavior acts an all-pass feature as long as the two modulation schemes are well matched. The operations are analyzed in the following paragraphs.

2.1 The Proposed DAC

The proposed DAC consists of a digital slicer, CP_3, and C_1. The digital slicer slices the digital triangular waveform from the profile generator into a digital clock. The digital clock charges and discharges the C_1 through the CP_3 to perform the DAC. The digital transitions resided in triangular waveform can be effectively smoothed out without a reconstruction filter and a high resolution DAC as compared to the traditional one. Therefore, the power consumption and chip area are greatly reduced. In addition, the digital slicer, the profile generator and the digital $\Sigma\Delta$ modulator use the same clock, F_{bk}, which is the output signal of the PGC, the output of the digital slicer can be tracked with the triangular waveform very well so that the delay mismatch between two points can be avoided.

Ignoring the loading effects in CP_1 and CP_2, the relation between controlled voltage V_c and the current I_{p3} of CP_3 can be written as

$$\frac{V_c}{I_{p3}} \approx \frac{1}{sC_1} \tag{1}$$

under the condition of $F_{sig} \ll 1/(2\pi R_1 C_2)$. According to (1), the analog triangular waveform is created as I_{p3} is a square waveform. Capacitor C_1 plays an important role. It converts not only the digital modulation signal into analog modulation signal, but also acts as a part of loop filter. In this way, we can eliminate the two inputs VCO or an adder to combine the two modulation signals. Here C_1 with one terminal grounded is implemented by the accumulation MOS capacitor to save area and to reduce distortion when the gate-source bias voltage is equal to or larger than 1 V [15]. The relation between I_{p3} and spreading ratio δ, which is defined as $\Delta F_{out}/F_{out}$ is derived as

$$\delta = \frac{I_{p3} K_{vco}}{2C_1 F_{sig} F_{out}}. \tag{2}$$

where F_{out} is nominal output frequency, F_{sig} is the modulation frequency of the triangular waveform and ΔF_{out} is the peak to peak frequency deviation.

2.2 Linear Model Analysis

The dynamics of the proposed architecture are analyzed by the linear model as shown in Fig. 3. K_d is gain of the PFD and charge pump and K_{vco} is the conversion gain of VCO. The divider value is N. G_m is the gain factor for flat compensation between two modulation points. Here the delay mismatch is ignored as mentioned above. $F(s)$ is dual-path loop filter transfer function. I_{p1} is the current of CP_1, I_{p2} is the current of CP_2. Let $I_{p1} = BI_{p2}$. Here $B = 4$. The trans-impedance of the filter can be written as

$$F(s) = \frac{V_c}{I_{p1}} = \frac{R_1\left(s + \dfrac{1}{R_1 B C_1}\right)}{s(1 + sR_1C_2)}. \tag{3}$$

From (3), the zero is lowered to $1/(BC_1)R_1$ with the aid of CP_2. In other words, the magnitude of capacitance C_1 can be reduced by the factor B. It is a favor for total integration.

The unity gain amplifier implemented by a one-stage operational amplifier. The non-ideality of the amplifier is examined. It is modeled by its DC gain A_v and its unity-gain frequency ω_t. Then, the transfer function of the unity gain amplifier is described as

$$A(s) = \frac{A_{err}}{1 + \frac{s}{\omega_t}}. \quad (4)$$

as $A_{err} = A_v/(A_v + 1)$ denotes the gain error. By using (4) and re-calculating $F(s)$, one can obtain

$$F(s) \approx \frac{R_1\left(s + \frac{1}{R_1\frac{BC_1}{A_{err}}}\right)}{s(1 + sR_1C_2)} \quad (5)$$

when $\omega_t \gg 1/(R_1C_2)$. Comparing (5) to (3), it is clear that the gain error will cause the capacitance multiplication a little higher than the expected.

G_m is the gain mismatch factor which comes from the difference between V_x and V_y. The amplitude of digital triangular waveform will not depend on process variations, but the amplitude of the analog triangular waveform will depends on process variations. According to (2), the gain mismatch factor may come from the I_{p3}, C_1 and K_{VCO}.

Here the frequency relationship is derived for the nature of frequency modulation in SSCG instead of the phase relationship used in traditional PLL analysis. $\Delta\omega_{out}$ is the frequency deviation of output signal F_{out}. ω_{sig} is assumed conceptually to be the frequency deviation of transmit signal F_{sig}. The closed loop transfer function of Fig. 3 can be derived as

$$\frac{\Delta\omega_{out}}{\omega_{sig}} = T(s) + (1 - T(s)) \times G_m$$

with

$$T(s) = \frac{K_{vco}K_dF(s)}{Ns + K_{vco}K_dF(s)}. \quad (6)$$

The first term in the right hand side appears as a low pass and second term appears as a high pass as $F(s)$ in (5) is considered as a low-passed behavior. From (6), $\Delta\omega_{out}$ is equal to ω_{sig} if $G_m = 1$. It means that if there are no mismatches between two modulation points, the bandwidth is very wide and gives rise to low distortion in the output signal.

2.3 Design Consideration for Sigma-Delta Modulator

Two important issues are taken into account regarding the $\Sigma\Delta$ modulator design. One is the order of the modulator and the other is the loop bandwidth of the PLL. As we have already known that the high order $\Sigma\Delta$ modulator is used to suppress the fractional spurious within the loop bandwidth. Here, in this design, a second order $\Sigma\Delta$ modulator is chosen to save the area and power while maintain the quality of the noise performance. To see the interrelation between the order of the $\Sigma\Delta$ modulator and the PLL loop bandwidth, the output phase noises from the modulator and the VCO are investigated. The noise power spectral densities (PSD) of the phase noise at the PLL output $S_\Phi(f)$ can be expressed as

$$S_\Phi(f) = S_{\Phi VCO}(f) + S_{\Phi\Delta\Sigma}(f) \quad (7)$$

where $S_{\Phi vco}(f)$ and $S_{\Phi\Delta\Sigma}(f)$ are the noise PSDs of the VCO and the $\Sigma\Delta$ modulator, respectively. $S_{\Phi\Delta\Sigma}(f)$ [14] can be found as

$$S_{\Phi\Delta\Sigma}(f) = \frac{(2\pi)^2}{12F_{bk}}\left[2\sin\left(\frac{\pi f}{F_{bk}}\right)\right]^{2(m-1)} \cdot |T(f)|^2 \quad (8)$$

Where m is the order of the modulator, F_{bk} is the operational frequency of the modulator and $T(f)$ is the closed loop transfer function of the PLL defined in (6). $S_{\Phi vco}(f)$ can be easily derived as

$$S_{\Phi VCO}(f) = S_{\Phi vn} \cdot |1 - T(f)|^2 \quad (9)$$

In general the loop bandwidth is much less than the comparison frequency F_{bk} at the phase detector to avoid the spurious. From (8), It is realized that the output PSD caused by the $\Sigma\Delta$ modulator is increasing inside of the PLL bandwidth with the shape $f^{2(m-1)}$ due to high pass characteristic of the $\Sigma\Delta$ modulator and decreasing outside of the PLL bandwidth due to low-pass characteristic of $T(f)$. In other words, the smaller the loop bandwidth is, the lower the noise is caused by the modulator. However, large bandwidth is needed to pass faithfully the modulation profile. Otherwise, the jitter is degraded. Thus, the loop bandwidth is traded off between modulation profile and jitter performance. In a conventional fractional-N based SSCG (FN-SSCG) [4], one needs PLL bandwidth to be ten times modulation frequency to get better modulation performance and then better EMI performance. The in-band fractional spur are suppressed by the third-order $\Sigma\Delta$ modulator to minimize the phase noise and jitter. Besides, a third-order loop filter is needed to further reduce the output of band phase noise and jitter. In other words, it needs higher power consumption and more area. However, thanks to the all pass nature in two-point modulation, the loop bandwidth can be shrunk for jitter without modulation profile distortion. Hence, in this study, a second-order $\Sigma\Delta$ modulator and a 70 kHz loop bandwidth with a second-order loop filter are designed for saving power and area.

The simulation results of frequency variation for different loop bandwidths are shown in Fig. 4 with loop simulation parameters listed in Table 1. The center is set at 400 MHz, the spread ratio is 2.5%, and the modulation frequency is set at 40 kHz. Cases with loop bandwidths of 70 kHz and 400 kHz are considered to account for the proposed TPDL-SSCG and the conventional FN-SSCG. Four different spread ratios of 2.487%, 2.667%, 2.588%, and 2.598% for the FN-SSCG with a 70 kHz BW denoted curve-a, the FN-SSCG with a 400 kHz denoted curve-b, the TPDL-SSCG with a 70 kHz BW denoted curve-c, and the TPDL-SSCG with a 400 kHz BW denoted curve-d are obtained, respectively. It is clearly indicated that curve-c has not only more accurate spread ratio, but also lower noise with respect to curve-b because curve-b has smaller $\Sigma\Delta$ noise than curve-c and the two point modulation is adopted for curve-b. There is a 0.18% difference in spread ratios for PLL loop bandwidths changed from 70 kHz to 400 kHz for the FN-SSCG, while there is only 0.01% difference in spread ratios for the TPDL-SSCG. And one more effect is seen from Fig. 4 that

the bigger loop bandwidth and the larger jitter appear at the output for both architectures. This confirms the results in (8). The proposed TPDL-SSCG has the advantages of low distortion so that the modulation profile is more like a triangular waveform.

The numerical results of phase noise for curve-b and curve-c in Fig. 4 in non-spread spectrum mode are shown in Fig. 5. Here, noise sources from CP_1, CP_2, reference clock, and the unity gain amplifier of the dual-path loop filter are neglected for simplicity. The VCO phase noise is assumed as -100 dBc/Hz at offset frequency of 1 MHz with the shape of f^{-2}. The solid line and dashed line represent the total phase noise for the FN-SSCG with a 400 kHz loop bandwidth and the TPDL-SSCG with a 70 kHz loop bandwidth, respectively. Others simulation parameters are using the same parameters listed in Table 1. The phase noises contributed from the VCO and the ΣΔ modulator are also plotted. The phase noises from the VCO for the FN-SSCG and the TPDL-SSCG are denoted by the line with a circle mark and the line with plus mark, respectively. The phase noise from the ΣΔ modulator for the FN-SSCG and the TPDL-SSCG are denoted by the line with diamond mark and the line with square mark, respectively. From Fig. 5, the phase noise is dominated by the VCO phase noise in in-band and output-of-band for the TPDL-SSCG; while the phase noise is dominated by the VCO's phase noise in in-band and the ΣΔ modulator's phase noise in out-of-band for the FN-SSCG. The rms phase jitters integrated from 1 kHz to 14.31818 MHz are 15.80 ps and 15.96 ps for the FN-SSCG and the TPDL-SSCG, respectively. The rms phase jitter for the TPDL-SSCG with second-order modulator and second-order loop filter is almost the same compared to the FN-SSCG with third-order modulator and third-order loop filter. The advantage of the proposed TPDL-SSCG is obviously seen that first, a lower order ΣΔ modulator can be used for lower power consumption, second, the lower order loop filter can be used for smaller chip area, and third, the linear modulation profile and smaller jitter can be optimized simultaneously. By the way, one can further lower the jitter by minimized the VCO phase noise for the TPDL-SSCG while the jitter can't minimized any more for the FN-SSCG because the dominated phase noise in out-of-band is the ΣΔ modulator.

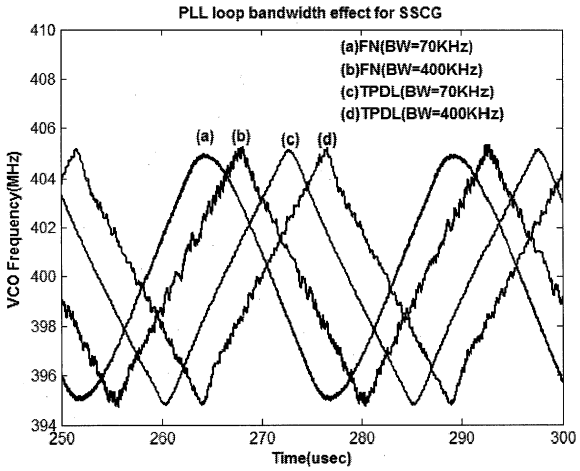


Fig. 4 SSCG output frequency for different PLL loop bandwidths with δ=2.5%.

Table 1 Simulation parameters.

	FN-SSCG	TPDL-SSCG
Input Frequency	14.31818MHz	14.31818MHz
Output Frequency	400MHz	400MHz
Spread Ratio	2.5%	2.5%
VCO Gain	200MHz/V	200MHz/V
Loop Bandwidth	70/400kHz	70/400kHz
Modulator	third-order MASH	second-order MASH
Loop filter	third-order	second-order
Third pole frequency	3.2MHz	N/A

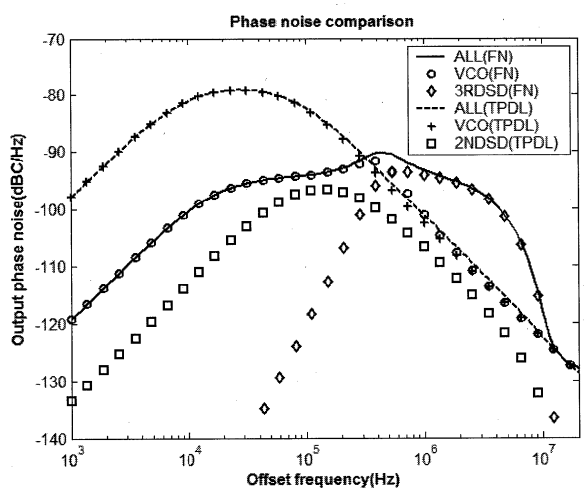


Fig. 5 Phase noise simulation for different PLL loop bandwidths.

3. Circuit Description

The circuits used in the work are described briefly next. In order to fulfill the various output frequency where the fractional part may exceed than 1, input range of the modified MASH-1-1 ΣΔ modulator is extended as shown in Fig. 6 to overcome the overflow problem [7]. Assume that the bit

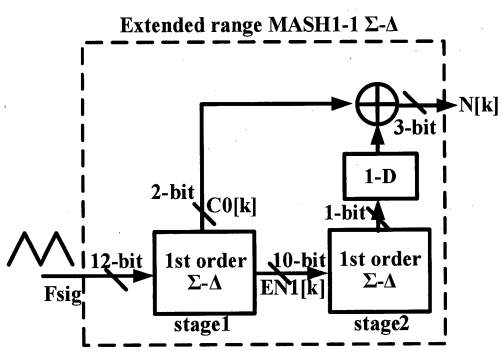


Fig. 6 Extended range MASH 1-1 ΣΔ modulator.

width of the modulator is BT. The input range of the conventional MASH type modulation is between $1/2^{BT}$ to $1-1/2^{BT}$. When an input exceeds 1, the modulator will be saturated to collapse the following stages. In order to conquer this issue, the architecture is revised. The stage-1 has a 2-bit carry while the stage-2 still keeps only 1-bit carry. The 2-bit carry outputs can manifest the inputs larger than or equal to 1 in such way that it bring quickly the integer part of the input to the output and will not saturate the following stages. The input range of the proposed one can be extended to $3-1/2^{BT}$.

Moreover, the proposed modulator can handle larger spread ratio than the conventional one and still have feature of unconditional stability.

The charge-pump of $CP_{1(2)}$ and CP_3 are shown in Figs. 7(a) and (b), respectively. The cascoded current sources with wide-swing bias circuit are employed for noise immunity against the power supply. A unity-gain buffer for CP_1 and CP_2 is used to reduce the charge sharing when switching. The unity-gain buffer is not needed for CP_3 due to the low operating frequency. The wide band VCO [13], which consists of the three stages of differential delay cells, is shown in Fig. 8(a). The schematic of the delay cell is shown in Fig. 8(b). The cross-coupled connection M_{n1} and M_{n2} is employed to obtain full swing and sharp waveform to reduce the jitter.

The unity gain buffer with rail-to-rail input and output used in the dual-path loop filter is shown in Fig. 9. The driving current is designed to be twice that of I_{p1} to provide enough driving capacity for CP_1. The simple one-stage design is adopted and its phase noise is designed for 10 dB less than the VCO phase noise at offset frequency of 1 MHz. The GBW is designed much larger than the pole of $1/R_1C_2$ to maintain linear modulation. The load of the buffer comprises a resistor R_1 in series with a small parasitic capacitor; therefore, no extra driving stage is needed.

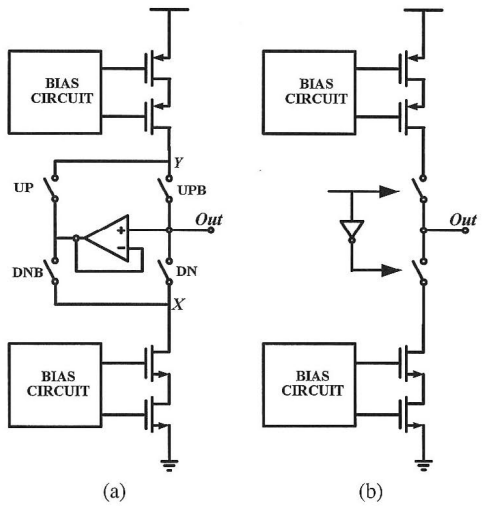


Fig. 7 (a) CP_1 and CP_2 circuits and (b) CP_3 circuit.

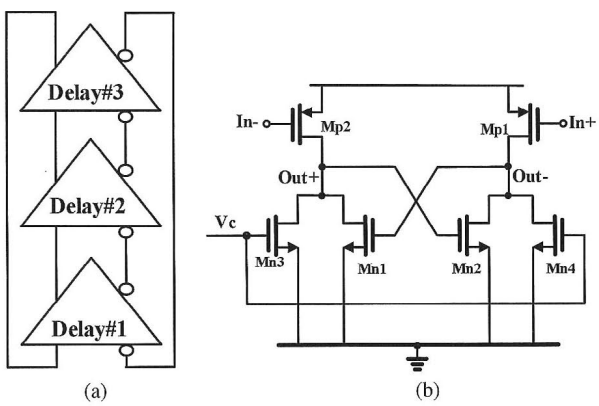


Fig. 8 (a) VCO circuits and (b) delay cell used in VCO.

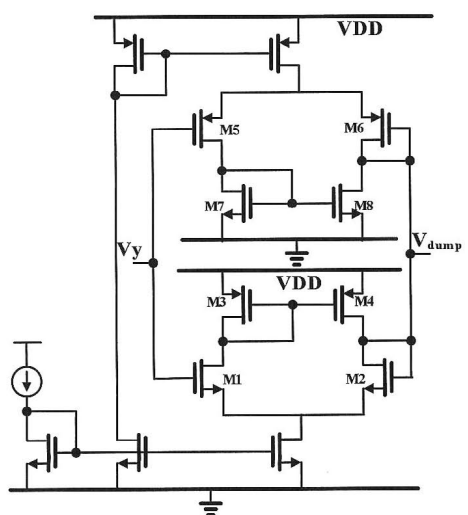


Fig. 9 Unity gain buffer circuit used in dual-path loop filter.

4. Measurement

The TPDL-SSCG is designed and fabricated by TSMC 0.35 μm single-poly quadruple-metal CMOS process. The die photograph is shown in Fig. 10 with area equal to $0.90 \times 0.89\ mm^2$. The output spectrum without spreading is shown

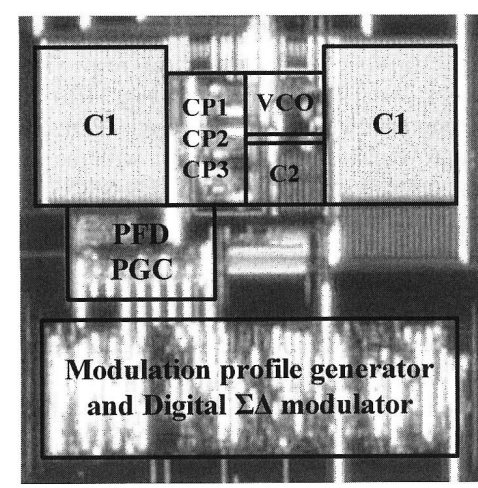
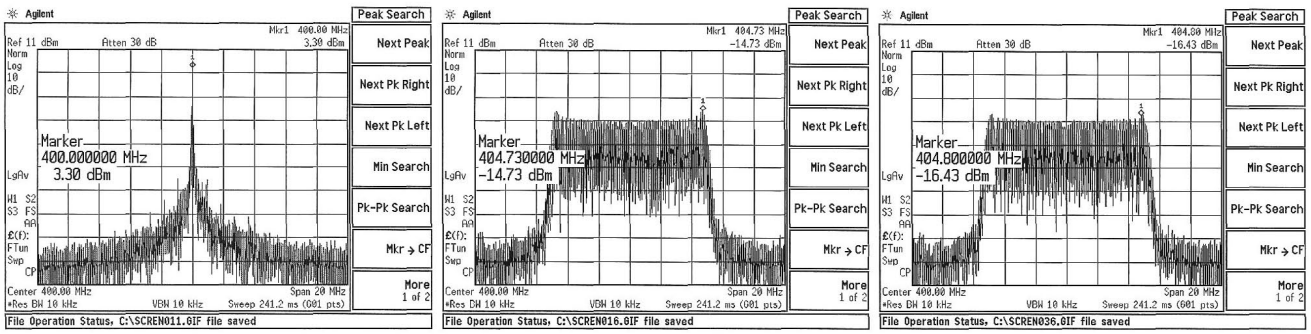
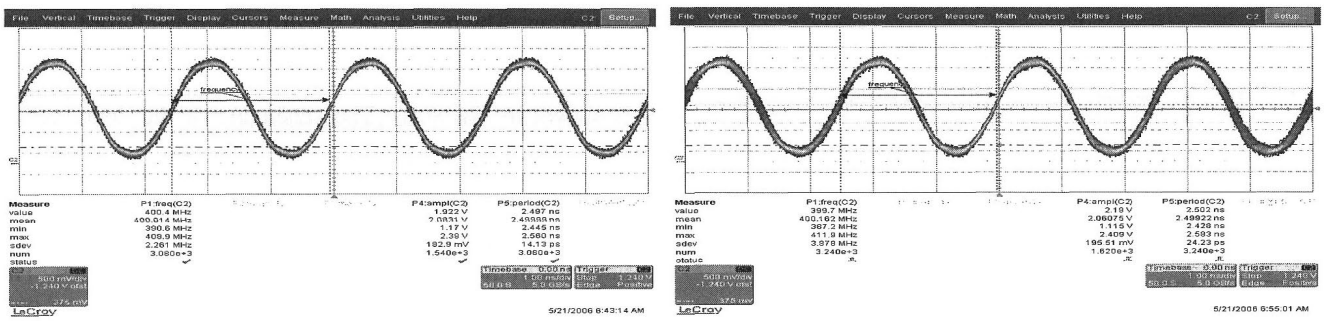


Fig. 10 The TPDL-SSCG die photograph.



(a) (b) (c)

Fig. 11 Measured spectra of 400 MHz output frequency (a) at non-spread spectrum mode, (b) of the conventional SSCG with 2.5% spread ratio, and (c) of the TPDL-SSCG with 2.5% spread ratio.



(a) (b)

Fig. 12 Measured period jitter of 400 MHz output frequency (a) at non-spread spectrum mode, and (b) of the TPDL-SSCG with 2.5% spread.

in Fig. 11(a) with clock speed at 400 MHz. The amplitude of the peak is 3.30 dBm. The output spectra using a traditional FN-SSCG and the proposed TPDL-SSCG with 2.5% spread ratio are shown in Figs. 11(b) and (c), respectively. A second-order loop filter and a PLL bandwidth close to 70 kHz are chosen for both Figs. 11(b) and (c). The second-order extended range MASH $\Sigma\Delta$ modulator is adopted for both Figs. 11(b) and (c). In other words, the traditional FN-SSCG is obtained just by switching off the path of VCO modulation. The amplitudes are reduced to −14.73 dBm and −16.43 dBm for Figs. 11(b) and (c), respectively. The peak reductions are about 18.03 dB and 19.73 dB with respect to that in Fig. 11(a) for Figs. 11(b) and (c), respectively. Two small peaks still exist at the edges in Fig. 11(b) due to insufficient loop bandwidth. The proposed TPDL-SSCG has 1.70 dB improvement in EMI reduction with the same loop bandwidth compared to the traditional FN-SSCG. The measured rms period jitter is 14.13 ps at non-spread spectrum mode as shown in Fig. 12(a). The measured rms period jitter is 24.23 ps for the TPDL-SSCG with 2.5% spread ratio as shown in Fig. 12(b). Only a 10.10 ps rms period jitter is increased when the SSCG is in active which is very close to the theoretical estimation of 10.42 ps (= 2.5% × 2500 ps/6). Table 2 gives the performance summaries of the TPDL-SSCG. The total power consumption is 33 mW.

Table 2 Performance summaries.

Modulation Method	Two point
Modulation Type	Center-spread
Modulation Frequency	40kHz
Spread Ratios(pp)	1.25%, 2.5%
Output Frequency	400MHz
VCO Gain	200MHz/V
Input Frequency	14.31818MHz
Loop bandwidth	~70kHz
Loop filter	R_1=12KΩ C_1=400pF C_2=40pF
Charge Pump Current	Ip_1=5uA
EMI reduction	19.73dB @ 2.5% center spread ratio
Chip Area (active)	0.90x0.89 mm^2
Power Dissipation	33mW including output buffer @ 3.0V

5. Conclusion

In this study, the spread spectrum clock generator with two-point modulation scheme is presented. The loop bandwidth of the PLL can be small but the modulation bandwidth is effectively expanded. This feature gives us the advantages of the linear modulation profile and using the lower order sigma-delta modulator without quantization noise penalty. Another advantage is the total integration without using an external loop filter. A novel configuration for replacing the high resolution DAC in triangular waveform generation is realized, which not only saves the area but also suppresses

the digital spur at the highly sensitive VCO input. The improvement of EMI reduction is better than 1.7 dB with respect to the conventional one.

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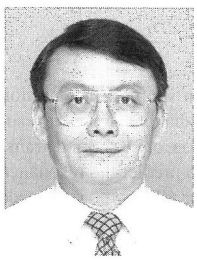

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