Impact of MOSFET Gate-Oxide Reliability on CMOS Operational Amplifier in a 130-nm Low-Voltage Process

Ming-Dou Ker, *Fellow, IEEE*, and Jung-Sheng Chen

***Abstract*—The effect of the MOSFET gate-oxide reliability on operational amplifier is investigated with the two-stage and folded-cascode structures in a 130-nm low-voltage CMOS process. The test operation conditions include unity-gain buffer (close-loop) and comparator (open-loop) configurations under the dc stress, ac stress with dc offset, and large-signal transition stress. After overstress, the small-signal parameters, such as small-signal gain, unity-gain frequency, and phase margin, are measured to verify the impact of gate-oxide reliability on circuit performances of the operational amplifier. The gate-oxide reliability in the operational amplifier can be improved by the stacked configuration under small-signal input and output application. The impact of soft and hard gate-oxide breakdowns on operational amplifiers with two-stage and folded-cascode structures has been analyzed and discussed. The hard breakdown has more serious impact on the operational amplifier.**

***Index Terms*—Analog circuit, dielectric breakdown, gate-oxide reliability, MOSFETs, operational amplifier.**

I. Introduction

THE REDUCTION of power consumption has become increasingly important to portable products, such as mobile phone, notebook, and flash memory. In general, the most common and efficient way to reduce the power consumption in CMOS very large scale integrated (VLSI) circuits is to reduce the power-supply voltage. To reduce the power consumption in CMOS VLSI systems, the standard supply voltage trends to scale down from 5 to 1 V. Thus, the gate-oxide thickness of the MOS transistor will become thin to reduce nominal operation voltage (power-supply voltage). In modern CMOS VLSI circuits including digital signal processor and embedded analog circuitry, the digital circuits are generally implemented by using thin-oxide devices. However, analog circuitry needs to be operated at a higher supply voltage than the nominal supply voltage of thin-oxide devices to achieve a wide dynamic range performance or to meet the compatibility requirement with standardized protocols from previous generations [1]. Some design technique to implement the high-voltage tolerance of analog circuits in nanoscale CMOS technology has been reported [1]. In general, the VLSI productions have a lifetime of more than ten years, but the thin gate oxide of the MOS transistor has many problems, such as gate-oxide breakdown, tunneling current, and hot carrier effect, that will degrade the lifetime of the MOS transistor. Therefore, to improve the gate-oxide reliability of MOS transistor and to investigate the effect of gate-oxide breakdown on CMOS circuit performances will become more important in the nanometer CMOS technology.

The occurrence of gate-oxide breakdown during the lifetime of CMOS circuits cannot be completely ruled out. The exact extrapolation of time to breakdown at circuit operating conditions is still difficult, since the physical mechanism governing the MOSFET gate dielectric breakdown is not yet fully modeled. It was less of a problem for old CMOS technologies, which have the thick gate oxide. However, because the probability of gate-oxide reliability strongly increases with the decrease of gate-oxide thickness [2], [3], the CMOS circuits in nanoscale technologies could be insufficiently reliable.

The defect generation leading to gate-oxide breakdown and the nature of the conduction after gate-oxide breakdown have been investigated [2]–[12], which point out that the gate-oxide breakdown will degrade the small-signal parameters of the MOS transistor, such as tranconductance g_m and threshold voltage V_{TH}. Recently, some studies on the impact of MOSFET gate-oxide breakdown on circuits have been reported [4]–[12]. In [4], it was demonstrated that the digital complementary logic circuits would remain functional beyond the first gate-oxide hard breakdown. A soft gate-oxide breakdown event in the CMOS digital dynamic logic circuits relying on the uncorrected soft nodes may result in the failure of the circuit [5]. The gate-oxide breakdown on RF circuits was also studied [6]. The impact of gate-oxide breakdown on CMOS differential amplifier and digital complementary logic circuits had been simulated [13]. The impact of gate-oxide breakdown on circuit performances of common-source amplifier had been investigated [14]. Some designs of analog circuits [15], [16] and the mixed-voltage I/O interface [17] indicate that gate-oxide reliability is a very import design consideration in CMOS circuits. The performances of analog circuits strongly depend on the I–V characteristics of MOSFET devices, because the small-signal parameters of MOSFET device are determined

Manuscript received October 14, 2007; revised January 28, 2008. This work was supported by the National Science Council, Taiwan, R.O.C., under Contract NSC 96-2221-E-009-182.

M.-D. Ker is with the Nanoelectronics and Gigascale Systems Laboratory, Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: mdker@ieee.org).

J.-S. Chen was with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. He is now with the Power Conversion Taiwan, Fairchild Semiconductor Corporation, Hsinchu 300, Taiwan, R.O.C.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TDMR.2008.922016

1530-4388/$25.00 © 2008 IEEE

by the biasing voltage and current of MOSFET devices. The small-signal gain and frequency response of analog circuits in CMOS processes are determined by the transconductance g_m and output resistance r_o of MOSFET devices. The transconductance g_m and output resistance r_o of MOSFET device can be expressed as

$$g_m = \mu C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{TH}}) = \frac{2I_D}{(V_{\mathrm{GS}} - V_{\mathrm{TH}})} \quad (1)$$

$$r_o = \frac{V_A}{I_D} \quad (2)$$

where μ is the mobility of carrier, L denotes the effective channel length, W is the effective channel width, C_{ox} is the gate-oxide capacitance per unit area, V_{TH} is the threshold voltage of MOSFET device, V_{GS} is the gate-to-source voltage of MOSFET device, V_A is the Early voltage, and the current I_D is the drain current of MOSFET device. Comparing (1) and (2), the drain current I_D is the key design factor for analog circuits in CMOS process. Therefore, the performances of analog circuits in CMOS processes are dominated by the drain currents of MOSFET devices. The drain current I_D of a MOSFET device operated in saturation region can be expressed as

$$I_D = \frac{1}{2}\mu C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2. \quad (3)$$

The channel-length modulation and body effect of MOSFET devices are not included in (3). The threshold voltage and gate-to-source voltage of MOSFET device are the important design parameters in (3). However, the gate-oxide overstress of MOSFET will cause degradation on the device characteristics of MOSFET. Therefore, the gate-oxide breakdown will have serious impact on the performances of analog circuits in the nanoscale CMOS technology. However, the impact of MOSFET gate-oxide breakdown on the CMOS operational amplifier circuits is still not well studied and really verified in a silicon chip. The CMOS analog circuits are very sensitive to the small-signal parameters of MOSFET, such as tranconductance g_m and threshold voltage V_{TH}. Therefore, the gate-oxide breakdown is expected to have severe impact on the circuit performances of analog circuits.

In this paper, the effect of MOSFET gate-oxide reliability on the operational amplifiers with the two-stage (nonstacked) and folded-cascode (stacked) structures is investigated in a 130-nm low-voltage CMOS process [18]. The small-signal gain, phase margin, unity-gain frequency, and power supply rejection ratio (PSRR) of these operational amplifiers with different configurations are measured and compared after different stresses.

II. Analog Circuits

The operational amplifier is a basic unit in many analog circuits and systems, such as output buffer, sample-and-hold circuit, and analog-to-digital converter. The operational amplifiers with the two-stage and folded-cascode structures are selected to verify the impact of MOSFET gate-oxide reliability on analog circuits. The complete circuits of the operational amplifiers are shown in Fig. 1(a) and (b). The operational amplifier with the two-stage structure comprises the differential amplifier $(M_1 - M_5)$, common-source amplifier $(M_6 - M_7)$, source follower $(M_8 - M_9)$, and bias circuit $(M_{B1} - M_{B4})$. The operational amplifier with the folded-cascode structure comprises the differential amplifier $(M_{10} - M_{20})$ and the bias circuit $(M_{B5} - M_{B16})$. The operational amplifiers with the two-stage and folded-cascode structures have been fabricated in a 130-nm low-voltage CMOS process. The test dies have been packaged by DIP 40-pin package and measured on a print circuit board (PCB). The normal operating voltage and the gate-oxide thickness (t_{ox}) of all MOSFET devices in these operational amplifiers are 1 V and 2.5 nm, respectively. The channel lengths of NMOS and PMOS transistors in the two operational amplifiers are set to 0.5 and 1 μm, respectively, to avoid the short-channel effects such as threshold variation, drain-induced barrier lowering effect, hot-carrier effect, velocity saturation, and mobility degradation effect. The body terminals of all the NMOS and PMOS transistors are connected to ground and power supply voltage, respectively. The device dimensions of two amplifiers are shown in Table I. This design approach is usually used to design the operational amplifier in analog integrated circuit applications.

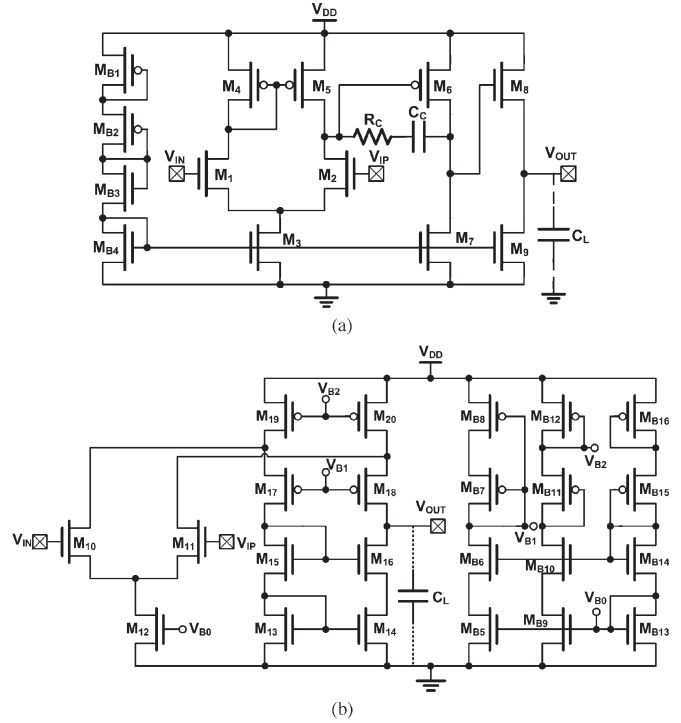


Fig. 1. Complete circuits of the operational amplifiers with the (a) two-stage and (b) folded-cascode circuit structures.

In signal MOSFET device, if the critical terminal voltage of the device, such as gate-to-source voltage (V_{GS}), gate-to-drain voltage (V_{GD}), and drain-to-source voltage (V_{DS}), is kept within the normal operating voltage V_{DD} of the technology, the electric fields across the MOS device will not cause the damage on the gate oxide. Therefore, the bias circuit of the operational amplifiers is designed with a stacked structure to

TABLE I
DEVICE DIMENSIONS OF OPERATIONAL AMPLIFIERS WITH THE TWO-STAGE OR FOLDED-CASCODE STRUCTURES

Device	Dimension	Device	Dimension	Device	Dimension
M_1	12.5μ/0.5μ	M_{13}	2μ/0.5μ	M_{B5}	4μ/0.5μ
M_2	12.5μ/0.5μ	M_{14}	2μ/0.5μ	M_{B6}	4μ/0.5μ
M_3	1μ/0.5μ	M_{15}	1μ/0.5μ	M_{B7}	0.98μ/0.5μ
M_4	2μ/0.5μ	M_{16}	1μ/0.5μ	M_{B8}	1.1μ/0.5μ
M_5	2μ/0.5μ	M_{17}	4μ/0.5μ	M_{B9}	4μ/0.5μ
M_6	4μ/1μ	M_{18}	4μ/0.5μ	M_{B10}	4μ/0.5μ
M_7	1μ/1μ	M_{19}	4μ/0.5μ	M_{B11}	2μ/0.5μ
M_8	15μ/0.5μ	M_{20}	4μ/0.5μ	M_{B12}	2μ/0.5μ
M_9	1.8μ/1μ	M_{B1}	10μ/1μ	M_{B13}	4μ/0.5μ
M_{10}	25μ/0.5μ	M_{B2}	10μ/1μ	M_{B14}	4μ/0.5μ
M_{11}	25μ/0.5μ	M_{B3}	1μ/0.5μ	M_{B15}	2.8μ/1μ
M_{12}	8μ/0.5μ	M_{B4}	1μ/0.5μ	M_{B16}	2.8μ/1μ

avoid the gate-oxide breakdown. The Miller-compensated capacitance C_C of the two-stage operational amplifier in Fig. 1(a) is realized by the metal–insulator–metal structure, which has no gate-oxide reliability problem. The impact of MOSFET gate-oxide reliability on the operational amplifiers with the two-stage and folded-cascode structures is verified by using continuous stress with supply voltage of 2.5 V. The input common-mode voltage of the operational amplifiers is set to 1.25 V. Simulated by HSPICE, the open-loop gain and phase margin of the operational amplifier with the two-stage structure are 64.7 dB and 47.8°, respectively, under output capacitive load of 10 pF. The open-loop gain and phase margin of another operational amplifier with the folded-cascode structure are 61.9 dB and 89°, respectively, under output capacitive load of 10 pF. The open-loop small-signal gain $(A_{V_\text{two-stage}})$ of the operational amplifier with the two-stage structure is given by

$$A_{V_\text{two-stage}}(S) \cong \frac{g_{m1}g_{m6}g_{m8}}{g_{\text{ox}}g_{\text{oy}}g_{\text{oz}}} \frac{1-SC_C/g_{m6}}{(1-SC_L/g_{\text{oz}})(g_{\text{oy}}+g_{m6}SC_L)} \quad (4)$$

where the g_o and g_m are the output conductance and transconductance of the corresponding MOSFET in the operational amplifiers. The g_{ox}, g_{oy}, and g_{oz} are equal to $g_{o5}+g_{o2}$, $g_{o6}+g_{o7}$, and $g_{o8}+g_{o9}$, respectively. The open-loop small-signal gain $(A_{V_\text{folded-cascode}})$ of the operational amplifier with the folded-cascode structure is also written as

$$A_{V_\text{folded-cascode}}(S) \cong \frac{g_{m11}R_o}{1+SC_LR_o} \quad (5)$$

$$R_o = \frac{1}{\frac{g_{o11}+g_{o20}}{g_{m18}r_{o18}} + \frac{g_{o14}}{g_{m16}r_{o16}}} \quad (6)$$

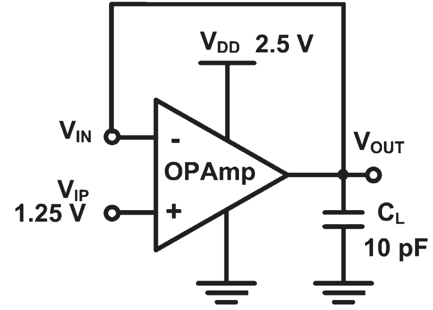


Fig. 2. Unity-gain buffer configuration for operational amplifiers under dc stress to investigate the impact of gate-oxide reliability to circuit performances.

where r_o is the output resistance of the corresponding MOSFET in the operational amplifiers. The short-channel effect, body effect, and parasitic capacitance of MOS transistors in the two operational amplifiers are ignored in (4)–(6). The capacitances C_L and C_C are the output capacitive load and Miller-compensated capacitance, respectively, in the two operational amplifiers.

III. OVERSTRESS TEST

The operational amplifiers with the close-loop (unity-gain buffer) and open-loop (comparator) configurations are selected to verify the impact of MOSFET gate-oxide reliability on the circuit performances of the operational amplifiers with the two-stage and folded-cascode structures in a 130-nm low-voltage CMOS process. The small-signal gain, phase margin, output-signal swing, PSRR, and rise and fall times of the operational amplifiers varied with gate-oxide breakdown will be measured and analyzed. Because the MOSFET devices in analog circuits usually work in the saturation region, the gate-oxide breakdown is more likely to occur as the conventional time-dependent dielectric breakdown. High gate-to-source voltage (V_{GS}), gate-to-drain voltage (V_{GD}), and drain-to-source voltage (V_{DS}) of the MOSFET are used to get a fast and easy-to-observe breakdown occurrence for investigating the impact of the gate-oxide reliability on the operational amplifiers. The advantages of using static stress are the well-defined distributions of the voltages on the devices in the operational amplifiers and the better understanding of the consequences of this overstress. The stress and measurement supply voltage V_{DD} in operational amplifier with two-stage and folded-cascode structures are set to 2.5 V. After overstress, the small-signal parameters of the operational amplifiers with the two-stage and folded-cascode structures are reevaluated under the same operation condition. The test operation conditions include unity-gain buffer (close-loop) and comparator (open-loop) configurations under the dc stress, ac stress with dc offset, and large-signal transition stress.

A. Unity-Gain Buffer (DC Stress)

The operational amplifiers with the two-stage and folded-cascode structures under the configuration of the unity-gain buffer are continuously tested in this dc stress, as shown in Fig. 2. The output node of the operational amplifiers is

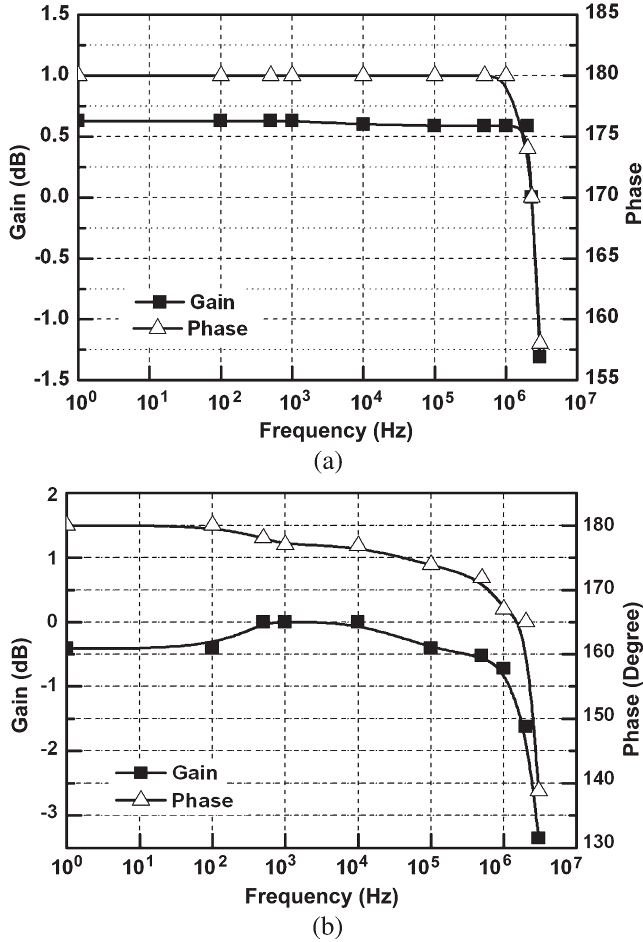


Fig. 3. Fresh frequency responses of the operational amplifiers with the (a) two-stage and (b) folded-cascode structures operating in the unity-gain buffer.

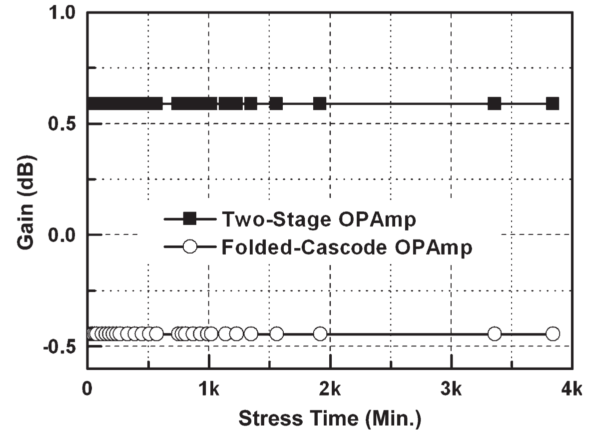


Fig. 4. Dependence of the small-signal gain on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the dc stress.

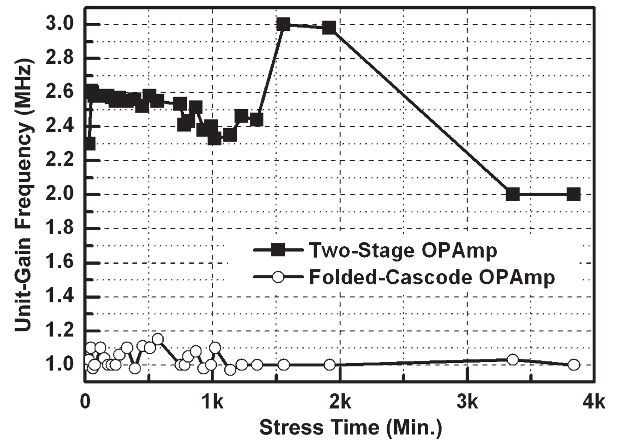


Fig. 5. Dependence of the unity-gain frequency on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the dc stress.

connected to the inverting input node to form the configuration of a unity-gain buffer. According to the basic negative-feedback theory, the close-loop small-signal gain of the operational amplifiers with the two-stage and folded-cascode structures under the unity-gain buffer configuration can be expressed as

$$A_{fV_\mathrm{two-stage}}(S) = \frac{A_{V_\mathrm{two-stage}}(S)}{1 + A_{V_\mathrm{two-stage}}(S)} \tag{7}$$

$$A_{fV_\mathrm{folded-cascode}}(S) = \frac{A_{V_\mathrm{folded-cascode}}(S)}{1 + A_{V_\mathrm{folded-cascode}}(S)} \tag{8}$$

where $A_{V_\mathrm{two-stage}}(S)$ and $A_{V_\mathrm{folded-cascode}}(S)$ are shown in (4) and (5), respectively. The small-signal gain, unity-gain frequency, and phase margin of the operational amplifier with the two-stage structure operating in a unity-gain buffer are 0.48 dB, 2.3 MHz, and 168°, respectively, under output capacitive load of 10 pF. Those of the operational amplifier with the folded-cascode structure operating in a unity-gain buffer are −0.4 dB, 1 MHz, and 163°, respectively, under output capacitive load of 10 pF. The noninverting node of the operational amplifiers is biased at 1.25 V, the output capacitive load is set to 10 pF, and the supply voltage V_{DD} is set to 2.5 V. The measured results of the fresh frequency responses before any stress are shown in Fig. 3(a) and (b), where the operational amplifiers operate in the unity-gain buffer.

During this dc overstress, the small-signal gain, unity-gain frequency, phase margin, offset voltage, PSRR, and rise and fall times of the operational amplifiers will be measured under the unity-gain buffer configuration. When those parameters are measured, the input signal of 1.25 V at the noninverting node (V_{IN}) is replaced by the ac small signal of 200-mV sinusoid signal (peak-to-peak amplitude) with a dc common-mode voltage of 1.25 V. The dependence of the small-signal gain on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the dc stress is shown in Fig. 4. The close-loop small-signal gain of the operational amplifiers with the two-stage and folded-cascode structures under the dc stress is not changed, even though the stress time is up to 4000 min. The dependence of the unity-gain frequency on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the dc stress is shown in Fig. 5. The unity-gain frequency of the operational amplifier with the two-stage structure under the

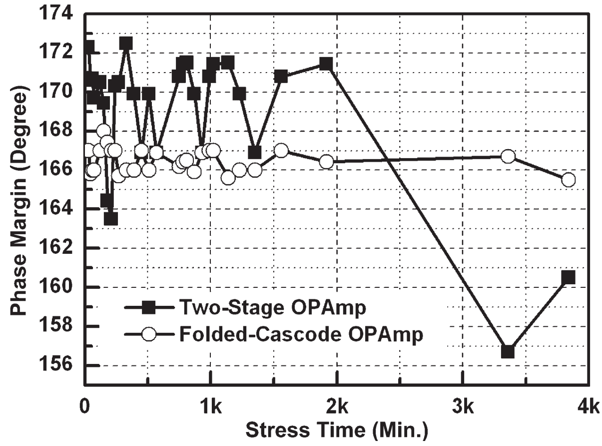


Fig. 6. Dependence of the phase margin on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the dc stress.

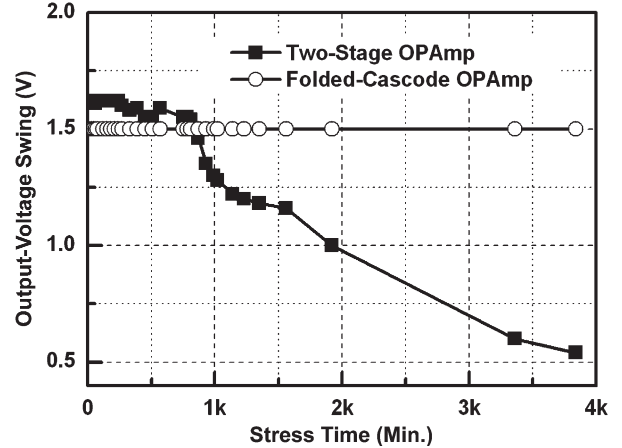


Fig. 7. Dependence of the output-voltage swing on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the dc stress.

dc stress is decreased, but that of the operational amplifier with the folded-cascode structure is not obviously changed under the same stress condition. The impact of MOSFET oxide breakdown on circuit behavior will cause the extra gate leakage, threshold voltage (V_{TH}) shift, and reduced transconductance (g_m) to degrade circuit performances. The threshold voltage (V_{TH}) shift of MOSFET will change its I–V characteristic. The oxide breakdowns on different MOSFET devices will have different impacts on the circuit performance under negative feedback configuration. The dependence of the phase margin on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the dc stress is shown in Fig. 6. The phase margin of the operational amplifier with the two-stage structure under the dc stress is decreased, but that of the operational amplifier with the folded-cascode structure is not obviously changed. The degradation on the small-signal performances in the operational amplifier with the two-stage structure under the dc stress can be explained that the gate-oxide breakdown will degrade the tranconductance g_m and threshold voltage V_{TH} of MOS transistor. In (4), the g_m and V_{TH} parameters are the principal factors, which dominate the small-signal gain, pole, and zero of the operational amplifier with the two-stage structure. Therefore, if the g_m and V_{TH} parameters are degraded with the stress, the small-signal performances of the operational amplifier with the two-stage structure will be changed under the unity-gain buffer configuration.

The dependence of the output-voltage swing on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the dc stress is shown in Fig. 7. The output-voltage swing of the operational amplifier with the two-stage structure under the dc stress is decreased, but that of the operational amplifier with the folded-cascode structure is not changed. The maximum output-signal swing of the operational amplifier with the two-stage structure under the unity-gain buffer configuration can be written as

$$V_{\mathrm{DS_sat}(M8)} \leq V_{\mathrm{out}} \leq V_{\mathrm{DD}} - V_{\mathrm{DS_sat}(M9)} \tag{9}$$

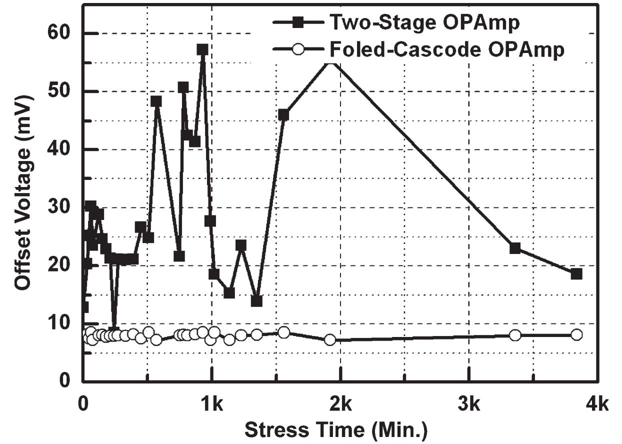


Fig. 8. Dependence of the offset voltage on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the dc stress.

where the $V_{\mathrm{DS_sat}}$ is the overdrive voltage $(V_{\mathrm{GS}} - V_{\mathrm{TH}})$. The gate-oxide degradation will degrade the threshold voltage V_{TH}, so the output-signal swing of the operational amplifier with the two-stage structure operating in unity-gain buffer will be degraded with the overstress under the dc stress.

The input dc offset voltage of operational amplifiers operating in the unity-gain buffer can be measured from the voltage difference between the inverting and noninverting nodes of the operational amplifiers, when the input pin (V_{IN}) is set to a common-mode voltage of 1.25 V. The dependence of the input dc offset voltage on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the dc stress is shown in Fig. 8. The offset voltage of the operational amplifier with the two-stage structure under the dc stress is increased, but that of the operational amplifier with the folded-cascode structure is not changed. The input dc offset voltage (V_{OS}) of the operational amplifier is caused by the MOS device mismatch and finite-gain error, which correspond to the V_{OS1} and V_{OS2}, respectively, under the unity-gain buffer configuration. The input dc offset

voltage of the operational amplifier under the unity-gain buffer configuration can be expressed as

$$V_{\mathrm{OS}} = V_{\mathrm{OS1}} + V_{\mathrm{OS2}} \quad (10)$$

$$V_{\mathrm{OS1}} = \frac{V_{\mathrm{GS}(M1)} - V_{\mathrm{TH}(M1)}}{2} \times \left[\frac{\Delta\left(\frac{W}{L}\right)_{(M1,M2)}}{\left(\frac{W}{L}\right)_{(M1,M2)}} + \frac{\Delta\left(\frac{W}{L}\right)_{(M4,M5)}}{\left(\frac{W}{L}\right)_{(M4,M5)}} \right] - \Delta V_{\mathrm{TH}(M1,M2)} \quad (11)$$

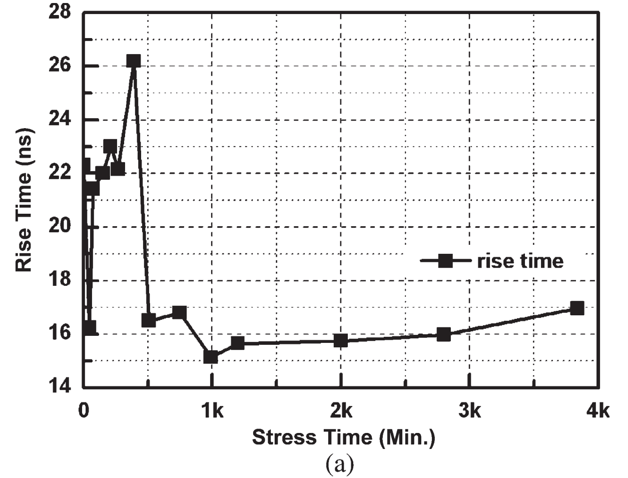
$$V_{\mathrm{OS2}} = \frac{V_{\mathrm{out}}}{A_{V_\mathrm{two-stage}}(0)}. \quad (12)$$

The dc offset voltage V_{OS1} is caused by MOS transistor mismatch of differential amplifier. The dc offset voltage V_{OS2} is caused by the finite small-signal gain of the operational amplifier. The dc offset voltage V_{OS1} plus V_{OS2} equals the total input dc offset voltage V_{OS}. In this case, only the impact of MOSFET gate-oxide degradation on the offset voltage V_{OS2} will be considered in the operational amplifier with the two-stage structure, because the differential pair of the two-stage operational amplifier is not degraded with the overstress. The impact of MOSFET oxide breakdown on circuit behavior will cause the extra gate leakage, threshold voltage (V_{TH}) shift, and reduced transconductance (g_m) to degrade circuit performances. The oxide breakdowns on different MOSFET devices will cause different impacts on the circuit performance under negative feedback configuration. The dc offset voltage V_{OS2} is inversely proportional to $A_{V_\mathrm{two-stage}}(0)$ in (4). However, the $A_{V_\mathrm{two-stage}}(0)$ of the operational amplifier with the two-stage structure will be degraded by gate-oxide degradation, so the input dc offset voltage will be degraded with gate-oxide degradation under the dc stress.

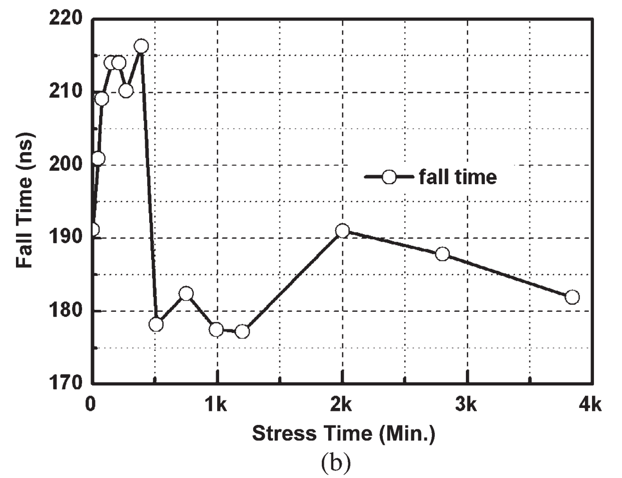
About the measurement setup for output-signal rise and fall times of the operational amplifiers operating in the unity-gain buffer, the square voltage signal from 1 to 1.5 V is applied to the input pin to measure the rise and fall times of the signal at output pin. The rise and fall times are defined as the times of the output-signal rise and fall edges from 10% to 90%, when the square waveform of input signal has the rise and fall times of 1 ns. The dependence of the rise and fall times on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the dc stress is shown in Fig. 9(a)–(c). The rise and fall times of the operational amplifier with the two-stage structure under the dc stress are obviously changed, but those of the operational amplifier with the folded-cascode structure are not changed. The rise and fall times of the operational amplifier with the two-stage structure can be expressed as

$$T_{\mathrm{rise}} \cong \frac{C_L}{I_{\mathrm{DM8}}} \quad (13)$$

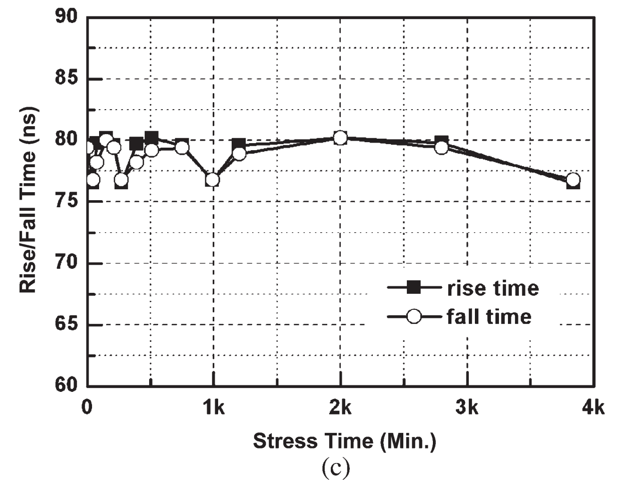
$$T_{\mathrm{fall}} \cong \frac{C_L}{I_{\mathrm{DM9}}} \quad (14)$$



(a)



(b)



(c)

Fig. 9. Dependence of the rise and fall times on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the dc stress. (a) and (b) Two-stage operational amplifier. (c) Folded-cascode operational amplifier.

where the I_{DM8} and I_{DM9} are the drain currents of MOS transistors M_8 and M_9, respectively. The drain current of MOS transistor in the saturation region can be written as

$$I_D = K_n \left(\frac{W}{L}\right) (V_{\mathrm{GS}} - V_{\mathrm{TH}})^2 \quad (15)$$

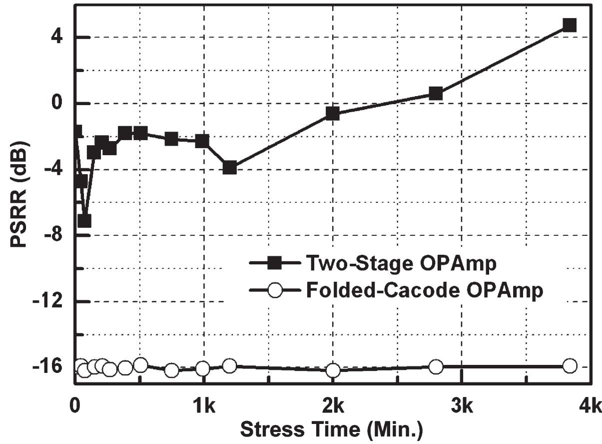


Fig. 10. Dependence of the PSRR on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the dc stress.

where the K_n is the tranconductance of MOS transistor and the W/L is the MOS transistor dimension ratio. In the (13) and (14), the rise and fall times of the operational amplifier with the two-stage structure are dominated by the drain current of MOS transistor, which is dependent on threshold voltage V_{TH} in (15). The gate-oxide degradation will degrade the threshold voltage V_{TH} of the MOS transistor, so the rise and fall times of the operational amplifier with the two-stage structure will be changed under the dc stress.

In the measurement setup for PSRR, a sinusoidal ripple of 100 mV is added to the power supply to measure the small-signal gain between the supply voltage and output pin voltage (V_{OUT}). The ac input signal at the power supply pin must include a dc bias that corresponds to the normal power supply voltage (2.5 V), so that the operational amplifiers operating in the unity-gain buffer remain powered up. The dependence of the PSRR on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the dc stress is shown in Fig. 10. The PSRR of the operational amplifier with the two-stage structure under the dc stress is obviously changed, but that of the operational amplifier with the folded-cascode structure is not changed. The PSRR of the operational amplifier with the two-stage structure under the unity-gain buffer configuration can be simply expressed as

$$\mathrm{PSRR} = \frac{V_{\mathrm{out}}}{V_{\mathrm{DD}}} \cong \frac{r_{oM8}}{r_{oM8} + r_{oM9}} \tag{16}$$

$$r_o = \frac{V_A}{I_D} \tag{17}$$

where the V_A is the early voltage of the MOS transistor. The small-signal output resistance depends on the drain current in the MOS transistor. Therefore, the gate-oxide degradation will degrade the PSRR of the operational amplifier with the two-stage structure under the unity-gain buffer configuration during the dc stress.

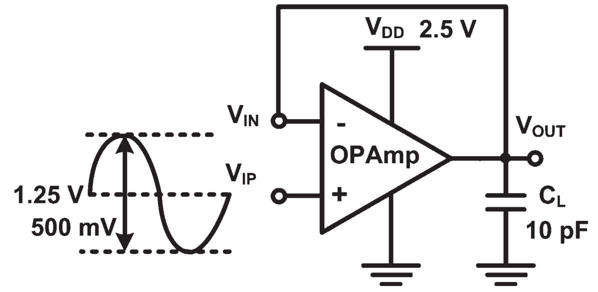


Fig. 11. Unity-gain buffer configuration for operational amplifiers under the stress of ac small-signal input with dc offset to investigate the impact of gate-oxide reliability to circuit performances.

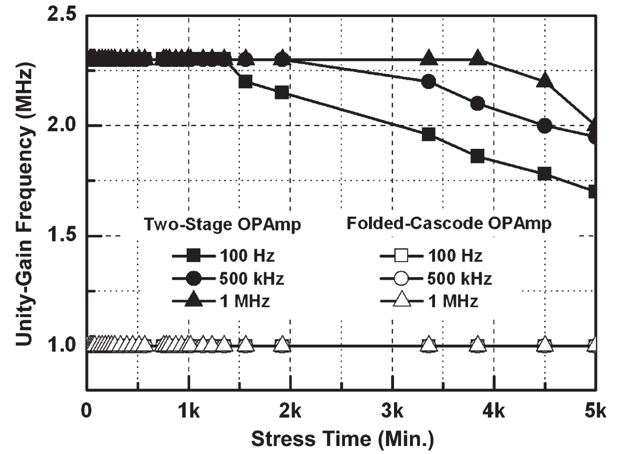


Fig. 12. Dependence of the unity-gain frequency on the stress time of the operational amplifiers with the two-stage or folded-cascode structures under the stress of the ac small-signal input with dc offset.

B. Unity-Gain Buffer (AC Stress With DC Offset)

The operational amplifiers under the configuration of the unity-gain buffer are continuously tested in the stress of the ac small-signal input with dc offset, as shown in Fig. 11. The noninverting node of the operational amplifiers with the two-stage and folded-cascode structures is biased by the ac sinusoidal signal of 500 mV (peak-to-peak amplitude) plus a dc offset voltage of 1.25 V with different frequencies of 100 Hz, 500 kHz, and 1 MHz. The output capacitive load is set to 10 pF, and the supply voltage V_{DD} is set to 2.5 V. The measurement setup is used to investigate the relationship between gate-oxide reliability and different frequencies of input signals in the CMOS analog circuit applications.

The dependence of the unity-gain frequency in the unity-gain buffers on the stress time under the stress of the ac small-signal input with dc offset is shown in Fig. 12. The performances of the operational amplifier with the folded-cascode structure are not degraded by the stress of the ac small-signal input with dc offset. In the operational amplifier with the two-stage structure, the high-frequency input signal causes a slow degradation on the unity-gain frequency, but the low-frequency input signal causes a fast degradation on the unity-gain frequency under the stress of the ac small-signal input with dc offset. The other small-signal performances in the operational amplifier with the

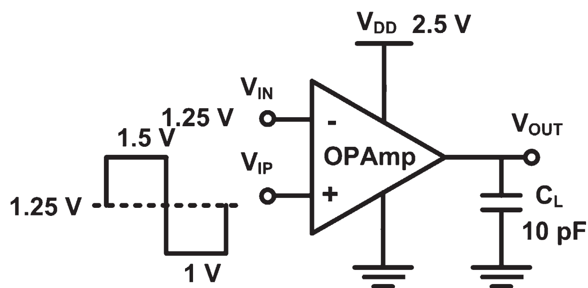


Fig. 13. Comparator configuration for operational amplifiers under the stress of large-signal transition to investigate the impact of gate-oxide reliability to circuit performances.

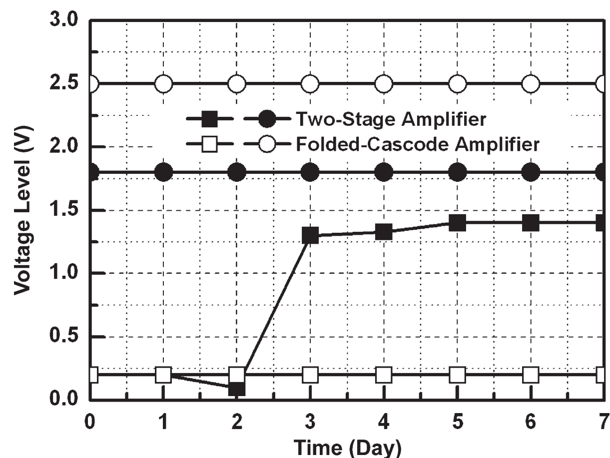


Fig. 14. Dependences of the high and low voltage levels at the output node on the stress time under stress of large-signal transition. The operational amplifiers with the two-stage or folded-cascode structures are stressed under the comparator configuration.

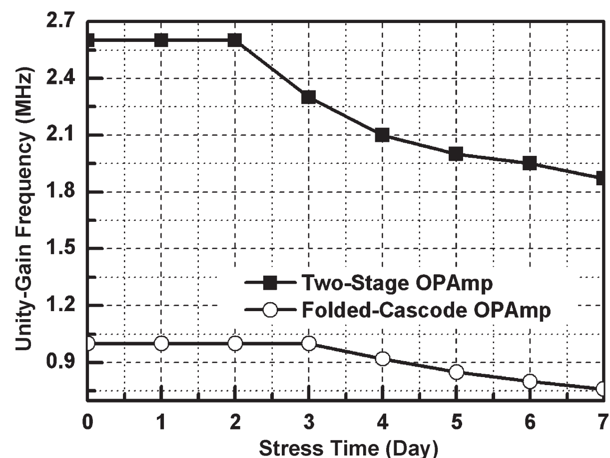


Fig. 15. Dependence of the unity-gain frequency on the stress time under the stress of large-signal transition. The operational amplifiers with the two-stage or folded-cascode structures are stressed under the comparator configuration.

two-stage structure under the stress of the ac small-signal input with dc offset have the same change trend as that under the dc stress, but the different frequencies of the input signal will cause the different degradation times. These measured results are consistent to that reported in [11]. The frequency dependence of t_{BD} (time to breakdown) is reasonably understood in terms of the redistribution of the breakdown species from the anodic interface toward the oxide bulk. These two different frequency regimes correspond to two extreme distributions. When the frequency is very high, the concentration of "breakdown species" is expected to be low. The distribution strongly peaked at both interfaces. This presumably explains the reduction of degradation. On the contrary, in the low frequency, concentration is expected to be high and to have a uniform distribution throughout the oxide film. This leads to the faster degradation process [11]. Therefore, the small-signal performance of the two-stage operational amplifier with different frequencies of the input signals will cause different degradation times under the stress of the ac small-signal input with dc offset.

C. Comparator (Large-Signal Transition)

The operational amplifiers under the comparator (open-loop) configuration are used to investigate the impact of gate-oxide reliability on CMOS analog circuits under the large-signal transition. The inverting input node of the operational amplifiers is biased at 1.25 V, the output capacitance load is set to 10 pF, and the supply voltage V_{DD} is set to 2.5 V. The operational amplifiers under the comparator configuration are continuously tested in this stress of large-signal transition, as shown in Fig. 13. The input square voltage waveform from 1 to 1.5 V with frequency of 100 Hz is applied to the noninverting input node of the operational amplifiers under the comparator configuration. The square waveform of input signal from 1 to 1.5 V will not induce the damage on the input devices of the operational amplifiers, because the voltages across the input devices (V_{GS}, V_{GD}, and V_{DS}) of the operational amplifiers are lower than the 1 V in this measurement.

The dependences of the high- and low-voltage levels at the output node on the stress time are shown in Fig. 14, where the operational amplifiers with the two-stage or folded-cascode structures in the comparator configuration are stressed by the large-signal transition. The low output voltage level of the operational amplifier with the two-stage structure under the stress of large-signal transition is increased when the stress time is increased. However, the high output voltage level of the operational amplifier with the two-stage structure is not changed after the same stress condition. The high and low voltage levels at the output node of the operational amplifier with the folded-cascode structure after the seven-day stress of large-signal transition are not changed. The dependence of the unity-gain frequency on the stress time under the stress of large-signal transition is shown in Fig. 15, where the operational amplifiers with the two-stage or folded-cascode structures are connected in the comparator configuration. The unity-gain frequency of the operational amplifiers with the two-stage and folded-cascode structures connected as unity-gain buffer is degraded after the stress of large-signal transition. The reason why the circuit performances of the operational amplifiers with the two-stage and folded-cascode structures, such as small-signal gain and unity-gain frequency, are degraded with the overstress is summed up being that the gate-oxide breakdown will degrade the transconductance (g_m), threshold voltage (V_{TH}), and

TABLE II
COMPARISONS OF OPERATIONAL AMPLIFIERS WITH THE TWO-STAGE OR FOLDED-CASCODE STRUCTURES AMONG THREE OVERSTRESS CONDITIONS

Stress Conditions	Performances	Two-Stage	Folded-Cascode
DC Stress	Small-Signal Gain	Seriously Degraded	No Change
	Unity-Gain Frequency	Seriously Degraded	No Change
	Output Voltage Swing	Seriously Degraded	No Change
AC Stress With DC Offset	Small-Signal Gain	• High Frequency → Slow Degraded Rate • Low Frequency → High Degraded Rate	No Change
Large-Signal Transition Stress	High and Low Output Voltage Levels	Seriously Degraded	No Change
	Unity-Gain Frequency	Seriously Degraded	Degraded

output conductance (g_o) of the MOS transistor. The approximate high and low output voltage levels of the operational amplifier with the two-stage and folded-cascode structures are near the $V_{\rm DD}$ and ground levels, respectively, under the comparator configuration. In this case, the $V_{\rm DD}$ level is set to 2.5 V, whereas the ground level is set to 0 V. The output-stage devices of the operational amplifiers with the two-stage and folded-cascode structures will be degraded with gate-oxide degradation, so the performances of the operational amplifiers with the two-stage and folded-cascode structures will be degraded under the large-signal transition stress.

IV. DISCUSSION

The summary of overstress results under three overstress conditions (dc, ac, and large-signal transition stresses) is listed in Table II. The gate-oxide breakdown will degrade the transconductance (g_m), output resistance (r_o), and threshold voltage $(V_{\rm th})$ of MOSFET devices. After the overstress, the performances of the two-stage operational amplifiers under close-loop and open-loop configurations are degraded. Because the differential amplifier of the operational amplifier with the two-stage structure consists of three cascode MOSFET devices, the voltages across the devices in the differential amplifier of the operational amplifier with the two-stage structure do not exceed 1 V under the stress with the input common-mode voltage of 1.25 V and supply voltage of 2.5 V. The differential amplifier of the operational amplifier with the two-stage structure is not degraded under the stresses with the supply voltage of 2.5 V. However, the output stage in the operational amplifier with the two-stage structure will be degraded under the stress with the input common-mode voltage of 1.25 V and supply voltage of 2.5 V. Therefore, the open-loop gain of the operational amplifier with the two-stage structure is decreased after the stresses. The offset voltage due to the finite gain error of the operational amplifier with the two-stage structure is increased after the stress.

The rise time, fall time, output voltage swing, and phase margin of the operational amplifier with the two-stage structure are also decreased after the stress. The gate-oxide reliability in the CMOS analog circuits can be improved by the stacked structure. The dc operating point is very important in the analog circuit design, because all small-signal parameters of the devices and circuits are determined by the dc operating point. If the dc operating point is changed after gate-oxide degradation, the analog circuits will not work correctly. However, the large-signal transition at input and output nodes of the operational amplifier with a stacked structure still causes some degradations on circuit performances of analog circuits. As a result, the analog circuits with a stacked structure are only effective to improve the gate-oxide reliability under small-signal applications at input and output nodes.

Under the same stress condition, the two-stage operational amplifier under close-loop (negative-feedback) configuration can be more easily stressed than that under the open-loop configuration. The close-loop configuration in the operational amplifiers is used to make the circuits stable and to keep the virtual short between inverting and noninverting nodes of the operational amplifiers. Therefore, the inverting, noninverting, and output nodes of the operational amplifiers have the same dc voltage level under the configuration of negative feedback. The transconductance (g_m), output resistance (r_o), and threshold voltage $(V_{\rm TH})$ of MOSFET devices will be changed after the stress. In order to make the circuits stable and to keep the virtual short between the two input nodes of the operational amplifier with the two-stage structure, the dc operating point of the output stage in the two-stage operational amplifier will be changed after the stress. Therefore, the power consumption (circuit performances) of the operational amplifier with the two-stage structure under the negative-feedback configuration will be increased (degraded) after the stress.

V. EFFECT OF HARD AND SOFT GATE-OXIDE BREAKDOWNS ON PERFORMANCES OF OPERATIONAL AMPLIFIER

A. DC Stress

The measured power supply current $I_{\rm VDD}$ of two-stage operational amplifier is jumped from 184 μA to over 300 μA, as shown in Fig. 16, after dc overstress. From such measurement, the oxide breakdown occurred in two-stage operational amplifier can be confirmed after dc overstress. After oxide breakdown, the measured output voltage swing waveform of operational amplifier with the two-stage structure after dc

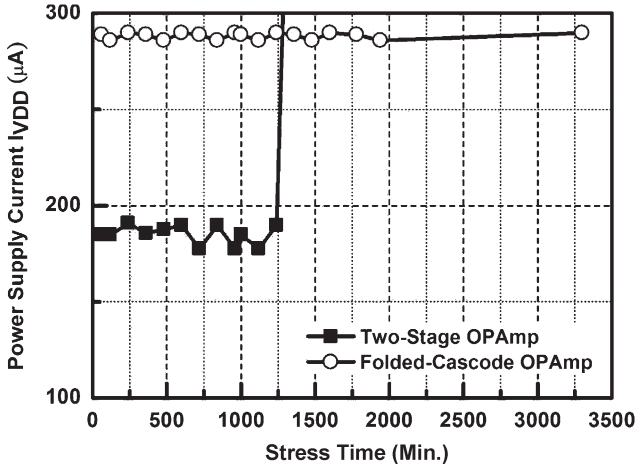


Fig. 16. Dependence of power supply current $I_{\rm VDD}$ of the operational amplifiers with the two-stage or folded-cascode structures on the stress time under dc stress.

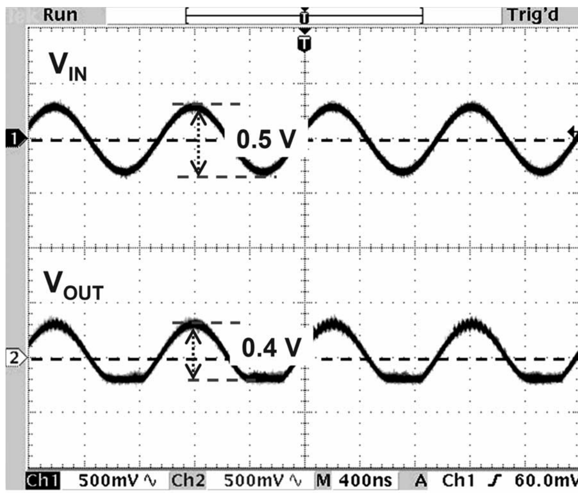


Fig. 17. Measured output voltage swing waveform of operational amplifier with the two-stage structure after dc stress.

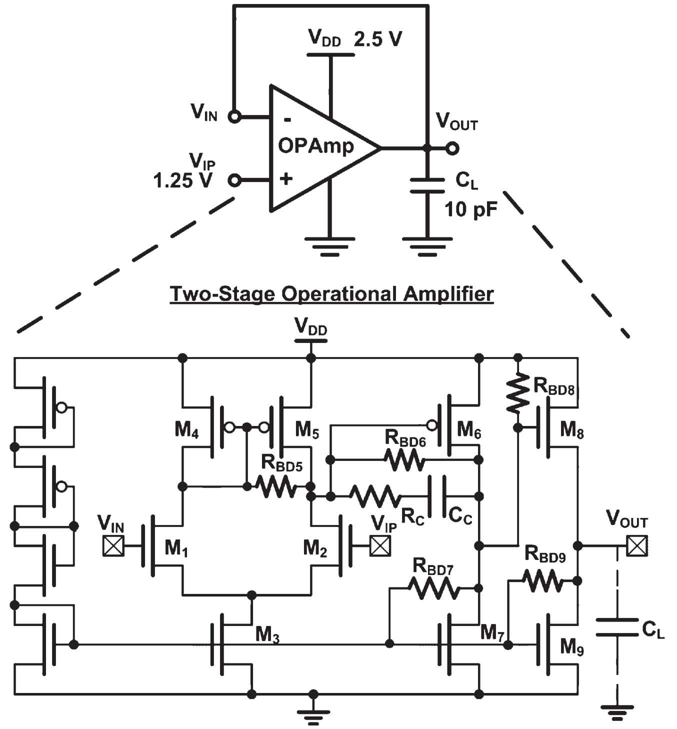


Fig. 18. Complete circuit of the operational amplifier with the two-stage structure including gate-oxide breakdown model under dc stress.

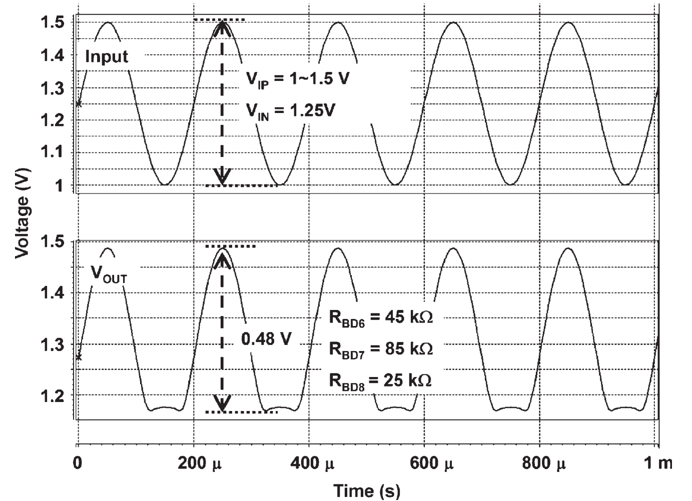


Fig. 19. Simulated output voltage swing waveform of operational amplifier with the two-stage structure under different breakdown resistances $R_{\rm BD6}$, $R_{\rm BD7}$, and $R_{\rm BD8}$.

stress, as shown in Fig. 2, is shown in Fig. 17. Based on the prior proposed method [10], the gate-oxide breakdown of MOSFET device can be modeled as resistance. Only the gate-to-diffusion (source or drain) breakdown was considered, since these represent the worst case situation. Breakdown to the channel can be modeled as a superposition of two gate-to-diffusion events. Typical hard breakdown leakage has close-to-linear I–V behavior and an equivalent resistance of $\sim 10^3$–10^4 Ω, whereas typical soft breakdown paths have high nonlinear power law I–V behavior and an equivalent resistance above 10^5–10^6 Ω [10]. The complete circuit of the operational amplifier with the two-stage structure, including the gate-oxide breakdown model, is shown in Fig. 18. The breakdown resistances of $R_{\rm BD6}$, $R_{\rm BD7}$, and $R_{\rm BD8}$ can be used to simulate the impact of hard and soft breakdowns on performances of the operational amplifier with the two-stage structure. The noninverting node of the operational amplifiers with the two-stage structure is biased by the ac sinusoidal signal of 500 mV (peak-to-peak amplitude) plus dc offset voltage of 1.25 V with a frequency of 5 kHz. The output capacitive load is set to 10 pF, and the supply voltage $V_{\rm DD}$ is set to 2.5 V. The simulated output voltage swing waveform of operational amplifier with the two-stage structure under different breakdown resistances $R_{\rm BD6}$, $R_{\rm BD7}$, and $R_{\rm BD8}$ is shown in Fig. 19. Comparing with Fig. 16, the hard breakdowns have occurred on M_6, M_7, and M_8 devices in two-stage operational amplifier after dc stress.

B. Large-Signal Transition Stress

When the two-stage operational amplifier is operated as comparator, the output voltage only has two voltage states.

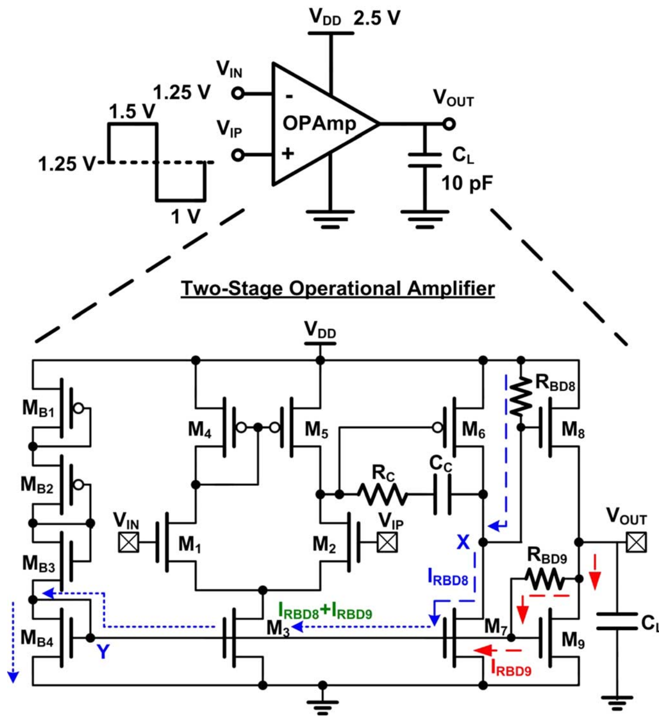


Fig. 20. Complete circuit of the operational amplifier with the two-stage structure including gate-oxide breakdown model under large-signal transient stress.

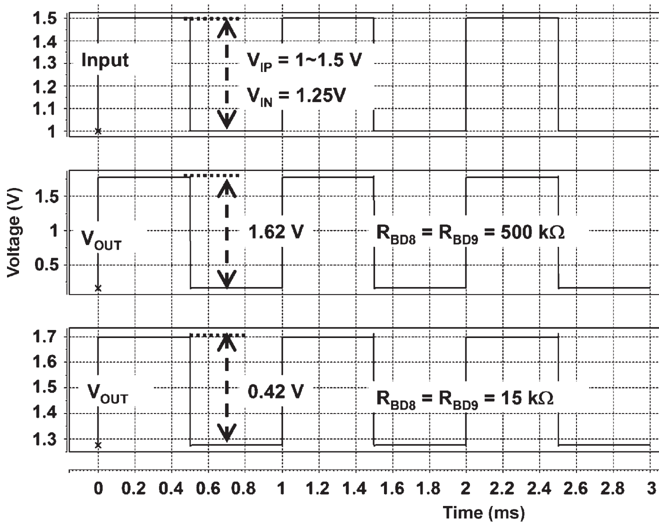


Fig. 21. Simulated high and low output voltage levels of operational amplifier with the two-stage structure under different breakdown resistances R_{BD8} and R_{BD9}.

One is high output voltage level, and another is low output voltage level. In order to investigate and understand the impact of hard and soft breakdowns on performances of the operational amplifier with the two-stage structure under large-signal transition stress, the complete circuits including the gate-oxide breakdown model are shown in Fig. 20. The simulated dependence of high and low output voltage levels of the operational amplifier with the two-stage structure under the different resistances R_{BD8} and R_{BD9} is shown in Fig. 21. Comparing Figs. 14 and 21, the breakdown locations in the operational amplifier with the two-stage structure occurred on M_8 and M_9 devices after large-signal transition stress. Because the oxide breakdowns occurred on devices M_8 and M_9 in two-stage operational amplifier under large-signal transient stress, the node voltages V_X and V_Y would be increased by the extra gate leakage currents I_{RBD8} and I_{RBD9}. When the voltage of 1.5 V is set to input node V_{IP} and the voltage of 1.25 V is set to input node V_{IN}, the node voltage V_X approximates to supply voltage V_{DD}. Therefore, the oxide breakdown has small impact on the high output voltage level of the two-stage operational amplifier under large-signal transient stress. When the voltage of 1 V is set to input node V_{IP} and the voltage of 1.25 V is set to input node V_{IN}, the node voltage V_X approximates to ground (0 V) to turn off the device M_8. After the large-signal transient stress, the node voltages V_X and V_Y would be increased by the extra gate leakage currents I_{RBD8} and I_{RBD9}. The device M_8 cannot be turned off after the large-signal transient stress. Therefore, the low output voltage level of the two-stage operational amplifier would be increased after the large-signal transient stress.

VI. Conclusion

The impact of MOSFET gate-oxide reliability on CMOS operational amplifiers with the two-stage (nonstacked) and folded-cascode (stacked) structures has been investigated and analyzed. The tested structures of the operational amplifiers including both the unity-gain buffer (close-loop) and comparator (open-loop) configurations are stressed under different input frequencies and signals. Because the dc operating point of the analog circuits is changed due to the gate-oxide degradation, the small-signal performances of the operational amplifier with the two-stage structure are seriously degraded after the stress. The performances of the operational amplifier with the two-stage structure under the close-loop configuration are damaged more easily than that under the open-loop configuration after the stress. The gate-oxide reliability in the CMOS analog circuits can be improved by the stacked structure under small-signal input and output applications. However, the large-signal transition still causes some degradation on the circuit performances of the operational amplifier with the folded-cascode (stacked) structure. The impact of soft and hard gate-oxide breakdowns on operational amplifiers with the two-stage and folded-cascode structures has been analyzed and discussed. The hard breakdown has more serious impact on the operational amplifier.

References

[1] D. Seo, H. Dabag, Y. Guo, M. Mishra, and G. H. McAllister, “High-voltage-tolerant analog circuits design in deep-submicrometer CMOS technologies,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 10, pp. 2159–2166, Oct. 2007.

[2] K. Eriguchi and M. Niwa, “Stress polarity dependence of the activation energy in time-dependent dielectric breakdown of thin gate oxides,” *IEEE Electron Device Lett.*, vol. 19, no. 11, pp. 339–401, Nov. 1998.

[3] B. P. Linder, S. Lombardo, J. H. Stathis, A. Vayshenker, and D. Frank, “Voltage dependence of hard breakdown growth and the reliability implication in thin dielectrics,” *IEEE Electron Device Lett.*, vol. 23, no. 11, pp. 661–663, Nov. 2002.

[4] B. Kaczer, R. Degraeve, M. Rasras, K. V. D. Mieroop, P. J. Roussel, and G. Groeseneken, "Impact of MOSFET gate oxide breakdown on digital circuit operation and reliability," *IEEE Trans. Electron Devices*, vol. 49, no. 3, pp. 500–506, Mar. 2002.

[5] B. Kaczer and G. Groesenken, "Potential vulnerability of dynamic CMOS logic to soft gate oxide breakdown," *IEEE Electron Device Lett.*, vol. 24, no. 12, pp. 742–744, Dec. 2003.

[6] H. Yang, J. S. Yuan, Y. Liu, and E. Xiao, "Effect of gate-oxide breakdown on RF performance," *IEEE Trans. Device Mater. Rel.*, vol. 3, no. 3, pp. 93–97, Sep. 2003.

[7] E. Xiao, J. S. Yuan, and H. Yang, "CMOS RF and DC reliability subject to hot carrier stress and oxide soft breakdown," *IEEE Trans. Device Mater. Rel.*, vol. 4, no. 1, pp. 92–98, Mar. 2004.

[8] B. E. Weir, P. J. Silverman, D. Monroe, K. S. Krisch, M. A. Alam, G. B. Alers, T. W. Sorsch, G. L. Timp, F. Baumann, C. T. Liu, Y. Ma, and D. Hwang, "Ultra-thin gate dielectrics: They breakdown, but do they fail," in *IEDM Tech. Dig.*, 1997, pp. 73–76.

[9] M. A. Alam, B. E. Weir, P. J. Siverman, Y. Ma, and D. Hwang, "The statistical distribution of percolation resistance as a probe into the mechanics of ultra-thin oxide breakdown," in *IEDM Tech. Dig.*, 2000, pp. 529–533.

[10] R. Degraeve, B. Kaczer, A. D. Keersgieter, and G. Groeseneken, "Relation between breakdown mode and breakdown location in short channel NMOSFETs and its impact on reliability specifications," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2001, pp. 360–366.

[11] M. Nafria, J. Sune, D. Yelamos, and X. Aymerich, "Degradation and breakdown of thin silicon dioxide films under dynamic electrical stress," *IEEE Trans. Electron Devices*, vol. 43, no. 12, pp. 2215–2226, Dec. 1996.

[12] B. Kaczer, F. Crupi, R. Degraeve, P. Roussel, C. Ciofi, and G. Groesenken, "Observation of hot-carrier-induced nFET gate-oxide breakdown in dynamically stress," in *IEDM Tech. Dig.*, 2002, pp. 171–174.

[13] A. Aevllan and W. H. Kraustschneider, "Impact of soft and hard breakdown on analog and digital circuits," *IEEE Trans. Device Mater. Rel.*, vol. 4, no. 4, pp. 676–680, Dec. 2004.

[14] J.-S. Chen and M.-D. Ker, "The impact of gate-oxide breakdown on common-source amplifiers with diode-connected active load in low-voltage CMOS processes," *IEEE Trans. Electron Devices*, vol. 54, no. 11, pp. 2860–2870, Nov. 2007.

[15] A. M. Abo and P. R. Gray, "A 1.5 V, 10-bits, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[16] J.-B. Park, S.-M. Yoo, S.-W. Kim, Y.-J. Cho, and S.-H. Lee, "A 10-b 150-Msample/s 1.8-V 123-mW CMOS A/D converter with 400-MHz input bandwidth," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1335–1337, Aug. 2004.

[17] B. Serneels, T. Piessens, M. Steyaert, and W. Dehaene, "A high-voltage output driver in the standard 2.5 V 0.25 μm CMOS technology," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2004, pp. 146–155.

[18] J.-S. Chen and M.-D. Ker, "Impact of MOSFET gate-oxide reliability in CMOS operational amplifiers in a 130-nm low-voltage CMOS process," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2005, pp. 423–430.

Ming-Dou Ker (S'92–M'94–SM'97–F'08) received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1993.

He was a Department Manager with the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute, Taiwan. He is currently a Full Professor with the Department of Electronics Engineering, National Chiao-Tung University, where he also serves as the Director of Master Degree Program in the College of Electrical Engineering and Computer Science as well as the Associate Executive Director of National Science and Technology Program on System-on-Chip, Taiwan. He is also with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University. In the field of reliability and quality design for circuits and systems in CMOS technology, he has published over 300 technical papers in international journals and conferences. He has proposed many inventions to improve reliability and quality of integrated circuits and microsystems, which have been granted with 129 U.S. patents and 137 Taiwan patents. His current research topics include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on-panel applications with TFT technology, and biomimetic circuits and systems for intelligent prosthesis applications. He had been invited to teach or to consult reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC industry.

Dr. Ker has served as a member of the Technical Program Committee and Session Chair of numerous international conferences. He was selected as the Distinguished Lecturer in IEEE Circuits and Systems Society for year 2006–2007. He also served as an Associate Editor in IEEE TRANSACTIONS ON VLSI SYSTEMS. He was the President of Foundation in Taiwan ESD Association. In 2003, he was selected as one of the Ten Outstanding Young Persons in Taiwan by Junior Chamber International. In 2005, one of his patents on ESD protection design has been awarded with the National Invention Award in Taiwan. He has been elevated as IEEE fellow, effective in 2008, with the citation of "for contributions to electrostatic protection in integrated circuits, and performance optimization of VLSI micro-systems."

Jung-Sheng Chen received the B.S. degree in electronics engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, R.O.C., in 2000, the M.S. degree in engineering and system science from the National Tsing-Hua University, Hsinchu, Taiwan, in 2002, and the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, in 2007.

He is currently with Power Conversion Taiwan, Fairchild Semiconductor Corporation, Hsinchu. His current research interests include power management integrated circuits and systems.