ESD Protection Design With On-Chip ESD Bus and High-Voltage-Tolerant ESD Clamp Circuit for Mixed-Voltage I/O Buffers

Ming-Dou Ker, *Fellow, IEEE*, and Wei-Jen Chang, *Member, IEEE*

***Abstract*—Considering gate-oxide reliability, a new electrostatic discharge (ESD) protection scheme with an on-chip ESD bus (ESD_BUS) and a high-voltage-tolerant ESD clamp circuit for 1.2/2.5 V mixed-voltage I/O interfaces is proposed. The devices used in the high-voltage-tolerant ESD clamp circuit are all 1.2 V low-voltage N- and P-type MOS devices that can be safely operated under the 2.5-V bias conditions without suffering from the gate-oxide reliability issue. The four-mode (positive-to-V_{SS}, negative-to-V_{SS}, positive-to-V_{DD}, and negative-to-V_{DD}) ESD stresses on the mixed-voltage I/O pad and pin-to-pin ESD stresses can be effectively discharged by the proposed ESD protection scheme. The experimental results verified in a 0.13-μm CMOS process have confirmed that the proposed new ESD protection scheme has high human-body model (HBM) and machine-model (MM) ESD robustness with a fast turn-on speed. The proposed new ESD protection scheme, which is designed with only low-voltage devices, is an excellent and cost-efficient solution to protect mixed-voltage I/O interfaces.**

***Index Terms*—Electrostatic discharge (ESD), high-voltage-tolerant ESD clamp circuit, I/O, mixed-voltage secondary, on-chip ESD bus, secondary breakdown current (I_{t2}) substrate-triggered technique.**

I. Introduction

THE system-on-a-chip (SoC) is becoming more popular and requires special design techniques and technologies in advanced CMOS processes. The gate-oxide thickness of MOSFET has been shrunk to improve circuit performance and operating speed for such SoC applications. In addition, the power supply voltage in CMOS ICs has also been scaled down to follow the constant-field scaling requirement and to reduce power consumption. However, for whole SoC integration, I/O circuits with low-voltages devices must drive or receive high-voltage signals to communicate with other ICs in microelectronic systems or subsystems. To integrate microelectronic systems with different power supply voltages, the chip-to-chip interface I/O circuits must be designed with mixed-voltage I/O interfaces [1]–[4].

The mixed-voltage I/O interfaces must be designed to prevent undesired leakage current paths between the chips [5], [6] and to avoid electrical overstress on the gate oxide [7]. To avoid the leakage current path from the I/O pad to the virtual device driver (VDD) power line, the N-well self-biased circuit and gate-tracking circuit are connected to the pull-up PMOS [8]. To solve the gate-oxide reliability issue without using the additional thick gate-oxide process (called dual gate oxide in some CMOS processes), the stacked NMOS structure had been widely used in the mixed-voltage I/O buffer [1]–[4] to reduce the process complexity and fabrication cost of the chip.

ESD stresses on an I/O pad have four pin-combination modes: positive-to-V_{SS} (PS mode), negative-to-V_{SS} (NS mode), positive-to-V_{DD} (PD mode), and negative-to-V_{DD} (ND mode) [9]–[12]. For the CMOS output buffer to have ESD robustness, the CMOS buffer is generally drawn with larger device dimensions and a wider spacing from the drain contact to the poly gate, which often occupies a larger layout area in the I/O cell. Without increasing device dimensions in the I/O cells, $V_{DD} - V_{SS}$ ESD clamp circuits across the power lines of CMOS ICs have been used to efficiently improve the ESD robustness of CMOS I/O buffers [13]–[15]. However, due to the leakage current issue in the mixed-voltage I/O buffer, any diode connected from the I/O pad to a V_{DD} power line is forbidden. Without a diode from the pad to V_{DD} in mixed-voltage I/O circuits, the positive-to-V_{SS} ESD voltage discharging on the I/O pad cannot be diverted from the pad to the V_{DD} power line and cannot be discharged through the effective power-rail ($V_{DD} - V_{SS}$) ESD clamp circuit. Such positive-to-V_{SS} ESD current on the I/O pad is totally discharged through the stacked NMOS in the mixed-voltage I/O circuit under a snapback-breakdown condition. The ESD current (I_{ESD}), under this positive-to-V_{SS} ESD stress condition, along the mixed-voltage output buffer, is shown by the dashed line in Fig. 1. When the single NMOS and the stacked NMOS are compared in a high-current snapback region, the stacked NMOS will have a higher trigger voltage, a higher snapback holding voltage, a slower turn-on speed, and a lower secondary breakdown current. Therefore, such mixed-voltage I/O circuits with stacked NMOS often have much lower ESD levels under the positive-to-V_{SS} ESD stress condition, as compared to the traditional I/O circuits with a single NMOS [16], [17]. The disadvantages result from the longer base width of the parasitic lateral npn bipolar junction transistor (BJT) in the stacked NMOS devices.

Although stacked NMOS devices solve the gate-oxide reliability issue in the mixed-voltage I/O buffer circuits,

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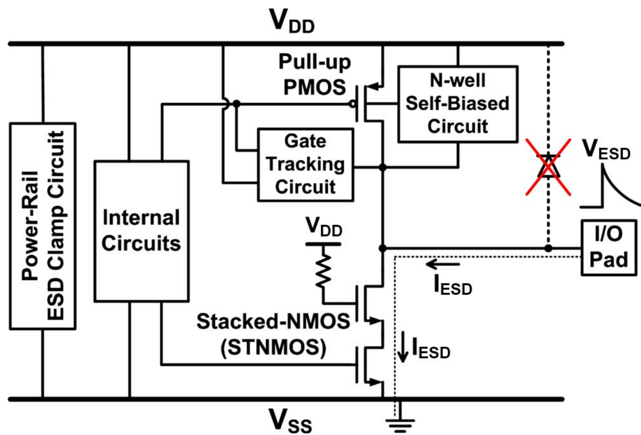


Fig. 1. ESD current paths in the 1.2-V/2.5-V mixed-voltage I/O buffer during a positive-to-V_{SS} ESD stress condition.

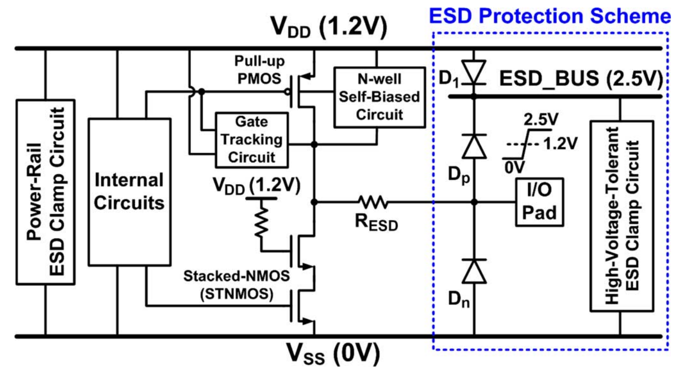


Fig. 2. Proposed new ESD protection scheme for 1.2 V/2.5 V mixed-voltage I/O interfaces with a high-voltage-tolerant ESD clamp circuit.

unfortunately, the high holding voltage of stacked NMOS devices causes degradation on its ESD robustness. The substrate-triggered technique, realized by special circuit design, is therefore applied to improve ESD robustness of stacked NMOS in the mixed-voltage I/O buffer. Recently, a special substrate-triggered design with a diode string has been reported to improve ESD robustness of mixed-voltage I/O circuits in a 0.25-μm CMOS process [18]. Moreover, a modified substrate-triggered design has also been reported to improve ESD robustness of the stacked NMOS device without using the thick gate oxide device in a 0.25-μm CMOS process [19].

In this paper, a new ESD protection scheme with an ESD_BUS and a high-voltage-tolerant ESD clamp circuit is designed to protect the mixed-voltage I/O interfaces against ESD stresses without suffering the gate-oxide reliability issue [20]–[23]. The proposed high-voltage-tolerant ESD clamp circuit, which combines the stacked NMOS of 1.2-V gate oxide with the substrate-triggered technique, is designed to protect the 1.2/2.5-V mixed-voltage I/O interfaces. This high-voltage-tolerant ESD clamp circuit has higher ESD robustness and a faster turn-on speed, which has been successfully verified in a 0.13-μm 1.2-V CMOS process.

II. New ESD Protection Scheme for Mixed-Voltage I/O Interfaces

Giving consideration to gate-oxide reliability, the proposed ESD protection scheme with an on-chip ESD bus (ESD_BUS) and a high-voltage-tolerant ESD clamp circuit for 1.2/2.5 V mixed-voltage I/O interfaces is shown in Fig. 2. To receive the input signals with a 2.5-V voltage level, the direct diode connection from the I/O pad to the 1.2-V V_{DD} is forbidden. Hence, to avoid the leakage current path from the I/O pad to the V_{DD}, the new ESD scheme is made with diodes D_p, D_n, and D_1, the ESD_BUS line, and a high-voltage-tolerant ESD clamp circuit, as shown in Fig. 2.

The additional ESD_BUS line is indicated by a wide metal line in the CMOS IC [24], [25]. To save the layout area, the ESD_BUS can be realized by a different metal layer, which overlaps the V_{DD} power line. The ESD_BUS is not directly connected to an external power pin, but it is initially biased at the V_{DD} of 1.2 V through the diode D_1 after the chip has been powered on. When 2.5-V input signals reach the I/O pad, the ESD_BUS line will be charged up to 2.5 V through diode D_p. Therefore, during normal circuit operating conditions with 2.5-V input signals, diode D_1, connected between the V_{DD} power line and ESD_BUS line, is used to block the leakage current path from the I/O pad to the V_{DD}.

The positive-to-V_{SS}, negative-to-V_{SS}, positive-to-V_{DD}, and negative-to-V_{DD} ESD stresses on the mixed-voltage I/O pad have corresponding ESD discharge paths in the proposed ESD protection scheme. The R_{ESD} is used to avoid damage on the stacked NMOS before the ESD current is discharged through the proposed ESD scheme. Under the positive-to-V_{SS} ESD stress condition, the ESD current will flow from the I/O pad through the diode D_p to the ESD_BUS, and then from the ESD_BUS through the high-voltage-tolerant ESD clamp circuit to V_{SS}. Under the negative-to-V_{SS} ESD stress condition, the ESD current will flow from V_{SS} through diode D_n in the forward-biased condition to the I/O pad. Under the positive-to-V_{DD} ESD stress condition, the ESD current will flow from the I/O pad through diode D_p to the ESD_BUS, and then from the ESD_BUS through the high-voltage-tolerant ESD clamp circuit to the V_{SS} line, and then through the power-rail ESD clamp circuit to the V_{DD}. Under the negative-to-V_{DD} ESD stress condition, the ESD current will flow from V_{DD} through the power-rail ESD clamp circuit to the V_{SS} line, and then from the V_{SS} through diode D_n in the forward-biased condition to the I/O pad.

Here, the ESD_BUS and high-voltage-tolerant ESD clamp circuit can be shared to provide efficient pin-to-pin ESD protection. In the pin-to-pin ESD test, the ESD pulse is applied to an I/O pin with other I/O pins grounded, whereas the V_{DD} and V_{SS} are floating [9]–[12]. During pin-to-pin ESD stress, as shown in Fig. 3, the ESD current will flow from one I/O pad through diode D_p to the common ESD_BUS, and then from the ESD_BUS through the high-voltage-tolerant ESD clamp circuit to the V_{SS} line, and finally from V_{SS} through the diode D_n to another grounded I/O pad.

In the prior arts [18], [19], ESD detection circuit was connected between the I/O pad and the V_{SS} line to improve the ESD robustness of the stacked NMOS in each I/O cell directly, which increased the additional loading capacitance to the I/O pad and occupied large layout area in the chip. To save the

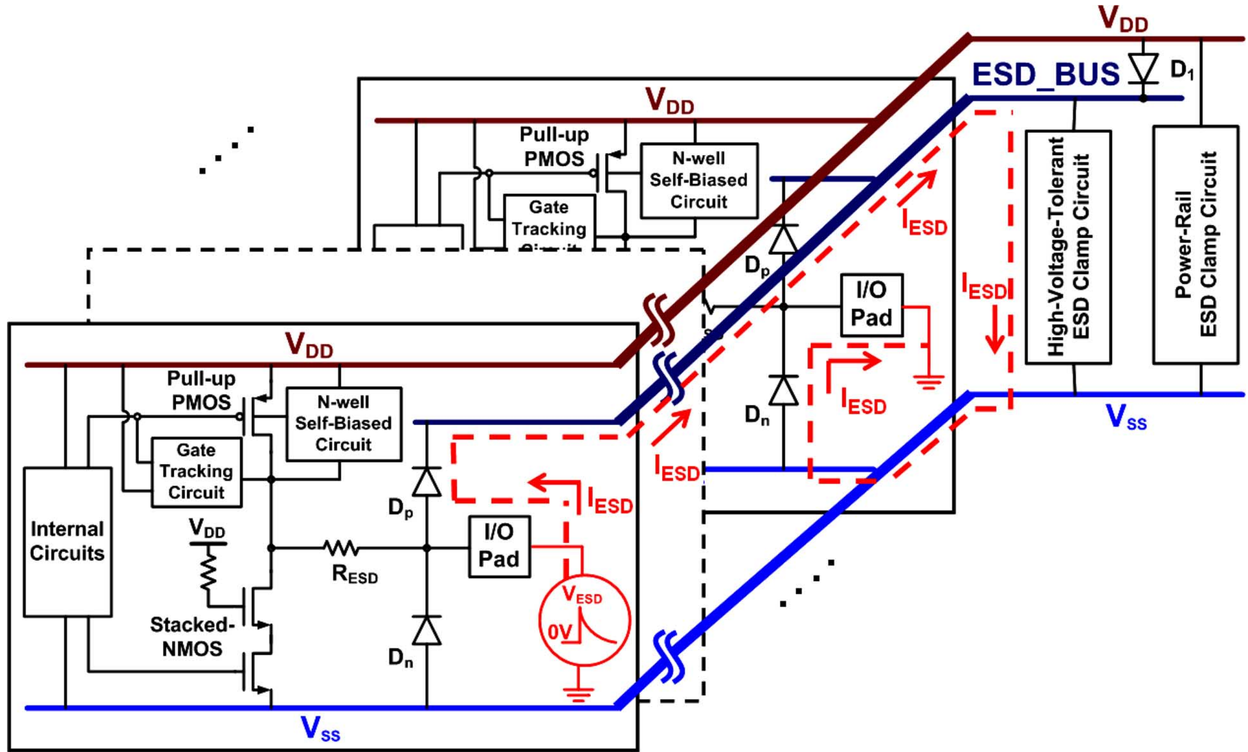


Fig. 3. Shared ESD_BUS and high-voltage-tolerant ESD clamp circuit for the whole set of I/O cells to achieve pin-to-pin ESD protection.

layout area of the chip and to decrease the loading capacitance on the I/O pad, the ESD_BUS and the high-voltage-tolerant ESD clamp circuit can be shared with other mixed-voltage I/O cells that have the same input/output voltage levels. Moreover, the other advantage of this new proposed ESD protection scheme is that the shared ESD_BUS and high-voltage-tolerant ESD clamp circuit can provide more efficient pin-to-pin ESD protection than the prior arts [18], [19]. Although the ESD protection scheme with both ESD_BUS and high-voltage-tolerant ESD clamp circuit can provide effective discharging path for the mixed-voltage I/O cells, however, the parasitic capacitance and parasitic resistance along the long ESD_BUS line in a large chip could degrade ESD protection effectiveness [26]–[29]. Hence, the location of the high-voltage-tolerant ESD clamp circuit should be placed near the I/O cells with some specified design rules in a given CMOS process [14].

In this ESD protection scheme, the high-voltage-tolerant ESD clamp circuit must sustain the high-voltage (2.5 V) stress in the mixed-voltage I/O circuit during normal circuit operating conditions. Hence, how to design a turn-on efficient high-voltage-tolerant ESD clamp circuit with only 1.2 V devices for 2.5 V application is the key design issue in the proposed ESD protection scheme for 1.2/2.5 V mixed-voltage I/O interfaces.

III. High-Voltage-Tolerant ESD Clamp Circuit

The high-voltage-tolerant ESD clamp circuit consisting only of 1.2 V devices is shown in Fig. 4, which contains the ESD detection circuit and the ESD clamp device. The ESD clamp device has a stacked NMOS (STNMOS) with a substrate-triggered technique [30]. The STNMOS is formed by two stacked NMOS transistors (M_{n1} and M_{n2}) with a 1.2-V gate

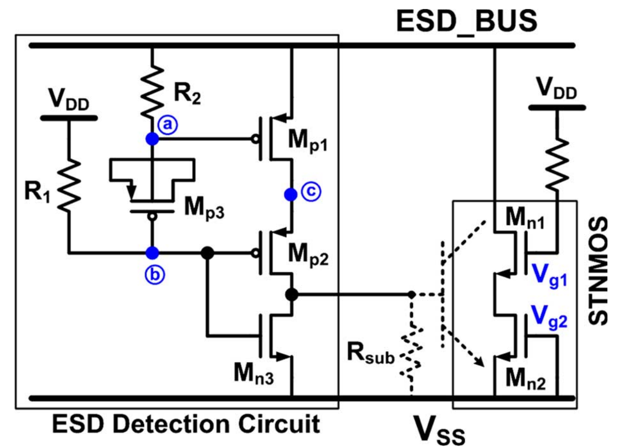


Fig. 4. Proposed high-voltage-tolerant ESD clamp circuit.

oxide in a 0.13-μm CMOS process. The gate of $\mathrm{M}_{n1}(\mathrm{V}_{g1})$ is biased at the V_{DD} of 1.2 V through a resistor to avoid the gate-oxide reliability issue, and the gate of $\mathrm{M}_{n2}(\mathrm{V}_{g2})$ is connected to the V_{SS} (grounded) to ensure the off state of the STNMOS during normal circuit operating conditions. Therefore, STNMOS will be kept off without gate-oxide reliability during normal circuit operating conditions with a 2.5-V ESD_BUS.

The ESD detection circuit is inactive during normal circuit operating conditions, but it becomes active to provide the substrate-triggered current to trigger on an ESD clamp device under an ESD stress event. The gate voltage of PMOS M_{p1} is decided by the RC delay caused by an N-well resistor R_2 and a capacitor (realized by M_{p3} in a stand-alone N well). Here, the time constant of R_2 and C (M_{p3}) is designed around the order of $\sim$1 μs to distinguish the power-on transition (the

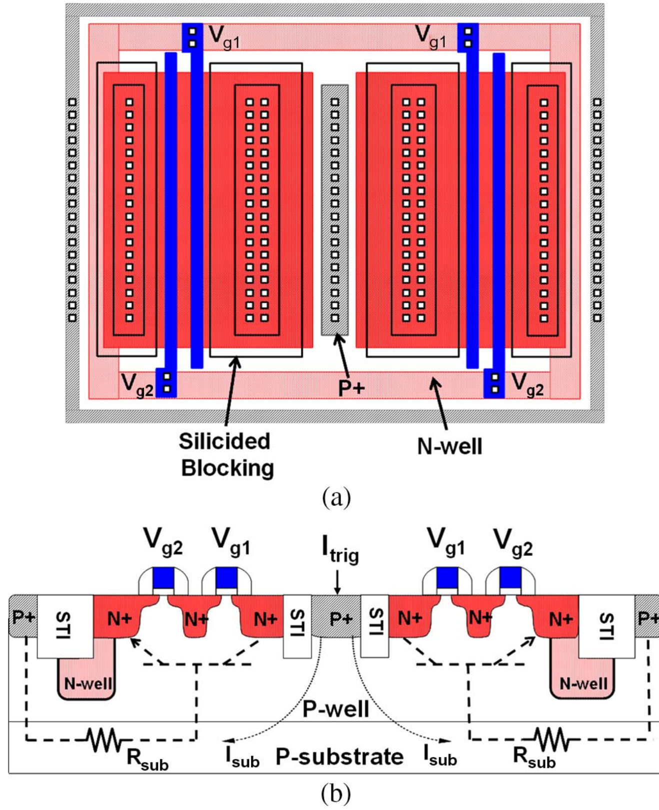


Fig. 5. (a) Finger-type layout pattern and (b) corresponding cross-sectional view of the substrate-triggered STNMOS device.

supply voltage with a rise time of several milliseconds) from the ESD transition (the ESD voltage with a rise time of several nanoseconds).

A. Substrate-Triggered STNMOS

The snapback breakdown of an STNMOS device depends on the substrate current (I_{sub}), which is created by the reverse-biased drain/substrate junction in breakdown condition, to forward bias the source/substrate junction. The substrate current (I_{sub}) drifting through the effective substrate resistance (R_{sub}) to ground will elevate the substrate potential (V_{sub}) of the emitter-base junction in the parasitic lateral npn bipolar junction transistor (BJT). When the emitter-base junction begins to weakly forward bias due to the increase of the local substrate potential, the lateral npn BJT will be turned on to discharge the ESD current. Hence, the substrate resistance (R_{sub}) and the substrate current (I_{sub}) are the design parameters to enhance turn-on efficiency [31], [32]. The substrate-triggered technique [30] can be applied to generate the necessary substrate current (I_{sub}) without causing drain/substrate junction breakdown. With the applied substrate-triggered current (I_{trig}), the trigger voltage (V_{t1}) of the STNMOS can be reduced for more effective ESD protection.

The finger-type layout pattern and the corresponding cross-sectional view of the substrate-triggered STNMOS device are shown in Fig. 5(a) and (b), respectively. Here, the drain of M_{n2} and the source of M_{n1} share a common N+ diffusion region. An additional P+ diffusion is inserted into the center region of the STNMOS device structure as the substrate-triggered point. An N-well structure is further diffused under the source region to form a higher equivalent substrate resistance (R_{sub}) to improve turn-on efficiency of the parasitic lateral npn BJT in the STNMOS.

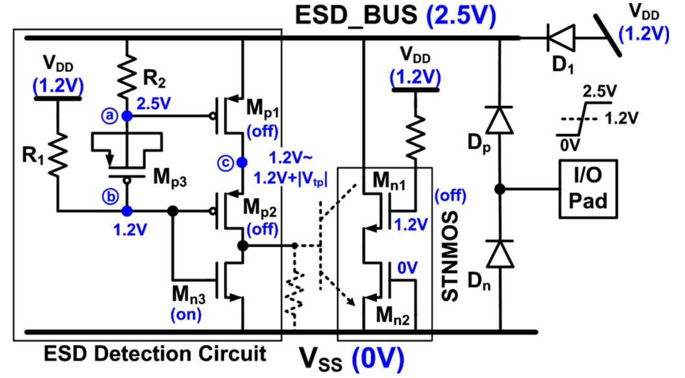


Fig. 6. Operation of a high-voltage-tolerant ESD clamp circuit during normal circuit operating conditions.

B. Principles of Operation

Operation of the high-voltage-tolerant ESD clamp circuit during normal circuit operating conditions is shown in Fig. 6. With a 1.2-V V_{DD} power supply voltage, the ESD_BUS could be charged up to (maximum) 2.5 V by the 2.5-V input signals at the I/O pad. With a maximum voltage level of 2.5 V on the ESD_BUS, the gate of M_{p1} (node a) will be biased at 2.5 V through resistor R_2, and the gate of M_{p2} and M_{n3} (node b) will be biased at 1.2 V through resistor R_1. Hence, M_{p1} and M_{p2} are kept off, and M_{n3} is turned on to bias the substrate of STNMOS at V_{SS}. There is no trigger current generated from the ESD detection circuit into the STNMOS, so STNMOS is guaranteed to be kept off under normal circuit operating conditions. The source-gate voltage of M_{p2} is less than the threshold voltage of the 1.2-V PMOS transistor $(|V_{tp}|)$, so the source voltage of M_{p2} (node c) is kept between V_{DD} and $V_{DD} + |V_{tp}|$. In this situation, all 1.2-V devices are free from the gate-oxide reliability issue under normal circuit operating conditions with a 2.5-V ESD_BUS in the mixed-voltage I/O interfaces.

Operation of the high-voltage-tolerant ESD clamp circuit during a positive-to-V_{SS} ESD stress event is shown in Fig. 7, where the ESD transition voltage is applied to the I/O pad with V_{SS} relatively grounded and V_{DD} floating. The ESD transient voltage will be conducted from the I/O pad through diode D_p to the ESD_BUS. The gate of M_{p1} (node a) will be kept at a relatively low voltage for a long time due to the RC delay of R_2 and M_{p3} in the ESD detection circuit. V_{DD} is initially floating with an initial voltage of 0 V before the ESD transition voltage is applied across the I/O pad and V_{SS}. Some ESD transient voltage would be coupled to V_{DD} through parasitic capacitance during ESD discharging, but R_1 and the parasitic capacitance at the gates of M_{p2} and M_{n3} will hold the gate of M_{p2} at a low voltage level for a long time to keep M_{p2} at the on state. Therefore, M_{p1} and M_{p2} (whose initial gate voltages are at a low voltage level of $\sim$0 V) can be quickly turned on by ESD energy to generate the substrate-triggered current (I_{trig}) into the

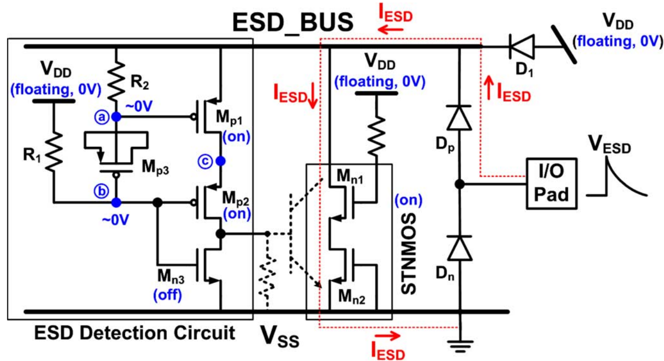


Fig. 7. Operation of a high-voltage-tolerant ESD clamp circuit during a positive-to-V_{SS} ESD stress event.

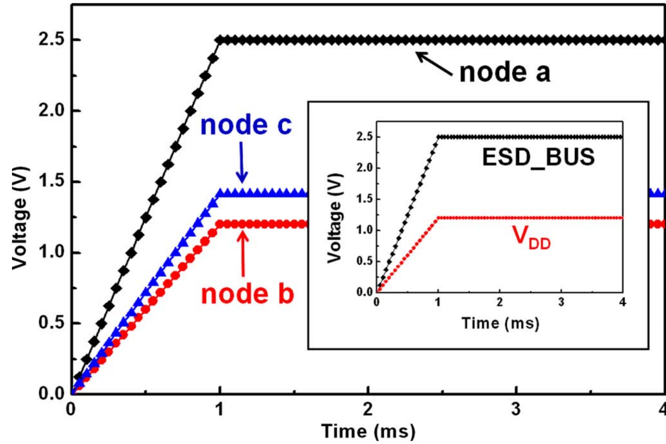


Fig. 8. Hspice-simulated voltage waveforms of the ESD detection circuit during normal power-on transition.

substrate of STNMOS. After the base-emitter voltage of the lateral npn BJT in the STNMOS is greater than its cut-in voltage, the STNMOS will be triggered into its snapback region. Hence, the positive-to-V_{SS} ESD current will be conducted from the I/O pad through diode D_p to the ESD_BUS, and then through the lateral npn BJT in the STNMOS to V_{SS}.

C. Hspice-Simulated Results

The device dimensions of M_{p1}, M_{p2}, M_{p3}, and M_{n3} in the ESD detection circuit are 40 $\mu m/0.2$ μm, 40 $\mu m/0.2$ μm, 10 $\mu m/7.5$ μm, and 5 $\mu m/0.2$ μm, respectively. R_1 and R_2 in the detection circuit are 1 kΩ and 50 kΩ, respectively. The Hspice-simulated voltage waveforms of the ESD detection circuit during power-on transition are shown in Fig. 8. ESD_BUS and V_{DD} are powered on to 2.5 V and 1.2 V, respectively, with a simultaneous rise time of 1 ms. Therefore, the gate voltage of M_{p1} (node a) in the ESD detection circuit with the selected $R_2 - M_{p3}$ value (1 μs) can be validated to follow up the power-on transition of the ESD_BUS, to keep the PMOS M_{p1} off. Moreover, from the Hspice-simulated voltage waveforms, the voltages across the gate-drain, gate-source, and gate-bulk terminations of every device in the proposed high-voltage-tolerant ESD clamp circuit do not exceed the process limitation (~1.32 V in a given 1.2-V CMOS process).

The transient simulation of the ESD detection circuit under an ESD stress event is shown in Fig. 9. When a 0–5.5V ESD-like voltage pulse with a rise time of 10 ns is applied to the ESD_BUS with V_{SS} relatively grounded and V_{DD} floating, the gate voltage of M_{p1} (node a) is kept at a low voltage level due to the time delay of $R_2 - M_{p3}$. Therefore, a substrate-triggered current (I_{trig}) can be conducted through M_{p1} and M_{p2} in the ESD detection circuit to trigger on STNMOS. By selecting suitable device dimensions for R_2, M_{p1}, M_{p2}, and M_{p3}, the peak current and period of the substrate-triggered current can be designed to meet different applications or specifications.

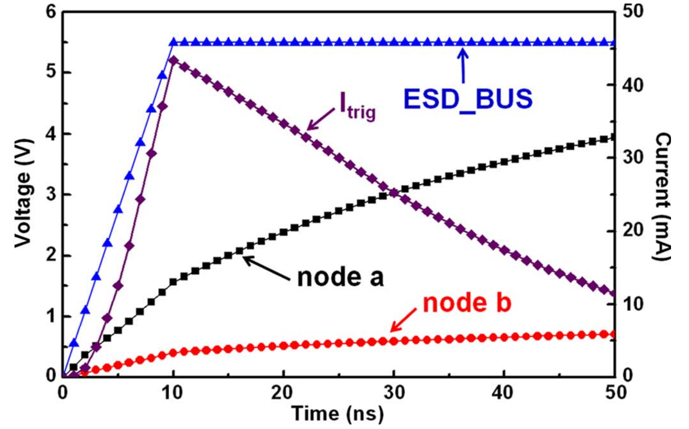


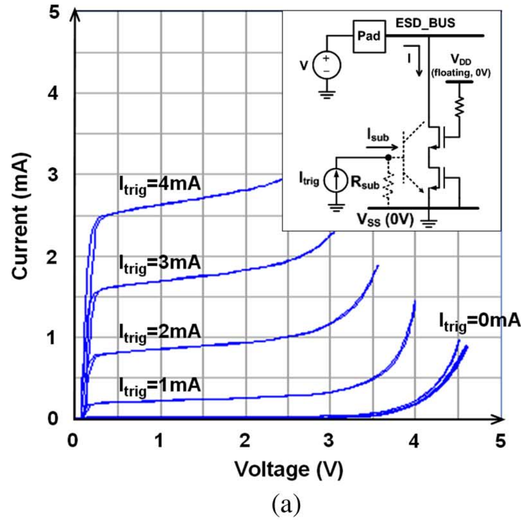
Fig. 9. Hspice-simulated voltage waveforms of the ESD detection circuit during an ESD stress event.

IV. Experimental Results

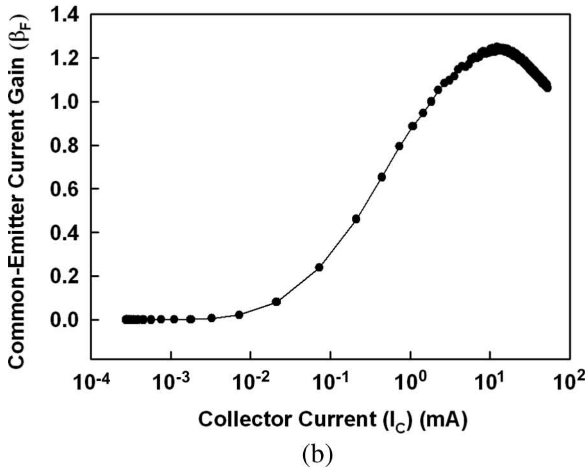
A. Characteristics of Substrate-Triggered STNMOS

The measured dc current-voltage (I–V) characteristics of STNMOS with a device dimension (W/L) of 360 $\mu m/0.2$ μm under different substrate-triggered currents (measured by a Tek370 curve tracer) are shown in Fig. 10(a). The trigger voltage of the parasitic lateral npn BJT in the STNMOS device decreases when the substrate-triggered current (I_{trig}) increases. Moreover, the relation of common-emitter current gain (β_F) to collector current (I_C) in the STNMOS is also shown in Fig. 10(b). β_F increases as I_C increases when I_C is lower than ~10 mA. However, β_F decreases as I_C increases when I_C is larger than ~10 mA. The peak value of β_F is about 1.3 when I_C is about ~10 mA.

To investigate the device behavior during high ESD current stress, the transmission line pulsing (TLP) technique [33] has been widely used to measure the second breakdown characteristics [secondary breakdown current (I_{t2}) and secondary breakdown voltage (V_{t2})] of ESD devices. The TLP generator (TLPG) with a pulse width of 100 ns and a rise time of 10 ns is used to find the I_{t2} of STNMOS devices under different substrate-triggered currents. The TLP-measured I–V characteristics of the substrate-triggered STNMOS with a device dimension (W/L) of 360 $\mu m/0.2$ μm under substrate-triggered currents of 0, 2, and 4 mA, respectively, are shown in Fig. 11. With a substrate-triggered current of 4 mA, STNMOS can be triggered on with a trigger voltage below 4 V, as compared to an original drain breakdown voltage of ~6 V. In addition, the turn-on uniformity among the multiple fingers of STNMOS can be improved by the substrate-triggered effect [30].



(a)



(b)

Fig. 10. (a) Measured DC I–V curves of the STNMOS device under different substrate-triggered currents. (b) Measured $\beta_F - I_C$ relation of the STNMOS device.

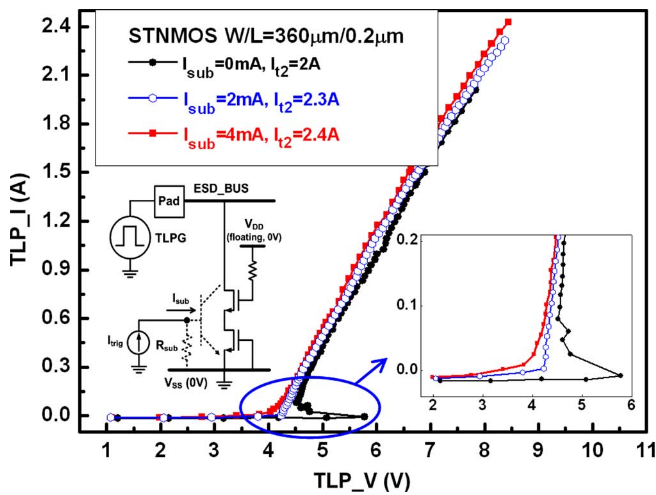


Fig. 11. TLP-measured I–V curves of the STNMOS device with device dimensions (W/L) of 360 μm/0.2 μm under different substrate-triggered currents.

The I_{t2} level of the substrate-triggered STNMOS device can be improved from 2 to 2.4 A when the substrate-triggered current is increased from 0 to 4 mA. With a higher I_{t2}, STNMOS can sustain a higher ESD level.

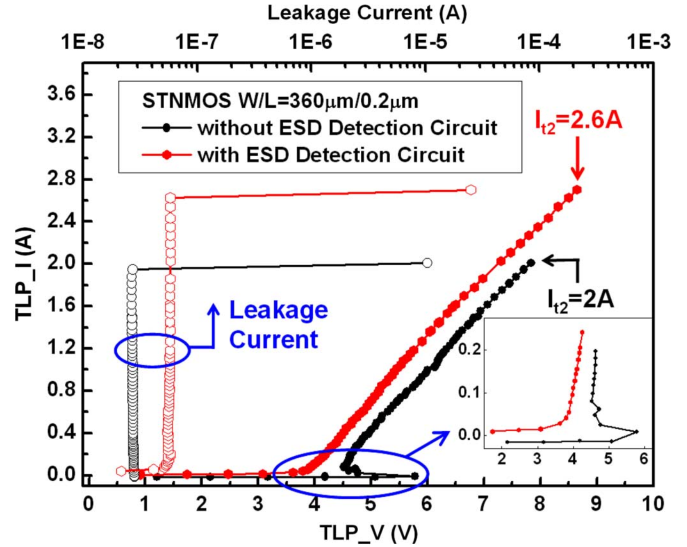


Fig. 12. TLP-measured I–V curve of the STNMOS with or without ESD detection circuit under device dimensions (W/L) of 360 $\mu\mathrm{m}/0.2\ \mu\mathrm{m}$.

Based on the experimental results, the high-voltage-tolerant ESD clamp circuit can be designed with a lower trigger voltage and higher ESD robustness. The TLP-measured I–V curves of STNMOS with or without the ESD detection circuit under device dimension (W/L) of 360 $\mu\mathrm{m}/0.2\ \mu\mathrm{m}$ are shown in Fig. 12. Compared to the stand-alone STNMOS, the secondary breakdown current (I_{t2}) of the STNMOS with the proposed ESD detection circuit can be increased from 2 to 2.6 A. The R_{ESD} in Fig. 2 should be designed a little larger than the critical value such that STNMOS in the mixed-voltage I/O interface will not be damaged before the ESD current is discharged through the diode D_p, the ESD_BUS, and the high-voltage-tolerant ESD clamp circuit to the grounded V_{SS} under the positive-to-V_{SS} ESD stress. The V_{t2} of STNMOS in the mixed-voltage I/O interface $(V_{t2,I/O})$ plus the voltage drop of the $R_{ESD}(I_{t2,I/O} \times R_{ESD})$ should be larger than the V_{t2} of STNMOS in the high-voltage-tolerant ESD clamp circuit $(V_{t2,ESD})$ plus the turn-on voltage of the diode $D_p(V_{D,on})$, as seen in the following equation,

$$V_{t2,\mathrm{ESD}} + V_{D,\mathrm{on}} \leq (I_{t2,\mathrm{I/O}} \times R_{\mathrm{ESD}}) + V_{t2,\mathrm{I/O}}. \quad (1)$$

Here, $V_{t2,ESD}$ (8.7 V) and $V_{t2,I/O}$ (7.8 V) can be derived from the secondary breakdown voltage of STNMOS with and without the ESD detection circuit in Fig. 12, respectively. The $I_{t2,I/O}$(2 A) can be derived from the secondary breakdown current of the STNMOS without the ESD detection circuit in Fig. 12. According to (1), R_{ESD} should be designed greater than 0.8 Ω in this given CMOS process.

Moreover, the I_{t2} of STNMOS with or without the ESD detection circuit under different device dimensions are also measured in Fig. 13. The STNMOS device with an ESD detection circuit has a higher I_{t2} than that without an ESD detection circuit. For the device dimension (W/L) of 240 $\mu\mathrm{m}/0.2\ \mu\mathrm{m}$, I_{t2} can be increased from 1.4 to 2.4 A, which is a $\sim$70% improvement.

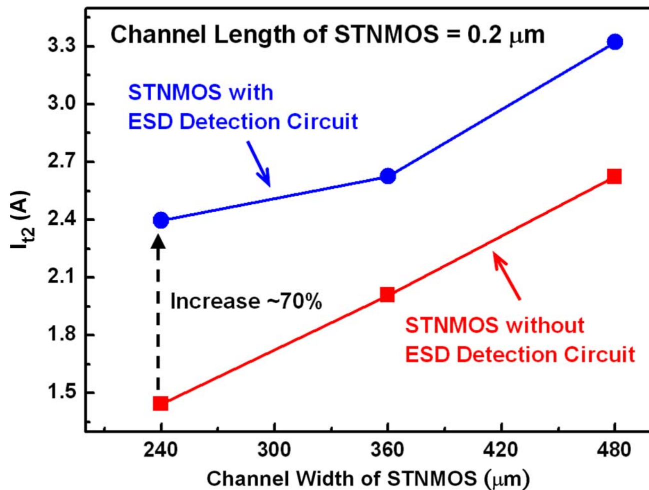


Fig. 13. TLP-measured I_{t2} of the STNMOS device with or without the ESD detection circuit under different channel widths.

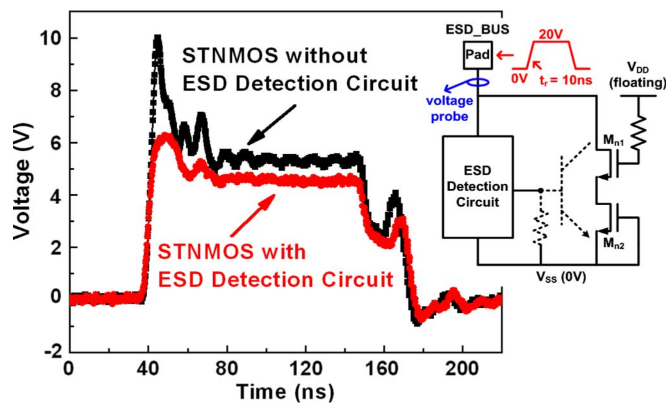


Fig. 14. Measured voltage waveform of STNMOS with or without the ESD detection circuit under 0–20 V voltage pulse with a rise time of 10 ns on the ESD_BUS pad.

B. Turn-on Speed

To verify the turn-on efficiency of the proposed high-voltage-tolerant ESD clamp circuit, a 0–20 V voltage pulse with a rise time of 10 ns is applied to the ESD_BUS with V_{SS} grounded and V_{DD} floating, as shown in Fig. 14. The overshooting peak voltage clamped by the STNMOS without the ESD detection circuit is about 10 V, which could cause damage to the gate oxide of the low-voltage devices. On the contrary, the 20-V voltage pulse can be quickly clamped by the STNMOS with the ESD detection circuit to a low voltage level (~5 V). The measured voltage waveforms in Fig. 14 have successfully verified the excellent turn-on efficiency of the proposed new high-voltage-tolerant ESD clamp circuit. Hence, during a positive-to-V_{SS} ESD stress condition, the ESD current can be quickly discharged from the I/O pad through diode D_p, ESD_BUS, and high-voltage-tolerant ESD clamp circuit to V_{SS}, instead of through STNMOS in the mixed-voltage I/O interface to V_{SS}.

C. ESD Robustness of STNMOS Devices

The human-body-model (HBM) and machine-model (MM) ESD level of STNMOS devices with different device dimensions are shown in Table I. In these ESD verifications, the failure criterion is defined as the I–V characteristic curve shifting over 30% from its original curve after three continuous ESD discharges at every ESD test level. With the substrate-triggered current generated from the proposed ESD detection circuit, the turn-on uniformity of STNMOS can be effectively improved. The HBM (MM) ESD levels of the STNMOS with the ESD detection circuit in the high-voltage-tolerant ESD clamp circuit under channel widths of 240, 360, and 480 μm, respectively, with a channel length of 0.2 μm are improved from 3, 4, and 5 kV (175, 250, and 275 V) to 4, 5, and 6.5 kV (225, 300, and 400 V), respectively, as compared with the stand-alone STNMOS. As a result, the ESD levels of these 1.2/2.5 V mixed-voltage I/O interfaces can be effectively improved by the proposed new ESD protection scheme with the ESD_BUS and the high-voltage-tolerant ESD clamp circuit. Furthermore, only the I/O cells and ESD protection circuits are drawn in this test chip, which is only the size of a small die. Hence, the charged-device-model (CDM) ESD level, which is strongly dependent on the die size, of the test chip in this paper can pass over ±1 kV.

TABLE I
HBM AND MM ESD LEVELS OF STNMOS WITH OR WITHOUT AN ESD DETECTION CIRCUIT

STNMOS W/L (μm/μm)	HBM ESD Level (kV)		MM ESD Level (V)	
	without Detection Circuit	with Detection Circuit	without Detection Circuit	with Detection Circuit
240/0.2	3	4	175	225
360/0.2	4	5	250	300
480/0.2	5	6.5	275	400

V. CONCLUSION

A new ESD protection scheme with an ESD_BUS and a high-voltage-tolerant ESD clamp circuit for a SoC with 1.2/2.5 V mixed-voltage I/O interfaces has been successfully designed and verified in a 0.13-μm CMOS process. The ESD stresses on the mixed-voltage I/O pad and the pin-to-pin ESD stresses can be effectively discharged by the proposed ESD protection scheme. With substrate-triggered current generated from the ESD detection circuit, the turn-on speed and ESD robustness of the high-voltage-tolerant ESD clamp circuit can be significantly increased as compared with a stand-alone STNMOS. For an STNMOS with a device dimension (W/L) of 480 μm/0.2 μm, the HBM (MM) ESD level of the 1.2/2.5 V mixed-voltage I/O interfaces can be improved from 5 kV (275 V) to 6.5 kV (400 V) by the ESD detection circuit in the proposed ESD protection scheme.

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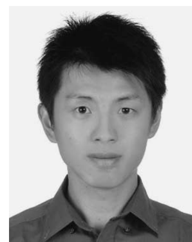

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