Comparison of MONOS Memory Device Integrity When Using $Hf_{1-x-y}N_xO_y$ Trapping Layers With Different N Compositions

H. J. Yang, C. F. Cheng, W. B. Chen, S. H. Lin, F. S. Yeh, Sean P. McAlister, *Senior Member, IEEE*, and Albert Chin, *Senior Member, IEEE*

***Abstract*—We have studied the nitrogen composition dependence of the characteristics of TaN/HfLaON/$Hf_{1-x-y}N_xO_y$/SiO_2/Si MONOS memory devices. By increasing the N composition in the $Hf_{1-x-y}N_xO_y$ trapping layer, both the memory window and high-temperature retention improved. The $Hf_{0.3}N_{0.2}O_{0.5}$ MONOS device displayed good characteristics in terms of its ±9-V program/erase (P/E) voltage, 100-μs P/E speed, large initial 2.8-V memory window, and a ten-year extrapolated retention of 1.8 V at 85 °C or 1.5 V at 125 °C.**

***Index Terms*—Erase, high-κ, nonvolatile memory, program.**

I. Introduction

FOR NONVOLATILE memory applications as scaling decreases below 50 nm, Poly-Si/SiO_2/Si_3N_4/SiO_2/Si (SONOS) devices [1]–[13] are promising. This is because of the merit of charge storage in discrete traps within the Si_3N_4, which prevents charge leakage through a single oxide defect, as compared with the conventional poly-Si floating gate memory case. By replacing the poly-Si in SONOS with a high work-function metal gate (MONOS), further improvements of the erase performance can be achieved by decreasing the electron injection over the gate. However, one difficulty in SONOS or MONOS is the small conduction band discontinuity (ΔE_C) of only 1.1 eV at the Si_3N_4/SiO_2 interface [14], which causes charge leak out from shallow trap levels near E_C of Si_3N_4. In contrast, a conventional poly-Si floating gate device has a much deeper energy of ∼3.15 eV for storage of charge. Therefore, the high-temperature retention is a serious concern for a shallow trap energy MONOS device that uses a Si_3N_4. To address this requires the use of a thick SiO_2 tunnel layer to improve the charge storage, but unfortunately, this leads to a performance degradation of increased program/erase (P/E) voltage and write speed. This is contrary to the scaling trend indicated in the International Technology Roadmap for Semiconductors (ITRS) [1]. To overcome this problem, we have previously proposed the use of an Al(Ga)N [11], [12] storage layer which has deeper ΔE_C than Si_3N_4. This improved the P/E voltage and write speeds in such deep-trap MONOS devices. Unfortunately, further improvement beyond Al(Ga)N [12] is limited since most of the metal–nitrides are metallic. To avert this problem, we used a higher κ $Hf_{1-x-y}N_xO_y$ dielectric for MONOS applications, where even lower P/E voltages and better high-temperature retention can be achieved [13]. Here, we increase the nitride composition in the $Hf_{1-x-y}N_xO_y$ beyond that of our previous work [13] and investigate how this alters the characteristics. Our TaN/HfLaON/$Hf_{0.3}N_{0.2}O_{0.5}$/SiO_2/Si MONOS device showed a large initial memory window of 2.8 V at 100 μs and a low ±9-V P/E. The ten-year extrapolated retention of 1.8 V at 85 °C or 1.5 V at 125 °C compares well with other published data [1]–[13].

II. Experimental Details

The fabrication process of the TaN/HfLaON/$Hf_{1-x-y}N_xO_y$/SiO_2/Si MONOS devices was similar to previous works [11]–[13]. First, a 2.9-nm-thick thermal SiO_2 was grown on a standard p-Si substrate. Then, a 9-nm $Hf_{1-x-y}N_xO_y$ layer was deposited by reactive sputtering under a mixed O_2 and N_2 conditions [13] with different O_2/N_2 ratios—to study the N% dependence of the MONOS device integrity [the detailed composition of N and O in the $Hf_{1-x-y}N_xO_y$ was measured by X-ray photoelectron spectroscopy (XPS)]. A 15-nm HfLaON [15] blocking oxynitride was included because of its good thermal stability at 1000 °C and its higher κ than the previously used HfAlO. Finally, a 150-nm TaN layer was added by sputtering. After standard processing, the MONOS devices were made by self-aligned As^+ ion implantation and given a 950-°C rapid thermal annealing activation to form the S/D regions. The memory devices were characterized by different P/E tests, retention experiments, and cycling endurance at 25 °C, 85 °C, and 125 °C.

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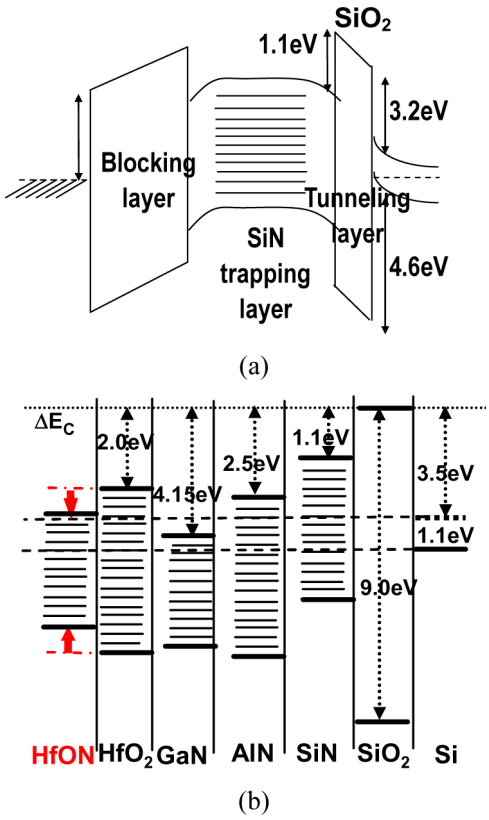


Fig. 1. (a) Schematic band diagram of a SiN trapping layer MONOS device and (b) the band alignment of various metal–oxide trapping layers to the oxide barrier and Si channel.

III. Results and Discussion

A. Engineering the Trap Energy

Fig. 1(a) shows a schematic energy band diagram of a conventional SiN trapping layer MONOS device. The SiN trapping layer has a small ΔE_C with respect to the barrier oxide of only 1.1 eV and many traps in deep as well as in shallow energy levels. Since the trap energy is distributed statistically, it is difficult to tune the trap energy to involve only deep energy levels. Thus, the SiN MONOS devices are expected to have poor retention properties because of the small ΔE_C and charge loss from shallow energy levels, unless a very thick barrier oxide is used to trade off the poor P/E voltage and speed. However, this is not consistent with scaling trends and system-on-chip (SoC) requirements, where lower P/E voltages and faster P/E speeds are needed. These are the fundamental challenges for conventional SiN charge-trapping MONOS devices.

To address these issues, we previously proposed and demonstrated the use of a deep trapping metal–oxide instead of a nitride. Fig. 1(b) shows the band alignment with respect to the barrier oxide and Si channel [12], [13], [16]. Although the trap energy is distributed statistically from levels which are shallow to ones that are deep, the ΔE_C in AlN and Al(Ga)N is improved when compared with SiN. Since the electron injection through the oxide follows an exponential dependence with a barrier height, a large ΔE_C with deeper trapping energy is the key factor in improving the retention in charge-trapping MONOS devices. This is confirmed by the >5 times better retention

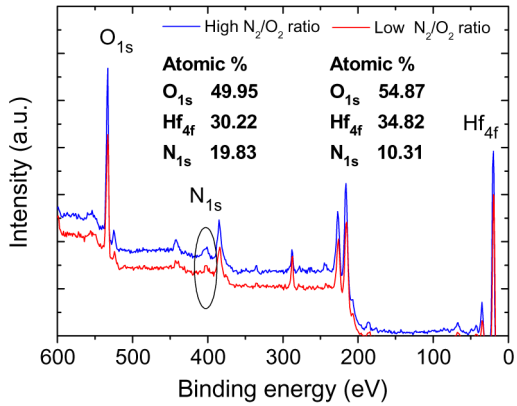


Fig. 2. XPS spectra of $Hf_{1-x-y}N_xO_y$, where the composition of $Hf_{0.30}N_{0.20}O_{0.50}$ and $Hf_{0.35}N_{0.10}O_{0.55}$ was determined from the data.

when using GaN instead of SiN, as suggested by the data from Samsung [16] and also verified by previously reported SiO_2/AlN/HfAlO/TaN [11] and SiO_2/AlGaN/$AlLaO_3$/TaN [12] MONOS memory devices. However, the P/E voltage is still relatively high compared with the target of 4.0–4.5 V for MONOS devices by the year 2018, according to the ITRS roadmap [1]. Such a low voltage operation (under 5 V) is also important for embedded SoC. To continue the improvement of memory device characteristics—in terms of lower P/E voltage and increased speed—we have proposed the use of HfON instead of Al(Ga)N. This is because of the twice as high κ value compared with Al(Ga)N, which reduces the P/E voltage and improves the speed. This is demonstrated experimentally by the low 8-V P/E voltage over the gate channel (or half that, ± 4 V, by using an inverter circuit and applying the different polarity voltages to the gate and the channel) and the <100-μs P/E speed [13]. Improved retention can be achieved by lowering the ΔE_C, which may be accomplished by increasing the N content in the HfON [17]. This has been confirmed by recent measurements of the conduction band offset of 0.7 eV for $Hf_{0.3}N_{0.2}O_{0.5}$ [18]—which is significantly lower than the 1.5-eV value for HfO_2.

B. P/E Characteristics

We first determined the N composition in the $Hf_{1-x-y}N_xO_y$. Fig. 2 shows the XPS spectra of $Hf_{1-x-y}N_xO_y$ with two different N_2/O_2 flow rates. The existence of Hf, N, and O is clear in the XPS spectra, where the compositions were determined to be $Hf_{0.35}N_{0.10}O_{0.55}$ and $Hf_{0.30}N_{0.20}O_{0.50}$ ($Hf_{0.3}N_{0.2}O_{0.5}$ in short). This was done by performing a Compass software calculation on the measured XPS data. These two compositions of the $Hf_{1-x-y}N_xO_y$ trapping layer MONOS devices were used in the following studies.

Fig. 3(a) and (b) shows the C–V hysteresis characteristics of the MONOS capacitor with different trapping layers of $Hf_{0.35}N_{0.10}O_{0.55}$ and $Hf_{0.3}N_{0.2}O_{0.5}$, respectively. The C–V hysteresis window increases with increasing voltage, indicating the good charge storage. The C–V hysteresis window of 2.4 and 6.5 V was measured under swept voltages of ± 10 V in $Hf_{0.35}N_{0.10}O_{0.55}$ and $Hf_{0.3}N_{0.2}O_{0.5}$, respectively. A similar capacitance density of $\sim$4.2 fF/μm^2, found in both devices,

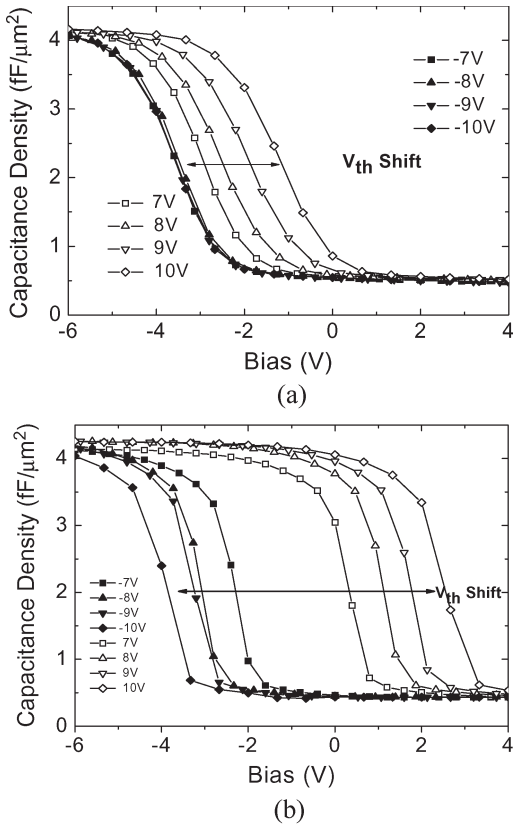


Fig. 3. C–V hysteresis curves for a TaN/HfLaON/$Hf_{1-x-y}N_xO_y$/SiO_2/Si MONOS device with (a) $Hf_{0.35}N_{0.10}O_{0.55}$ and (b) $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layers.

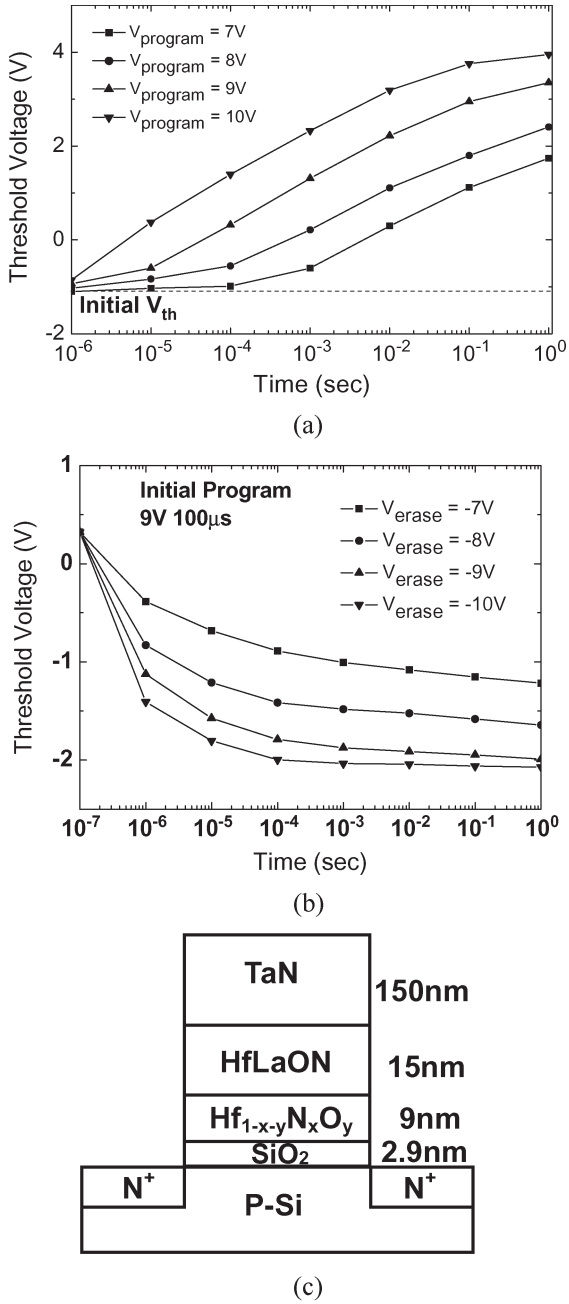


Fig. 4. Measured (a) program and (b) erase characteristics of TaN/HfLaON/$Hf_{0.35}N_{0.10}O_{0.55}$/$SiO_2$/Si MONOS transistors, where the device structure is shown in (c).

ensures that the large hysteresis window was not due to process variations in the MONOS structure. Hence, the large increase in hysteresis window must be due to the different $Hf_{1-x-y}N_xO_y$ trapping layer in the MONOS, which then suggests a higher trap density and/or deeper trap energy in $Hf_{1-x-y}N_xO_y$ with increasing N/O ratio [11], [13].

The P/E characteristics at various gate voltages are shown in Figs. 4 and 5 for $Hf_{0.35}N_{0.10}O_{0.55}$ and $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layer MONOS devices, respectively. The P/E functions were achieved through a Fowler–Nordheim tunneling mechanism, where a positive or negative voltage pulse, with various pulse widths, was applied between the gate and the channel. During programming, an electron inversion channel was formed by biasing the source–drain electrodes, where the positive gate-channel bias voltage permitted inversion electron injection into the trapping layer.

In both cases, the threshold voltage $(V_{\rm th})$ increases with increasing P/E voltage and time—this is typical for MONOS memory devices. For the $Hf_{0.35}N_{0.10}O_{0.55}$ trapping layer MONOS device, a memory window of 2.1 V was obtained at $\pm$9 V for only 100-μs P/E. For comparison, the $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layer MONOS device showed a larger $\Delta V_{\rm th}$ memory window of 2.6 V at a lower P/E voltage of $\pm$8 V under 1-ms/100-μs speed, which increases to 2.8 V at $\pm$9-V 100-μs P/E. The larger memory window suggests a higher trap density in the $Hf_{1-x-y}N_xO_y$ with the higher N composition. This result compares well with our previous TaN/AlHfO/HfON/SiO_2/Si devices that had a thicker trapping layer [13]. The low P/E voltage indicates a small voltage drop in the HfLaON($\kappa = 22$)$-$$Hf_{0.3}N_{0.2}O_{0.5}$($\kappa \sim 22$), leading to fast P/E functions due to the large electric field over the SiO_2 tunnel layer. Such a low P/E voltage is valuable for under 5-V embedded SoC operation, where an inverter circuit with opposite polarities of 4 $\sim$ 4.5 V can be used between the gate and the channel [13].

C. Data Retention and Endurance

Data retention is one of the most important parameters for nonvolatile memory. Fig. 6 shows the retention behavior of the $Hf_{0.35}N_{0.10}O_{0.55}$ trapping layer MONOS device. The initial $\Delta V_{\rm th}$ was 2.1 V under 100 μs and $\pm$9-V P/E, and the

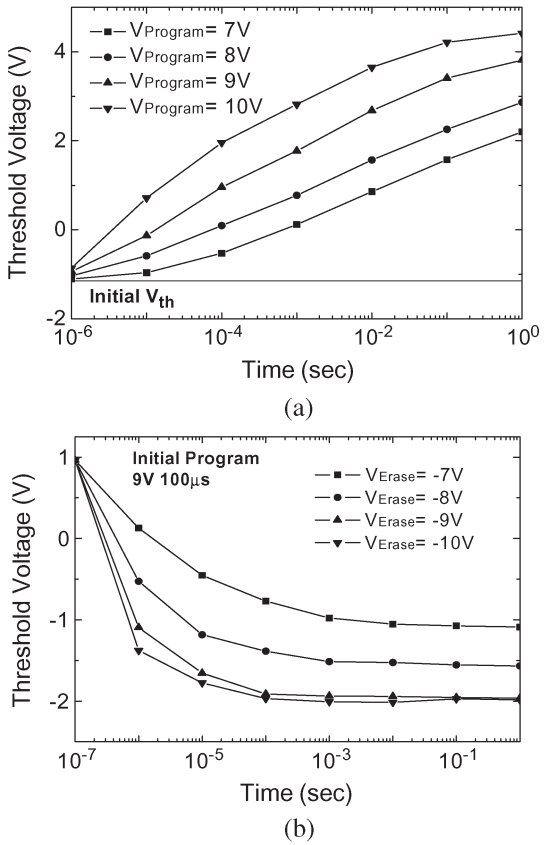


Fig. 5. Measured (a) program and (b) erase characteristics of TaN/HfLaON/$Hf_{0.3}N_{0.2}O_{0.5}/SiO_2/Si$ MONOS transistors.

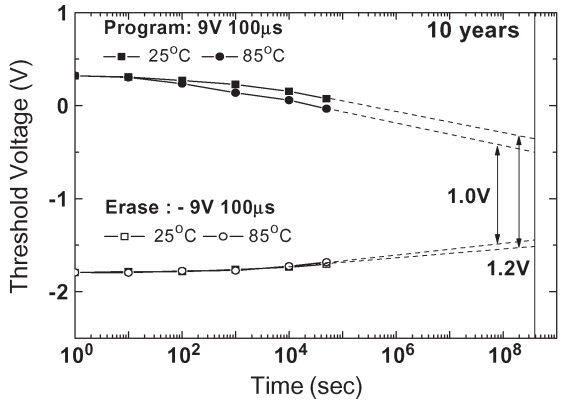


Fig. 6. Retention characteristics of TaN/HfLaON/$Hf_{0.35}N_{0.10}O_{0.55}/SiO_2$/Si devices at 25 °C and 85 °C.

extrapolated ten-year memory windows were 1.2 and 1.0 V at 25 °C and 85 °C, respectively. The good retention is due to the small decay rate of 98 and 42 mV/dec at 85 °C for the high and low states, respectively.

For comparison, in Fig. 7(a) and (b), we show the retention data of a $Hf_{0.3}N_{0.2}O_{0.5}$ MONOS device at 25 °C and 85 °C−125 °C, respectively. The extrapolated ten-year memory window at 25 °C increased from 1.7 to 2.1 V with increasing P/E conditions from ±8 V 500 μs/100 μs to ±9 V 100 μs/100 μs. At 85 °C, the ten-year window was still large at 1.8 V under 100-μs ±9-V P/E. Even at 125 °C, a 1.5-V ten-year window was obtained. Therefore, not only the room temperature but also the high-temperature retention characteristics can be improved by using a higher N% $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layer in a MONOS device than one with a $Hf_{0.35}N_{0.10}O_{0.55}$ composition. The decay rates were 52, 92, and 110 mV/dec for the high state and 27, 36, or 55 mV/dec for the low state under 100-μs ±9-V P/E at 25 °C, 85 °C, and 125 °C, respectively. This is an improvement compared with other devices having a thin tunnel SiO_2, as detailed in Table I [5]–[7], [11]–[13]. The 85-°C and 125-°C retention decay rates are also better than the previous deep-trap AlGaN and HfON data [11]–[13]. Improved retention characteristics could thus be expected.

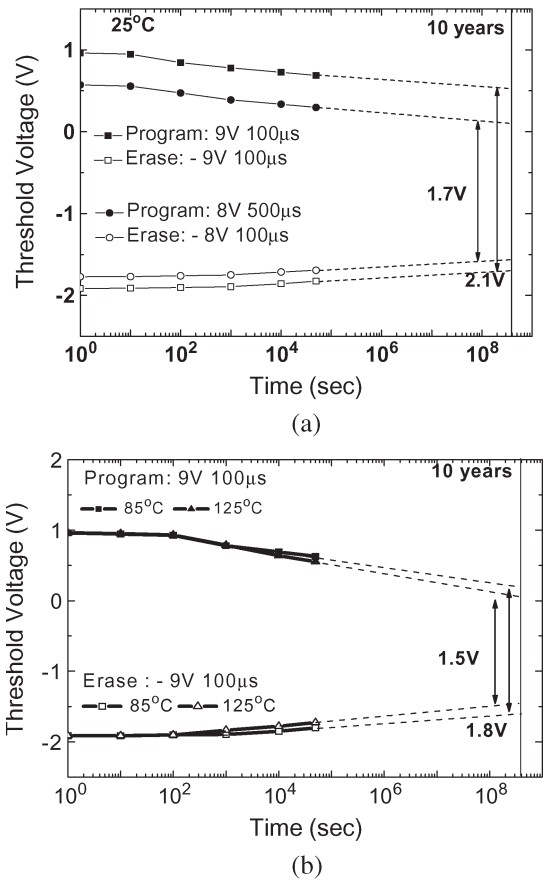


Fig. 7. Retention characteristics of TaN/HfLaON/$Hf_{0.3}N_{0.2}O_{0.5}/SiO_2$/Si devices at (a) 25 °C and (b) 85 °C and 125 °C.

We have also measured the endurance characteristics of the TaN/HfLaON/$Hf_{1-x-y}N_xO_y/SiO_2$/Si MONOS devices with the different trapping layers. As shown in Fig. 8, good endurance was obtained—as is evident from the still large memory windows of 2.4 and 1.7 V after 10^5 cycles at ±9-V 100-μs P/E for $Hf_{0.3}N_{0.2}O_{0.5}$ and $Hf_{0.35}N_{0.10}O_{0.55}$ MONOS devices, respectively. The stress-induced degradation of the nonvolatile memory devices is normally related to interface trap generation at the tunnel oxide-Si interface. We suggest that the good cycling characteristics are due to the fast 100-μs P/E functions where less stress is applied to the thin SiO_2 tunnel layer.

To study the possible read disturbance [19], [20], we have measured the device following the gate stress disturbance condition at the current density of 100 $nA/(15\ nm)^2$ [19]. This is because similar low voltage P/E at 10 V/−9 V was also reported in [20] and close to our 9-V/−9-V P/E condition. Fig. 9 shows

TABLE I
COMPARISON OF MEMORY CHARACTERISTICS FOR THE $Hf_{0.3}N_{0.2}O_{0.5}$, $Hf_{0.35}N_{0.10}O_{0.55}$ TRAPPING LAYER MONOS DEVICE WITH OTHER STATE-OF-THE-ART DEVICES

	P/E condition for retention & cycling	Initial ΔV_{th} (V)	ΔV_{th} (V) for 10-years @ 85°C	P/E decay after 10-years @ 85°C	P/E decay after 10-years @ 125°C
This Work $SiO_2/Hf_{0.3}N_{0.2}O_{0.5}$/ HfLaON/TaN	**9V 100μs/ -9V 100μs**	**2.8**	**1.8**	**36%**	**46%**
	10V 100μs/ -10V 100μs	**3.0**	**1.9**	**37%**	**47%**
This Work $SiO_2/Hf_{0.35}N_{0.10}O_{0.55}$/ HfLaON/TaN	**9V 100μs/ -9V 100μs**	**2.1**	**1.0**	**52%**	-
$SiO_2/Si_3N_4/Al_2O_3$/TaN TANOS [5]	13.5V 100μs/ -13V 10ms	4.4	2.07	53%	-
SiO_2/ Si_3N_4/ SiO_2 FinFET SONOS [6]	13V 10μs/ -12V 1ms	4.5	2.4	47%	-
$SiO_2/Si_3N_4/SiO_2$ Tri-gate MONOS [7]	11.5V 3ms/ -11.5V 100ms	1.2	1.1 (@25°C)	8% (@25°C)	-
SiO_2/AlN/AlHfO/IrO_2 [11]	13V 100μs/ -13V 100μs	3.7	1.9	48%	-
SiO_2/AlGaN/$AlLaO_3$ [12]	11V100μs/ -11V 100μs	3.0	1.6	46%	-
SiO_2/HfON/AlHfO/TaN [13]	8V 100μs/ -8V 100μs	2.5	1.45	42%	60%

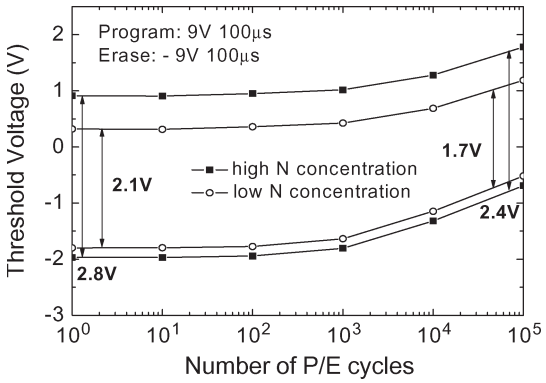


Fig. 8. Endurance characteristics of TaN/HfLaON/$Hf_{1-x-y}N_xO_y/SiO_2/Si$ MONOS devices with different $Hf_{0.3}N_{0.2}O_{0.5}$ and $Hf_{0.35}N_{0.10}O_{0.55}$ trapping layers.

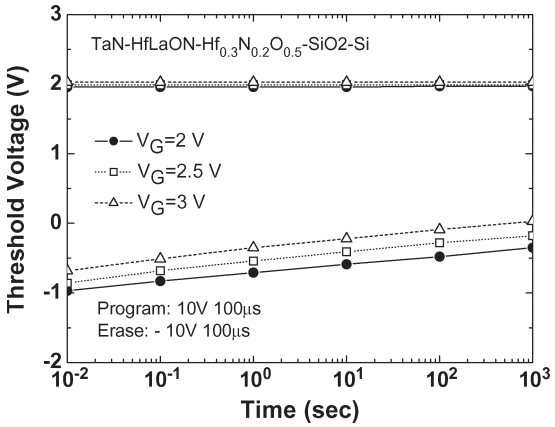
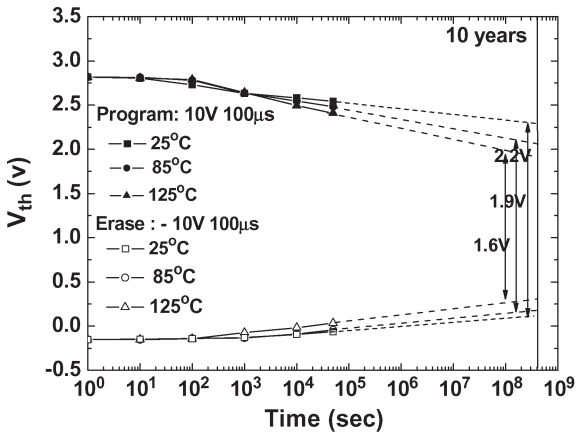
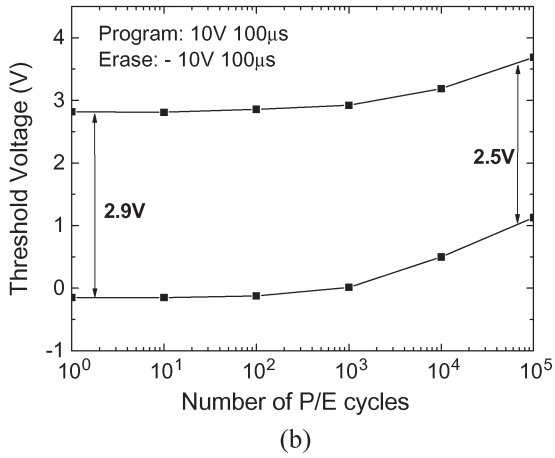


Fig. 9. Gate stress disturbance of TaN/HfLaON/$Hf_{0.3}N_{0.2}O_{0.5}/SiO_2/Si$ device.



(a)



(b)

Fig. 10. (a) Retention and (b) endurance characteristics of TaN/HfLaON/ $Hf_{0.3}N_{0.2}O_{0.5}/SiO_2/Si$ devices at 10-V and 100-μs P/E.

charge retention in gate stress conditions of our memory device, where the P/E voltage is increased to higher 10 V/−10 V. The stored charges were not lost largely as evident from the small $V_{\rm th}$ change even after 1000-s gate stresses. Therefore, similar to a previous conclusion [19], the read disturbance is not a severe concern. The retention and endurance characteristics of TaN/HfLaON/$Hf_{0.3}N_{0.2}O_{0.5}$/SiO_2/Si devices at worse 10-V and 100-μs P/E were shown in Fig. 10(a) and (b), respectively.

Table I shows the comparison of the memory device data. The SiO_2/$Hf_{0.3}N_{0.2}O_{0.5}$/HfLaON/TaN device shows good integrity in terms of its 100-μs P/E speed, low $\pm$9-V P/E voltage, large 2.8-V initial $\Delta V_{\rm th}$, and good ten-year memory window of 1.8 V at 85 °C or 1.5 V at 125 °C. The 36%–46% retention decay rates at 85 °C−125 °C are among the best in Table I [5]–[7], [11]–[13].

IV. Conclusion

Improved memory performance in a MONOS device has been obtained by using a high N/O ratio $Hf_{0.3}N_{0.2}O_{0.5}$ dielectric as the trapping layer. Compared with devices using a low N/O ratio $Hf_{0.35}N_{0.10}O_{0.55}$ layer, the $Hf_{0.3}N_{0.2}O_{0.5}$ MONOS devices showed a wider memory window and a smaller high-temperature decay rate. Our TaN/HfLaON/$Hf_{0.3}N_{0.2}O_{0.5}$/SiO_2/Si MONOS device has potential for nonvolatile memory applications.

Acknowledgment

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