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Guest Editorial: Special Issue on Design and Programming of Signal Processors for Multimedia Communication

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This special issue addresses some of the technical challenges in the design and programming of signal processors for multimedia communication. The past decade has witnessed astonishing growth in Internet usage, penetration of mobile phone service, and proliferation of communication-ready portable devices. All these are whetting the appetite of the populace for more convenient and ubiquitous access to multimedia information, at a higher quality than previously available. The development of terminal equipment to meet such demand presents a significant technical challenge, considering that it is highly desirable that the equipment be cost effective, power efficient, versatile, and extensible for future upgrades. Over time, signal processors have become an indispensable part in such equipment. For example, a recent study shows that 90% of the SoC products in 130 nm technology have at least one programmable processor. Nonetheless, there are challenges in the design and programming of signal processors for multimedia communication, in particular, (1) general-purpose signal processor design, (2) application-specific signal processor design, (3) operating systems and programming support, and (4) application programming. To address the concerns, six papers are included in this special issue.

This issue opens with two general-purpose signal processor designs. To meet the diverse computing requirements while achieving high computational and energy efficiencies, the system architectures presented here provide desired features via two different approaches: (1) novel micro-architecture in the DSP cores and (2) reconfiguring computational circuits.

- In "Design and Implementation of a High-Performance and Complexity-Effective VLIW DSP for Multimedia Applications," Lin et al. present a novel signal processor design for high computational efficiency and low cost. It has a ping-pong register file design where 16 data registers are dynamically partitioned into ping and pong banks. The ping-pong register file design saves significant silicon area and access time over a traditional centralized design. The design also has a hierarchical instruction encoding scheme which could further reduce the code size.
- In "Implementation of a Coarse-Grained Reconfigurable Media Processor for AVC Decoder," Mei et al. describe a special kind of signal processor architectures, which combines a reconfigurable architecture and a VLIW engine. Additionally, the paper presents a comprehensive solution, including a C-based compilation flow, VLSI design evaluation and FPGA-based emulation. Detailed performance analysis of an H.264 video decoder design is conducted to illustrate its capability. The paper demonstrates the benefit of coarse-grained reconfigurable processor and the feasibility of a C-based design flow.

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In addition to high flexibility to a broad domain of application, an alternative approach is to build an application-specific signal processor. In this case, it can deliver the required performance with the lowest cost or highest efficiency.

- In "An Area-Efficient Design of Variable-Length Fast Fourier Transform Processor," Wang and Li describe an area-efficient design of a variable-size FFT processor. The size of FFT is programmable so that it can be used for various OFDM-based communication systems, such as digital audio broadcasting (DAB), digital video broadcasting-terrestrial (DVB-T) and digital video broadcasting- handheld (DVB-H). To make the processor area-efficient, it reduces the number of non-trivial multipliers and optimizes the realization by substructure sharing.

Beyond the underlying hardware and software to run on the hardware, it is also important to have operating systems and programming support.

- In "Enhancing Microkernel Performance on VLIW DSP Processors via Multiset Context Switch," Hsieh et al. propose a mechanism for reducing the context switch overhead. The proposed optimization scheme implements a probability cost model in the compiler to partition the registers based on the life range information. When the contexts are divided into several sets, the OS can just save and restore part of the registers instead of the whole context when performing task switching.
- In "Effective Code Generation for Distributed and Ping-Pong Register Files: A Case Study on PAC VLIW DSP Cores," Lin et al. discuss the compiler design for the PAC DSP. The clustered architecture design and distributed ping-pong register files in the PAC DSP raise new challenges of code generation. Thus, the authors develop a new register allocation scheme based on simulated annealing and other retargeting optimization phases that achieve effective code generation.

This issue concludes with one application case study to illustrate the application programming issues and solutions on a modern DSP.

- In "Algorithm and Software Optimization of Variable Block Size Motion Estimation for H.264/AVC on a VLIW-SIMD DSP," Lee et al. discuss the design and programming of variable block size motion estimation for H.264 on Texas Instruments' DSP. The authors demonstrate several techniques, e.g., loop length increase, non-aligned memory load reduction, and pack/unpack minimization, to optimize the performance by one order of magnitude. Software engineers, who work on media processing, can use these techniques to improve the implementation.

In short, we hope that this Special Issue provides enlightening information to the community in a timely fashion on the design and programming of signal processors for multimedia communication. We would like to thank the authors for their excellent contribution. We also appreciate the reviewers for their constructive comments.