Characterizing Fluorine-Ion Implant Effects on Poly-Si Thin-Film Transistors With Pr_2O_3 Gate Dielectric

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***Abstract*—The fluorine ion implantation applied to the polycrystalline silicon thin-film transistors (poly-Si TFTs) with high-κ Pr_2O_3 as gate dielectric is investigated for the first time. Using the Pr_2O_3 gate dielectric can obtain a high gate capacitance density and thin equivalent-oxide thickness, exhibiting a greatly enhancement in the driving capability of TFT device. Introducing fluorine ions into the poly-Si film by fluorine ion implantation technique can effectively passivate the trap states in the poly-Si film and at the Pr_2O_3/poly-Si interface to improve the device electrical properties. The Pr_2O_3 TFTs fabricated on fluorine-implanted poly-Si film exhibit significantly improved electrical performances, including lower threshold voltage, steeper subthreshold swing, higher field-effect mobility, lower off-state leakage current, and higher on/off current ratio, as compared with the control poly-Si Pr_2O_3 TFTs. Also, the incorporation of fluorine ions also improves the reliability of poly-Si Pr_2O_3 TFTs against hot-carrier stressing, which is attributed to the formation of stronger Si-F bonds. Furthermore, superior threshold-voltage rolloff characteristic is also demonstrated in the fluorine-implanted poly-Si Pr_2O_3 TFTs. Therefore, the proposed scheme is a promising technology for high-performance and high-reliability solid-phase crystallized poly-Si TFT.**

***Index Terms*—Fluorine–ion implantation, high-κ gate dielectric, Praseodymium oxide (Pr_2O_3), thin-film transistors (TFTs).**

I. Introduction

In RECENT years, low-temperature polycrystalline silicon thin-film transistors (poly-Si TFTs) have been widely used in active-matrix liquid crystal displays (AMLCDs) [1], [2]. Poly-Si TFTs have many advantages, including higher driving current and greater field-effect mobility, compared with conventional amorphous silicon thin-film transistors (α-Si TFTs). To realize the system-on-panel (SOP) purpose, the capability of integrating not only pixel switching elements but also peripheral driving circuits on single glass substrate is also attractive [3]. The complicated process can be remarkably simplified and thus the production cost can be reduced. To fabricate poly-Si TFTs on low-melting point glass substrates, low-temperature technology is required for accomplishing commercial flat-panel displays due to the maximum process temperature limiting to 600 °C. The solid-phase crystallization (SPC) technique was widely utilized for phase transformation from amorphous to polycrystalline due to its low fabrication cost and good grain-size uniformity [4]. However, it is difficult to develop high-performance and high-reliability poly-Si TFTs that are applicable for both pixel switching elements and peripheral driving circuits. Pixel switching elements require TFTs to operate at high voltage with low gate-leakage currents to drive the liquid crystal. In contrast, TFTs with good electrical properties, including low operation voltage, low subthreshold swing, high driving currents, and low gate-leakage currents are necessary for achieving display driving circuits. However, the SPC poly-Si TFTs with traditional SiO_2 gate dielectrics exhibit inferior electrical characteristics, including low field-effect mobility, high subthreshold swing, and low driving currents, which could not meet the requirement of peripheral driving circuits. Poly-Si TFTs with continuously scaling down of the SiO_2 gate dielectrics can improve the subthreshold characteristics and driving current capability, but may induce gate-dielectric degradation and poor dielectric breakdown property to unavoidably degrade the electrical reliability [5].

In order to address these issues, poly-Si TFTs incorporating high dielectric constant (high-κ) materials as gate dielectrics are able to increase the gate capacitance density and then enhance the mobile carrier density in the poly-Si channel region. To reach the same gate capacitance density, the physical thickness of high-κ gate dielectrics can be thicker than that of SiO_2 gate dielectrics. Therefore, integrating high-κ gate dielectrics into poly-Si TFTs can maintain high driving currents and suppressed gate-leakage currents. Several new high- κ materials, including oxide–nitride–oxide (ONO) gate stack, Al_2O_3, and Ta_2O_5, have been proposed replacing traditional SiO_2 as the gate dielectrics of poly-Si TFTs [6]–[8]. However, the performance enhancement on the poly-Si TFTs with ONO gate stack, Al_2O_3, and Ta_2O_5 gate dielectrics is finite. This can be ascribed to that the dielectric constant of ONO gate stack and Al_2O_3 gate dielectric is not high enough $(\kappa < 9)$ as well as the bandgap of Ta_2O_5 gate dielectric is too narrow. In the recent studies, praseodymium oxide (Pr_2O_3) material has been demonstrated to possess outstanding electrical and crystallographical properties, including high dielectric constant of about 31, low gate-leakage current, symmetric band alignment, and excellent thermal stability in contact with Si, which render this material an interesting alternative to the more studied hafnium oxide (HfO_2) [9], [10]. Poly-Si TFT incorporating Pr_2O_3 as gate dielectric has been proposed in our previous work [11], which addressed the issues mentioned previously.

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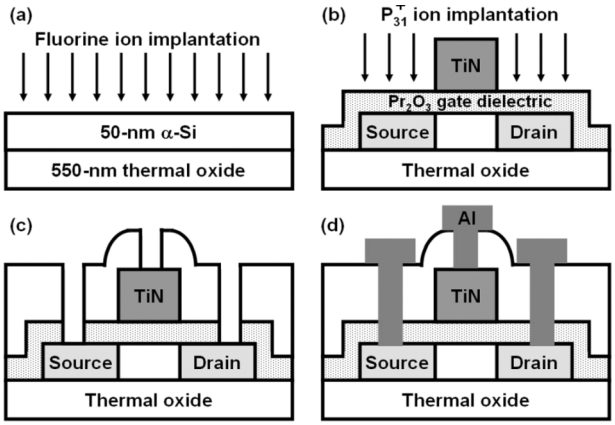

Fig. 1. Schematic diagrams of the key fabrication steps for the proposed poly-Si TFT incorporating Pr_2O_3 gate dielectric on fluorine-implanted poly-Si film.

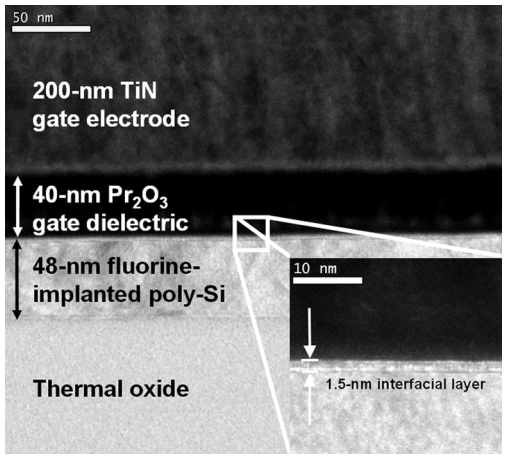

Fig. 2. Cross-sectional TEM image of the proposed poly-Si TFT structure.

However, poly-Si TFTs with high-κ gate dielectrics would suffer from more undesirable off-state gate-induced drain leakage (GIDL) currents, resulted from the higher field-enhanced emission rate via the grain-boundary trap states [12]. To resolve this GIDL current issue, several methods have been proposed to reduce the trap state density. The commonly applied passivation methods are hydrogen-based plasma treatment and fluorine ion implantation technique. Hydrogen plasma treatment is widely used to passivate the trap states to suppress the undesirable GIDL currents, but it is difficult to control the optimal processing time for satisfactory performance improvement [13]. Also, the hydrogenated poly-Si TFTs also suffer from a serious instability of electrical properties under long-term electrical stress, which is attributed to the weak Si–H bonds [14]. Another promising strategy, fluorine ion implantation, has been utilized to improve the device performance by eliminating the trap states at the grain boundaries [15], [16]. In addition, strong Si–F bonds, more stable than Si–H bonds, can significantly improve the device reliability under long-term electrical stress.

In this paper, Pr_2O_3 gate dielectric TFTs on fluorine-implanted poly-Si films have been successfully fabricated and their device characteristics and reliability have been characterized. The proposed scheme is a simple, low-cost ,and process-compatible technology to achieve high-performance and high-reliability solid-phase crystallized poly-Si TFTs.

II. Experimental Procedures

Fig. 1 schematically depicts the major fabrication processes for the proposed fluorine-implanted poly-Si Pr_2O_3 TFT. First, a 50-nm undoped amorphous silicon (α-Si) layer was deposited on a thermally oxidized Si wafer by dissociation of SiH_4 gas in a low-pressure chemical vapor deposition (LPCVD) system at 550 °C. Following, the fluorine ion implantation was realized with the accelerating energy and dosage at 10 keV and 5×10^{12} cm^{-2}, respectively [see Fig. 1(a)]. The fluorine ions were implanted into the α-Si layer without pad oxide on, and the projected fluorine-ion range was located at the middle of the α-Si film. Subsequently, a solid-phase crystallization (SPC) process was performed at 600°C for 24 h in N_2 ambient for Si phase transformation from amorphous to polycrystalline and dopant activation of fluorine ions. Individual active regions were patterned and defined. After standard RCA cleaning, a 40-nm Pr_2O_3 gate dielectric was deposited by electron-beam evaporation system and then densified at 600 °C for 30 min in O_2 ambient to improve the gate-dielectric property. A 200-nm TiN film was deposited, followed by the dry etching of TiN gate electrode stopping on the Pr_2O_3 layer. A self-aligned phosphorous ion implantation was performed with the dosage and energy of 5×10^{15} cm^{-2} and 70 keV, respectively [see Fig. 1(b)]. The dopant was activated at the thermal budget of 600°C for 30 min in N_2 ambient, followed by the deposition of a 300-nm low-temperature passivation SiO_2 layer and the definition of contact holes. The contact holes opening was performed with the selective wet etching of passivation SiO_2 layer and Pr_2O_3 dielectric film by buffered oxide etch (BOE) and H_2SO_4–H_2O_2 solutions, respectively [Fig. 1(c)]. Finally, a 400-nm Al electrode was deposited and patterned [Fig. 1(d)]. The control poly-Si Pr_2O_3 TFT without fluorine ion implantation step was also prepared. To concentrate on the fluorine passivation effect of the trap states, no additional hydrogen plasma treatment and thermal sintering processes were performed after the Al electrode formation. The electrical and reliability characteristics were performed using an HP 4156B.

III. Results and Discussion

The cross-sectional transmission electron microscopy (XTEM) image of the proposed poly-Si TFT integrating TiN gate electrode and Pr_2O_3 gate dielectric is depicted in Fig. 2. From the XTEM image, the physical thicknesses of the Pr_2O_3 gate dielectric and the poly-Si channel are around 40 and 48 nm, respectively. The higher resolution XTEM image near the Pr_2O_3/poly-Si interface displayed in the inset of Fig. 2 exhibits an around 1.5-nm SiO_2-like interfacial layer between the Pr_2O_3 gate dielectric and poly-Si channel. A metal-oxide-semiconductor (MOS) capacitor structure using Pr_2O_3 as gate dielectric on single-crystalline Si was prepared to investigate the electrical properties of Pr_2O_3 gate dielectric. Fig. 3 shows typical capacitance–voltage (*C–V*) characteristic of the MOS capacitor at 1 MHz. The MOS capacitor has the same gate-dielectric thickness as the proposed TFT device

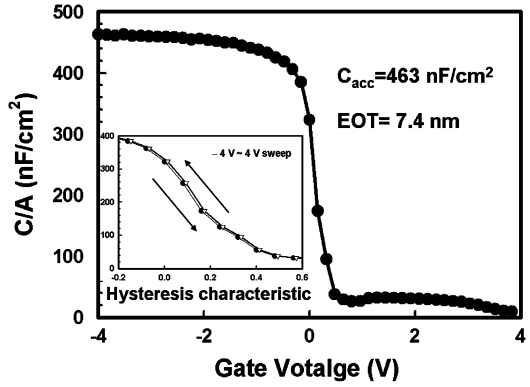

Fig. 3. Typical *C-V* characteristic of the Pr_2O_3 gate dielectric. The inset figure shows the hysteresis characteristic.

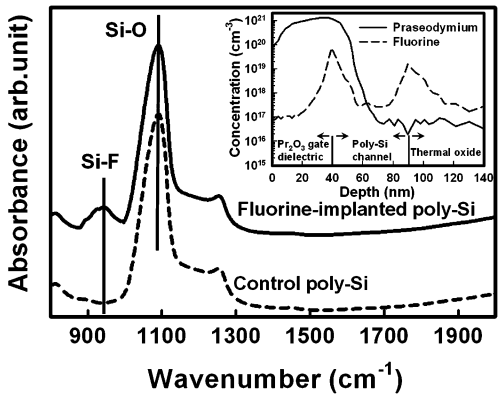

Fig. 4. FTIR spectra of the poly-Si films with and without fluorine ion implantation. The inset shows the SIMS profiles of fluorine and praseodymium atoms for the fluorine-implanted poly-Si film.

has. An accumulation gate capacitance density (C_{acc}) at an applied voltage of $V_{GS} = -4$ V is 463 nF/cm^2. Therefore, the equivalent-oxide thickness (EOT) of the MOS capacitor with Pr_2O_3 gate dielectric extracted from the accumulation gate capacitance density is 7.4 nm. The effective dielectric constant value of Pr_2O_3 gate dielectric was extracted by using the series capacitor model with a series connection of high-κ and SiO_2-like interfacial layer [17]. The effective dielectric constant value of Pr_2O_3 film is extracted to be 26 by assuming the dielectric constant value of SiO_2-like interfacial layer to be 3.9. The hysteresis of *C–V* characteristic is also shown in the inset of Fig. 3. The *C–V* characteristic for hysteresis extraction was measured by sweeping the voltage from accumulation to inversion (-4 to 4 V) and then sweeping back (4 to -4 V). The Pr_2O_3 gate dielectric demonstrates negligible hysteresis characteristic of 7.2 mV, indicating it is a promising gate-dielectric candidate for poly-Si TFT.

Fourier transform infrared (FTIR) spectroscopy and secondary ion mass spectroscopy (SIMS) analysis were utilized to verify the fluorine existing in the poly-Si film. The FTIR spectra of the fluorine-implanted and control poly-Si films after SPC process are shown in Fig. 4. The main peak of the functional group Si-F bonds is clearly observed at around 930 cm^{-1} in the fluorine-implanted poly-Si film [18]. The stronger peak of Si-O bond is derived from the bottom thermal SiO_2 substrate. Therefore, Si-F bonds are formed in the poly-Si film by utilizing fluorine ion implantation. Moreover, the inset in Fig. 4 shows the SIMS profiles of fluorine and praseodymium atoms for the fluorine-implanted poly-Si film. It was apparently observed that considerable fluorine ions were detected in the poly-Si film and, in particular, two obvious fluorine peaks were piled up at the Pr_2O_3 gate dielectric/poly-Si channel and the poly-Si channel/bottom thermal SiO_2 interfaces. Note that the incorporated and piled-up fluorine ions in the poly-Si film and at the Pr_2O_3/poly-Si interface would bring about an effective passivation of deep trap states and interface states, resulting in fewer Si dangling bonds and Si strain bonds.

Fig. 5 shows the transfer characteristics $(I_{DS}-V_{GS})$ of the poly-Si Pr_2O_3 TFTs with and without fluorine ion implantation. The measurements are performed at two different drain voltages of $V_{DS} = 0.1$ V and 1 V. The drawn channel width (W) and channel length (L) are 10 μm and 5 μm, respectively. The parameters of the devices, including the threshold voltage (V_{th}),

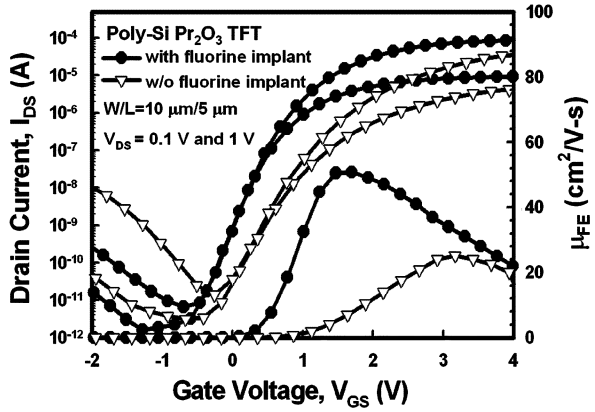

Fig. 5. Transfer characteristics of the poly-Si Pr_2O_3 TFTs with and without fluorine ion implantation.

TABLE I
ELECTRICAL CHARACTERISTICS COMPARISON OF THE FLUORINE-IMPLANTED AND CONTROL POLY-SiPr_2O_3 TFTS

Key Parameters	V_{th} (V)	μ_{FE} (cm²/V-s)	S.S. (mV/dec)	$I_{off,max}$ at V_{DS}=1 V V_{GS}= −2 V	I_{on}/I_{off} at V_{DS}=1 V
Fluorine-implanted Pr_2O_3 TFT	0.65	51.5	216	2.6×10^{-10}	1.6×10^{7}
Control Pr_2O_3 TFT	1.57	25.1	320	1.2×10^{-8}	3.4×10^{6}

field-effect mobility (μ_{FE}), and subthreshold swing (S.S.) are extracted at $V_{DS} = 0.1$ V, whereas the maximum off-state leakage current $(I_{off,max})$ and maximum on-state current (I_{on}) are defined at $V_{DS} = 1$ V. The on/off current ratio (I_{on}/I_{off}) is defined as the ratio of the maximum on-state current to the minimum off-state leakage current at $V_{DS} = 1$ V. The threshold voltage is defined as the gate voltage required to achieve a normalized drain current of $I_{DS} = (W/L) \times 100$ nA. The detailed device parameters of the fluorine-implanted and control poly-Si Pr_2O_3 TFTs are summarized in Table I.

Accordingly, the electrical performance of the fluorine-implanted poly-Si Pr_2O_3 TFT is remarkably improved compared to that of the control poly-Si Pr_2O_3 TFT. With the fluorine ion

implantation, the poly-Si Pr_2O_3 TFT exhibits significant performance improvements in terms of drastically decreased threshold voltage from 1.57 to 0.65 V and reduced subthreshold swing from 320 to 216 mV/dec. It is known that the deep trap states, associated with the Si dangling bonds, accompanied with many energy states near the middle of Si bandgap, would strongly affect the threshold voltage and subthreshold swing [13]. Therefore, introducing fluorine ions into the poly-Si film by using fluorine ion implantation can effectively terminate the deep trap states at the grain boundaries. In addition, the maximum on-state current and on/off current ratio of the fluorine-implanted poly-Si Pr_2O_3 TFT are also superior to those of the control poly-Si Pr_2O_3 TFT. The corresponding on/off current ratios for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs are 1.6×10^7 and 3.4×10^6, respectively. The on/off current ratio of the fluorine-implanted poly-Si Pr_2O_3 TFT is approximately five times larger than that of the control poly-Si Pr_2O_3 TFT.

Fig. 5 also shows the relation between the field-effect mobility and the gate voltage for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs. The field-effect mobility is extracted from the transconductance value at $V_{DS} = 0.1$ V. As can be seen, the maximum field-effect mobility of the fluorine-implanted poly-Si Pr_2O_3 TFT is higher than that of the control poly-Si Pr_2O_3 TFT. With the fluorine ion implantation, the poly-Si Pr_2O_3 TFT shows approximately 105% enhancement in the maximum field-effect mobility. Note that the tail states near the bandedge resulted from the strain bonds in the poly-Si and at the Pr_2O_3/poly-Si interface would greatly affect the field-effect mobility [13]. This feature implies that the fluorine ion implantation treatment can not only passivate the Si dangling bonds but also relieve the Si strain bonds. The proposed poly-Si TFTs crystallized by SPC technique can demonstrate good electrical performances even without additional hydrogen plasma treatment or other advanced phase crystallization techniques with narrow process window [19], [20].

However, incorporating high-κ gate dielectric into poly-Si TFT would contribute to a higher electric field at the gate-to-drain overlap area, exhibiting a higher field-enhanced emission rate via the grain-boundary trap-states. Thus, the control poly-Si Pr_2O_3 TFT would suffer from more undesirable gate-induced drain leakage (GIDL) currents, especially under continuously decreasing gate voltage. The GIDL current of the fluorine-implanted poly-Si Pr_2O_3 TFT (2.6×10^{-10}) is much lower than that of the control poly-Si Pr_2O_3 TFT (1.2×10^{-8}), under applied voltages of $V_{GS} = -2$ V and $V_{DS} = 1$ V. This observation suggests that the incorporation of fluorine ions into the poly-Si film can effectively passivate the trap states, thereby resulting in lower GIDL currents under a high electric field.

In order to verify the effect of fluorine passivation, the grain-boundary trap-state density (N_{trap}) was calculated from the square root of the slope of the $\ln[(I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ plot according to the grain-boundary trapping model proposed by Proano *et al.* [21]. Fig. 6 exhibits the $\ln[(I_{DS}/(V_{GS} - V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ and the extracted grain-boundary trap-state densities at $V_{DS} = 0.1$ V and high gate voltage for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs. It can be found that the fluorine-implanted poly-Si Pr_2O_3 TFT shows a N_{trap} of 4.58×10^{12} cm^{-2},

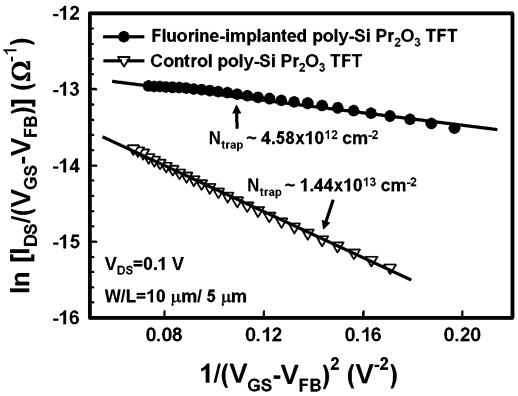

Fig. 6. The $\ln[I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ at $V_{DS} = 0.1$ V and high gate voltage for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs.

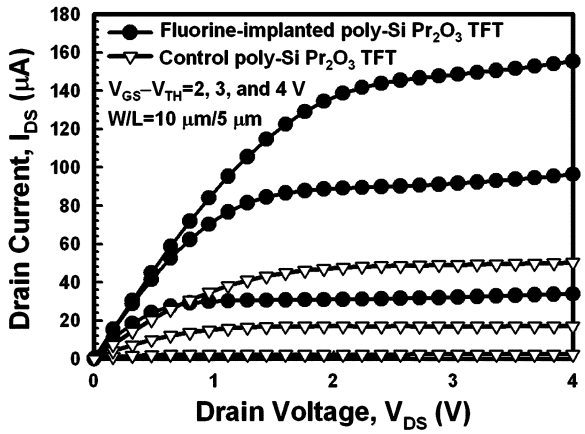

Fig. 7. Output characteristics of the fluorine-implanted and control poly-Si Pr_2O_3 TFTs.

whereas the control poly-Si Pr_2O_3 TFT possesses a N_{trap} of 1.44×10^{13} cm^{-2}. This result implies that the fluorine ions can effectively passivate the present grain-boundary trap states in the poly-Si film, thereby exhibiting improved device performances. Combined with the SIMS profiles, we believe that the passivation effect is due to the piled-up and accumulated fluorine ions at the Pr_2O_3/poly-Si interface and in the poly-Si film.

Fig. 7 shows the output characteristics ($I_{DS}-V_{DS}$) of the fluorine-implanted and control poly-Si Pr_2O_3 TFTs. As can be seen, with the fluorine ion implantation, the poly-Si Pr_2O_3 TFT exhibits a significant enhancement in the on-state driving current under common gate drive of $V_{GS}-V_{TH} = 2, 3$, and 4 V. The fluorine passivation of trap states would result in a higher field-effect mobility, thus exhibiting an obvious improvement on the driving capability. Fig. 8 illustrates the activation energy (E_A) of drain current as a function of gate voltage at $V_{DS} = 1$ V for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs. E_A was extracted by the measurements of $I_{DS}-V_{GS}$ characteristics at various temperatures ranging from 25 °C to 150 °C [22]. E_A represents the carrier transport barrier across the grain boundaries of the poly-Si film. In the turned-off state, the value of E_A reflects the required energy for field-enhanced emission of carriers via the trap states, whereas in the turned-on state, the value of E_A reflects the carrier transport barrier height caused by the

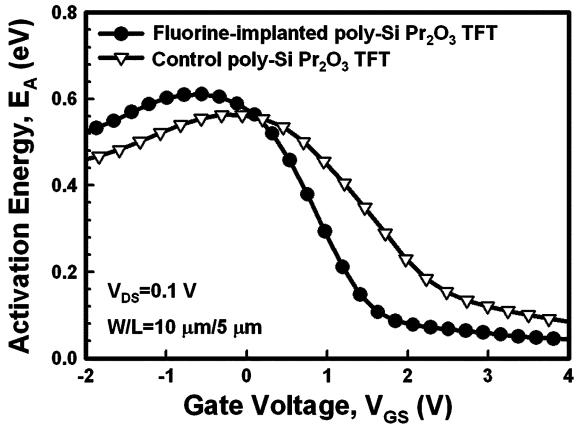

Fig. 8. Activation energy versus gate voltage for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs.

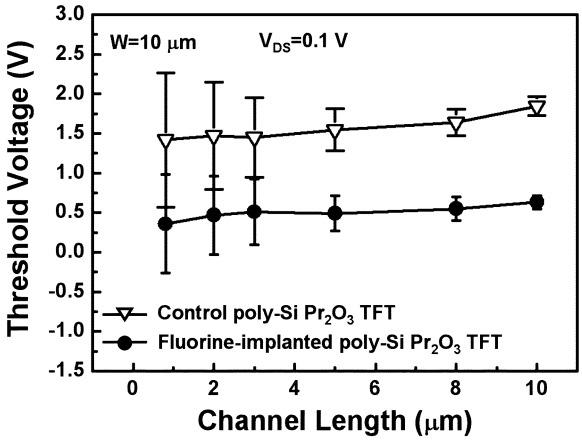

Fig. 9. Threshold voltage rolloff characteristics for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs.

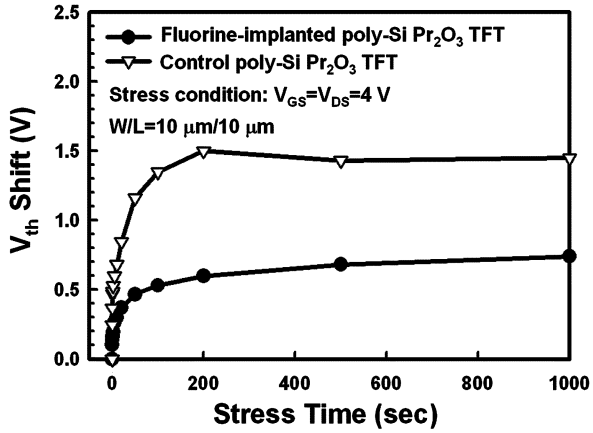

Fig. 10. Threshold-voltage shift over hot-carrier stress time for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs.

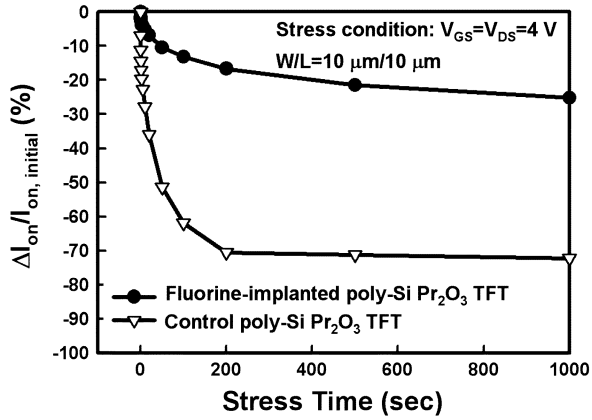

Fig. 11. On-current variation over hot-carrier stress time for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs.

trap states within the poly-Si channel. The fluorine-implanted poly-Si Pr_2O_3 TFT exhibits a higher E_A in the turned-off state, but a lower E_A in the turned-on state, as compared to the control poly-Si Pr_2O_3 TFT. It should be noted that the trap states can be effectively terminated by the incorporation of fluorine ions into the poly-Si film. Moreover, a steeper curve can be found in the subthreshold region for the fluorine-implanted poly-Si Pr_2O_3 TFT, thereby demonstrating well terminated interface states by the fluorine ion implantation. This implication is consistent with the above extracted data of trap state density.

To investigate the short-channel effect of poly-Si Pr_2O_3 TFTs with and without fluorine ion implantation, the average and statistical distributions of threshold voltage as a function of channel length with a fixed channel width of 10 μm are shown in Fig. 9. The number of sampling devices characterized under each condition is 20. The vertical bars in the figure indicate the minimum and maximum values of the devices characteristics and the circle as well as triangular symbol present the average values. The threshold voltage of poly-Si TFTs with traditional SiO_2 gate dielectrics is decreased with continuously scaling down channel length, called the threshold-voltage rolloff effect, dominated by the reduction of grain- boundary trap states [23]. In contrast, the poly-Si Pr_2O_3 TFT with a high gate capacitance density can rapidly fill up the grain-boundary trap states and then maintain superior turned-on characteristics, demonstrating a better threshold-voltage rolloff property. In addition, as the channel length scales down, fluctuations of threshold voltage by the variation of the number of grain boundaries in the poly-Si channel become more significant in the control poly-Si Pr_2O_3 TFT. This is reasonable and is related to the inherent grain structure contained in the poly-Si channels [24]. Therefore, using the fluorine to passivae the trap states can not only decrease the average threshold voltage but also reduce the fluctuation of threshold voltage.

Additionally, hot-carrier stress was performed to investigate the electrical reliability of the fluorine-implanted and control poly-Si Pr_2O_3 TFTs. The TFT devices with a dimension of $W/L = 10\mu\text{m}/10\mu\text{m}$ were bias stressed at $V_{DS} = 4$ V and $V_{GS} = 4$ V for 1000s to examine the hot-carrier stress immunity. The threshold-voltage shift (ΔV_{th}) and on-current variation (δI_{on}) over stressing time for the fluorine-implanted and control poly-Si Pr_2O_3 TFTs are shown in Figs. 10 and 11, respectively. The ΔV_{th} and δI_{on} were defined as $V_{th,\ stressed} - V_{th,\ initial}$ and $(I_{on,\ stressed} - I_{on,\ initial})/I_{on,\ initial} \times 100\%$, respectively, where the index of initial and stressed represents the measured values before and after stresses. Hot-carrier multiplication near the drain side causes the degradation of threshold voltage

and on current. The poly-Si Pr_2O_3 TFT with fluorine ion implantation shows less degradation on threshold voltage and on current. Notably, the threshold-voltage shift and on-current variation of the fluorine-implanted poly-Si Pr_2O_3 TFT after 1000 s stress are found to be 0.7 V and 26 %, which are superior to those of the control poly-Si Pr_2O_3 TFT (1.5 V and 72 %, respectively). It has been reported that the degradation of electrical characteristics induced by hot-carrier stress can be attributed to the following two reasons: the generation of Pr_2O_3/poly-Si interface states and the formation of Si dangling bonds from the breaking of weak Si–Si or Si–H bonds in the poly-Si channel [14]. Therefore, introducing fluorine ions into the poly-Si film by fluorine ion implantation would bring about the passivation of trap states and the formation of strong Si–F bonds in place of weak Si–Si and Si–H bonds, thereby leading to great improvements in the electrical reliability.

IV. Conclusion

We reported integrating an effective fluorine passivation treatment into poly-Si Pr_2O_3 TFT by employing fluorine ion implantation technique. Significant performance improvements on the poly-Si Pr_2O_3 TFT have been demonstrated with the fluorine ion implantation. A lower threshold voltage, lower GIDL current, steeper subthreshold swing, higher field-effect mobility, and higher on/off current ratio can be achieved due to the passivation of trap states in the poly-Si film and at the Pr_2O_3 gate dielectric/poly-Si channel interface. Furthermore, the fluorine-implanted poly-Si Pr_2O_3 TFT also improves the hot-carrier stress immunity, presumably due to the formation of strong Si–F bonds instead of weak Si–Si and Si–H bonds. Besides, superior threshold-voltage rolloff characteristic is also achieved. It is concluded that the integration of fluorine ion implantation and Pr_2O_3 gate dielectric technologies could be available for fabricating high-performance and high-reliability poly-Si TFT even without additional hydrogen plasma treatment or advanced phase crystallization techniques.

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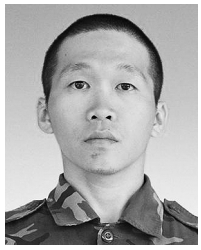

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