High-Performance Metal-Induced Laterally Crystallized Polycrystalline Silicon P-Channel Thin-Film Transistor With TaN/HfO_2 Gate Stack Structure

Ming-Wen Ma, *Student Member, IEEE*, Tien-Sheng Chao, *Senior Member, IEEE*, Chun-Jung Su, *Student Member, IEEE*, Woei-Cherng Wu, *Student Member, IEEE*, Kuo-Hsing Kao, and Tan-Fu Lei, *Member, IEEE*

***Abstract*—In this letter, high-performance low-temperature poly-Si p-channel thin-film transistor with metal-induced lateral-crystallization (MILC) channel layer and TaN/HfO_2 gate stack is demonstrated for the first time. The devices of low threshold voltage $V_{TH} \sim 0.095$ V, excellent subthreshold swing S.S. ~ 83 mV/dec., and high field-effect mobility $\mu_{FE} \sim 240\ cm^2/V \cdot s$ are achieved without any defect passivation methods. These significant improvements are due to the MILC channel film and the very high gate-capacitance density provided by HfO_2 gate dielectric with the effective oxide thickness of 5.12 nm.**

***Index Terms*—High-κ, low-temperature poly-Si thin-film transistor (LTPS-TFT), metal gate, metal-induced lateral crystallization (MILC).**

I. Introduction

HIGH-PERFORMANCE low-temperature poly-Si thin-film transistors (LTPS-TFTs) have been intensively investigated for the application of the active matrix liquid-phase crystal displays [1] and the three-dimensional (3-D) circuit-integration elements such as SRAMs and DRAMs [2], [3]. However, the poly-Si channel film would still have many grain boundaries which degrade the subthreshold swing S.S., threshold voltage V_{TH}, and field-effect mobility μ_{FE} and the results in a large operation voltage [4]–[6]. Hydrogen-related plasma is generally used to passivate these grain boundaries in the poly-Si channel film to have a lower operation voltage of LTPS-TFTs [7]–[9]. Nevertheless, the introduction of hydrogen would also result in the degradation of the reliability of LTPS-TFTs [10], [11]. Recently, high-κ materials such as $HfSiO_x$, HfO_2, $LaAlO_3$, and Al_2O_3 have been used as the gate dielectrics of LTPS-TFTs to enhance the gate-capacitance density, resulting in the improvement of the S.S. and V_{TH} without any hydrogen-related plasma treatments [12]–[15].

The improvement of S.S., V_{TH}, and μ_{FE} of the devices with high-κ gate dielectrics is still not high enough for the application of system-on-panel (SOP) or 3-D circuit integration. Compared with solid-phase-crystallization (SPC) method, excimer laser crystallization (ELC) method is capable of producing poly-Si film with low defect densities and higher μ_{FE} [16]. However, ELC suffers from high initial cost and high process complexity. Metal-induced lateral-crystallization (MILC) method is another batch process with low cost to achieve high μ_{FE} of LTPS-TFTs due to its large grain size and longitudinal grain boundaries [17]–[21].

In this letter, we demonstrate the p-channel LTPS-TFT with TaN gate, HfO_2 gate dielectric, and MILC poly-Si channel film. High-performance LTPS-TFTs of very low V_{TH}, excellent S.S., and very high μ_{FE} can be obtained, which are very promising for the realization of SOP and 3-D circuit integration.

II. Experimental Procedure

The fabrication of devices started by depositing a 50-nm undoped amorphous Si (α-Si) layer at 550 °C in a low-pressure chemical-vapor-deposition system on Si wafers capped with a 500-nm thermal oxide layer. A 5-nm Ni was deposited by an electron-beam evaporation system at room temperature and patterned by a lift-off process as a seed layer to crystallize the α-Si, as shown in Fig. 1(a). Lee *et al.* and Wong *et al.* have shown that a very thin thickness of Ni within 5 nm is enough for MILC process [17]–[21]. Then, the 50-nm α-Si layer was recrystallized by the MILC process at 550 °C for 24 h in a N_2 ambient, as shown in Fig. 1(b). After the residual Ni was removed by $H_2SO_4 + H_2O_2$, a 500-nm plasma-enhanced chemical-vapor-deposition oxide was deposited at 300 °C for device isolation. The device active region was formed by patterning and etching the isolation oxide. The source and drain (S/D) regions in the active device region were implanted with boron (10 keV at $5 \times 10^{15}\ cm^{-2}$) and activated at 600 °C for 24-h annealing in a N_2 ambient, as shown in Fig. 1(c). A 25-nm HfO_2 was deposited by an electron-beam evaporation system at room temperature. Then, 200-nm TaN gate electrode was deposited by sputter at room temperature and patterned by reactive ion etching. After the patterning of S/D contact holes, Al was deposited by thermal evaporation system

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M.-W. Ma, C.-J. Su, and T.-F. Lei are with the Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

T.-S. Chao, W.-C. Wu, and K.-H. Kao are with the Institute and Department of Electrophysics, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C (e-mail: tschao@mail.nctu.edu.tw).

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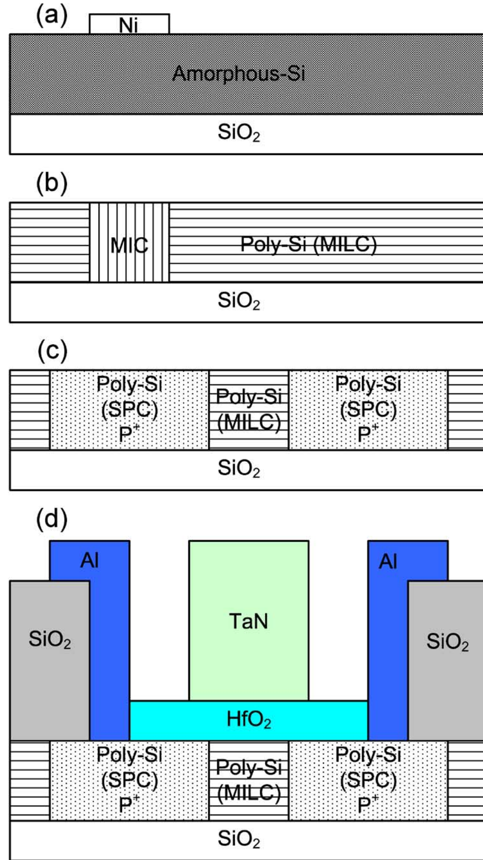

Fig. 1. Cross-sectional view and process flow of the TaN/HfO$_2$ gate stack structure LTPS-TFT with MILC channel film.

as the gate and S/D contact pad. Finally, the TFT devices were completed by the contact pad definition. The cross-sectional view of the TaN/HfO$_2$ gate stack structure LTPS-TFT with MILC channel film was shown in Fig. 1(d).

The device with gate length (L) and width (W) of 2 μm and 1 μm, respectively, was measured. The $V_{\rm TH}$ was defined as the V_G at which the drain–current reaches 100 nA $\times$ W/L and $V_{\rm DS} = 0.1$ V. The $\mu_{\rm FE}$ was extracted from the maximum transconductance (G_m).

III. Results and Discussion

Fig. 2 shows the transfer characteristics $(I_D–V_G$ and $G_m)$ of LTPS-TFT with TaN/HfO$_2$ gate stack structure and MILC poly-Si channel film. A very low $V_{\rm TH}(\sim 0.095$ V) and ultra-sharp subthreshold current curve is observed, which indicates an excellent S.S. (~83 mV/dec) that can be comparable with single crystalline silicon channel. A very high gate-capacitance density, which corresponds to a very low effective oxide thickness EOT ~5.12 nm, is obtained from the capacitance–voltage curve of TaN/HfO$_2$ on a P-type single crystalline silicon substrate to extract the gate-capacitance density of TaN/HfO$_2$ LTPS-TFT, as shown in the inset in Fig. 2. Therefore, the high $\mu_{\rm FE}$ $(\sim 240$ cm^2/V $\cdot$ s) can be calculated from the maximum G_m. The high-performance electrical characteristics of LTPS-TFT are attributed to both the low defect density of poly-Si channel film crystallized by MILC and high gate-capacitance density provided by high-κ gate dielectric HfO$_2$. Some impor-

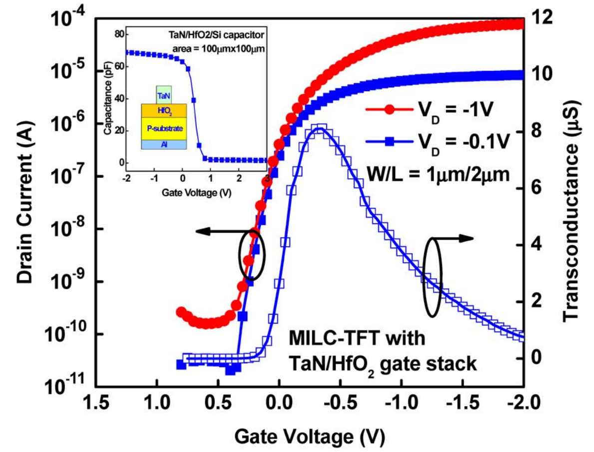

Fig. 2. Transfer characteristics $(I_D–V_G$ and transconductance $G_m)$ of LTPS-TFT with TaN/HfO$_2$ gate stack structure and MILC polycrystalline silicon channel film. The inserted figure is the $C–V$ curve of TaN/HfO$_2$ capacitor.

TABLE I
Important Parameters of the TaN/HfO$_2$ Gate Stack Structure LTPS-TFT With MILC Channel Film. Other Works Are Also Listed for Comparison

	MILC P-TFT with HfO$_2$	MILC P-TFT with SiO$_2$ [19]	SPC P-TFT with HfSiO$_x$ [12]	SPC P-TFT with SiO$_2$ [12]
W/L (μm/μm)	1/2	10/5	5/10	5/10
V_{TH} (V)	0.095	-4.2	-0.91	-6.85
S.S. (V/decade)	0.083	1.0	0.37	1.06
EOT (nm)	5.12	100	25.5	46.5
μ_{FE} (cm^2/V-s)	240	98	27.45	15.82
I_{on}/I_{min}	4.09x10^5	3.4x10^7	4.12x10^6	3.56x10^6

tant electrical parameters of LTPS-TFT are listed in Table I and compared with other works. Compared with the conventional SPC TFT with thick SiO$_2$ gate dielectric, we can observe that the conventional MILC-TFT with thick SiO$_2$ gate dielectric shows a significant improvement on $\mu_{\rm FE}$, as shown in Table I. It is due to the fact that the MILC channel film has low defect density in poly-Si [21]. However, the S.S. of conventional MILC-TFT is still too high to reduce the operation voltage of LTPS-TFT [17]–[21]. The replacement of thick SiO$_2$ gate dielectrics by high-κ gate dielectrics can provide a large gate-capacitance density to attract more carriers with a smaller gate voltage to fill up the traps and lower the potential barrier height in the poly-Si channel film [22]. This makes the LTPS-TFTs turn on within several voltages, resulting in the reduction of the S.S. and the operation voltage. As shown in Table I, the $V_{\rm TH}$ and S.S. can be obviously reduced without any hydrogen-related plasma treatments, as high-κ gate dielectrics are used. In addition, the mobility of TaN/HfO$_2$ MILC-TFT is much larger than the conventional MILC-TFT. It can be attributed to the

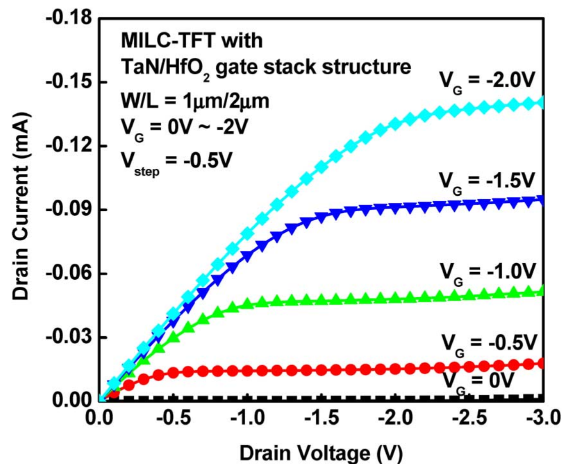

Fig. 3. Output characteristic I_D–V_D of MILC LTPS-TFT with TaN/HfO_2 gate stack structure.

small device's length and width that less grain boundaries exist in the channel film.

However, the drain leakage current of LTPS-TFT with TaN/HfO_2 gate stack structure and MILC poly-Si channel film is higher than conventional MILC and SPC LTPS-TFT, resulting in a degradation of the $I_{\rm on}/I_{\rm min}$ current ratio. The high drain leakage current is attributed to the poor grain boundaries of SPC/MILC interface in S/D junction region, because the longitudinal grain boundaries of MILC channel film would not be continuous in the S/D junction region, which is activated by SPC. The SPC poly-Si has a columnar grain structure with grain boundaries that are randomly oriented with respect to the longitudinal grain boundaries of MILC channel film, resulting in poor grain boundaries of the S/D and channel interface. The process flow of S/D ion implantation before the MILC process may improve this drawback. However, the S/D ion implantation will affect the MILC length. The modified process of metal-gate/high-κ MILC TFT is under study.

Fig. 3 shows the output characteristic I_D–V_D of MILC LTPS-TFT with TaN/HfO_2 gate stack structure and indicates a very high driving current within -2 V of gate and drain voltages. The high driving current would be very suitable for the application of SOP and 3-D circuit integration.

IV. Conclusion

The combination of high-κ gate dielectric and MILC poly-Si channel film has been proposed for the first time. The p-channel LTPS-TFT with TaN/HfO_2 gate stack structure and MILC polycrystalline channel film can achieve high $\mu_{\rm FE}$ ($\sim$240 $\text{cm}^2/\text{V} \cdot \text{s}$), low $V_{\rm TH}$($\sim$0.095 V), and excellent S.S. ($\sim$83 mV/dec) simultaneously. The combination of TaN/HfO_2 gate stack structure and MILC poly-Si channel would be very promising for the application of SOP.

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