Passivation Effect of Poly-Si Thin-Film Transistors With Fluorine-Ion-Implanted Spacers

Wei-Ren Chen, Ting-Chang Chang, Po-Tsun Liu, Chen Jung Wu, Chun-Hao Tu, S. M. Sze, and Chun-Yen Chang

***Abstract*—In this letter, polycrystalline silicon thin-film transistors (TFTs) consisting of lightly doped drain structure and fluorine-ion-implanted spacers were investigated for the passivation effect under the hot carrier stress. The dose and distribution of fluorine are exhibited by secondary ion mass spectrometry analysis. We could use this method to provide enough fluorine atoms to passivate the defects between the N^- regime and the conduction channel. Moreover, the TFTs with fluorine-ion-implanted spacers have better electrical characteristics than the standard device for resisting the degradation effects of hot carrier, such as smaller degradation of transconductance, current crowding effect, and subthreshold slope.**

***Index Terms*—Fluorine passivation, ion implantation, polycrystalline silicon (poly-Si), spacer, thin-film transistor (TFT).**

I. Introduction

POLYCRYSTALLINE silicon (poly-Si) thin-film transistors (TFTs) are very actively being investigated for pixel switching transistors of high-quality active-matrix liquid-crystal displays, organic light-emitting displays, and driving circuits of system-on-panel, due to their higher carrier mobility and lower threshold voltage than amorphous-silicon (a-Si) TFTs [1], [2]. However, the poly-Si TFTs need an important process, i.e., defect passivation treatment, to improve the devices performance, i.e., the grain boundaries in the substrate will seriously affect the electrical characteristics of devices, because they act as the tapping centers to trap carries and become energy barriers in the grain boundaries to reduce carrier mobility [3].

In recent years, this problem of defect passivation has been studied by many researchers, among whom are H. N. Chern *et al.* and J. W. Park *et al.*, who introduced fluorine (F)-ion-implanted substrate to eliminate the defects in the grain boundary and form a stronger Si–F bond than the Si–H bond to withstand electrical stress [4], [5]. The advantages of the ion implantation method are easy control of the dose and distribution of elements in the substrate, but the direct ion-implanted substrate may cause damages at the surface and bulk, leading to the need for an extrahigh temperature annealing process. Moreover, the defects, which exist between the conduction channel and the drain, are a main issue of device degradation in terms of hot carrier operation range. These degradation effects are related to the presence of high electric fields at the drain junction. Hence, we generally use drain engineering (e.g., lightly doped drain (LDD) and large-angle-tilt-implanted drain) to prevent the degradation phenomenon of poly-Si TFTs for hot carrier stress, but the effect is limited for poly-Si TFTs [6], [7].

In our work, we propose a passivation method of poly-Si TFT by using fluorine-ion-implanted spacers, and this method can accurately enable enough amount of fluorine atoms to passivate defects near the drain junction with the conduction channel. The method combines with the LDD process and fluorine passivation effect, resulting in better electrical performance after dc stress reliability.

II. Experiment

The poly-Si TFT with spacers (LDD) structure was built with a 50-nm-thick undoped a-Si layer deposited on a 500-nm-thick oxide-coated silicon wafer (buffer oxide) by low pressure chemical vapor deposition (LPCVD) at 550 °C. Then, the deposited a-Si layer was recrystallized by solid-phase crystallization at 600 °C for 24 h in a N_2 ambient. Next, the active region with a channel width of 10 μm was patterned by a G-line stepper and transferred by transformer couple plasma etching using the mixture of Cl_2 and HBr. After defining the active region, the 50-nm-thick tetra-ethyl-ortho-silicate (TEOS) gate oxide was deposited by LPCVD. Subsequently, a 200-nm-thick undoped poly-Si layer was deposited and transferred to a gate electrode (with a channel length of 10 μm). After poly-Si gate formation, self-aligned phosphorous implantation was performed with a dose of 5×10^{13} cm^{-2} to form the N^- regime at the source/drain region and then deposited 300-nm-thick TEOS oxide to obtain spacers by dry etching. Before the dry etching process, the 300-nm-thick TEOS oxide was implanted fluorine atoms (with a dose of 5×10^{15} cm^{-2} and energy of 27 KeV) at the middle position; this position can prevent implantation-induced interface damage between the channel and the gate oxide. After the spacer definition process, the N^+ regimes of the source and drain used self-aligned phosphorous implantation with a dose of 5×10^{15} cm^{-2}, and the activation

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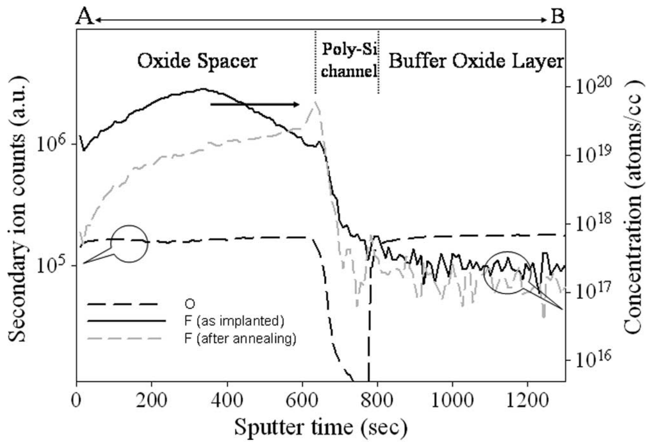
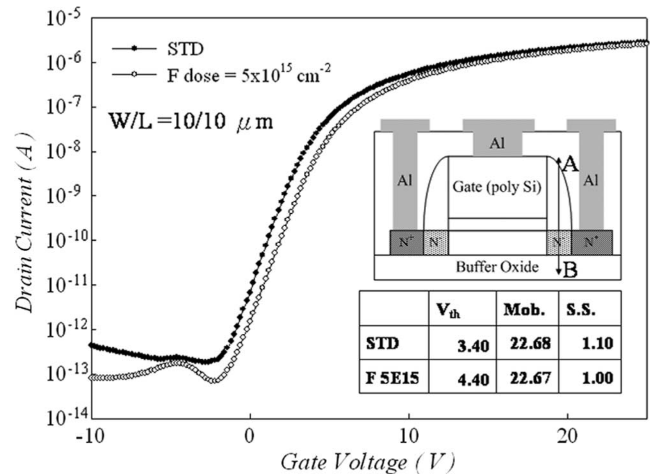


Fig. 1. SIMS depth profile (secondary ion counts with sputter time) of the fluorine-ion-implanted oxide spacers/poly-Si channel/buffer oxide layer. The bold dashed line, solid line, and gray dashed line represent the oxygen signal, fluorine signal (before annealing), and fluorine signal (after annealing), respectively.



	V_{th}	Mob.	S.S.
STD	3.40	22.68	1.10
F 5E15	4.40	22.67	1.00

Fig. 2. Comparison of typical I_D–V_G characteristics of the TFTs with standard device and the fluorine-ion-implanted spacers at $V_D = 0.1$ V. The parameters of the threshold voltage, mobility, and subthreshold swing are extracted in the inset tables.

of the source/drain region was realized by the thermal budget of the passivation TEOS oxide layer at 700 °C for 3 h. The $50 \times 50\ \mu\text{m}^2$ contact holes were patterned by dry etching, and Al metallization was performed. Finally, the devices were sintered at 350 °C in nitrogen ambient for 30 min. Furthermore, the standard device (STD) with no fluorine ion implantation was also fabricated for comparison.

III. Result and Discussion

Fig. 1 shows the secondary ion mass spectrometry (SIMS) depth profile of fluorine-implanted oxide spacers/poly-Si channel/buffer oxide layer, and the inset of Fig. 2 also shows the diagram of the measurement regime (from A to B). It is clearly observed that the peak value of as-implanted fluorine concentration exactly exists at the middle part of the spacers, and the fluorine atoms can diffuse to the interface and bulk of poly-Si channel during the activation of the source/drain process. Due to the material property of fluorine [8], the fluorine atoms can easily bond with the dangling bonds of grain boundaries to form the stronger Si–F bonds to achieve the passivation effect. Hence, we can use the fluorine-ion-implanted oxide spacers to simply mend the defects of the N^- regime in order to reduce the impact ionization effect in terms of hot carrier operation.

Fig. 2 presents the typical drain current–gate voltage I_D–V_G curves of the standard TFTs and the proposed TFTs with fluorine-ion-implanted oxide spacers at the linear regime (drain voltage = 0.1 V). The electrical parameters are also extracted in the inset tables. It can be found that the mobility (Mob.) and subthreshold swing (S.S.) are similar to those of standard TFTs, yet the threshold voltage V_{th} of TFTs with fluorine-ion-implanted oxide spacers is larger than that of the standard TFTs, which is about 1 V. Because the partial fluorine atoms of the spacers can also diffuse into the edge of the gate oxide during the activation of the source/drain process, this result brings about the reduction of gate control ability at the channel edge. This drawback could be improved via the suitable implanted dose and distribution. Here, we can also obtain a lower leakage current than STD due to the fluorine passivation effect in the N^- regime for using the fluorine-ion-implanted oxide spacers.

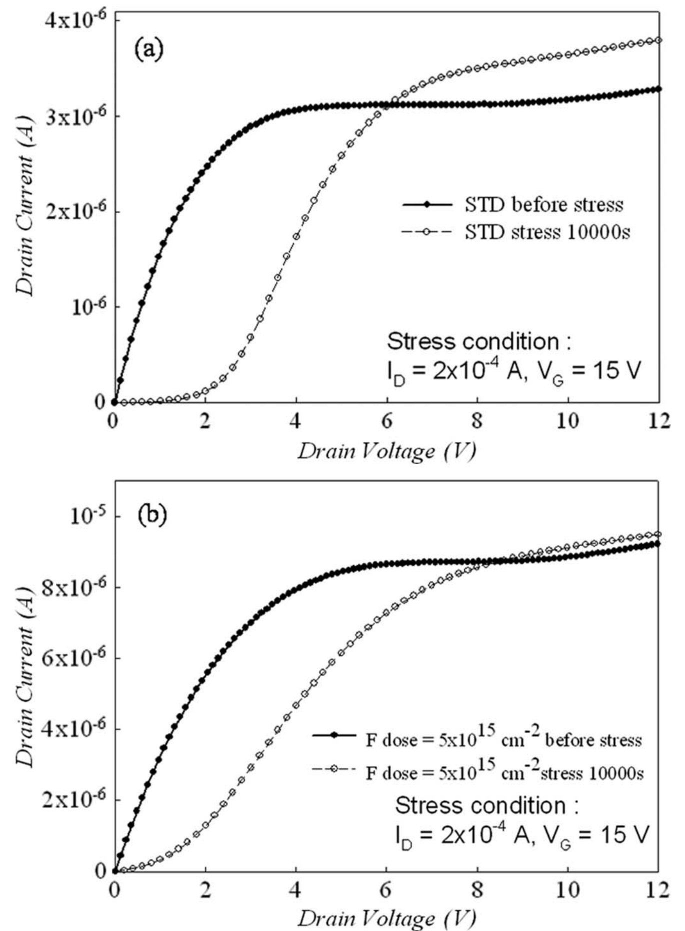


Fig. 3. Comparison of the I_D–V_D characteristics of the TFTs under hot carrier stress (10 000 s) with (a) standard device and (b) fluorine-ion-implanted spacers. The gate voltages (before stress/after stress) were set at $V_G(13.4\text{ V}) - V_{\text{th}}(3.4\text{ V}) = 10$ V and $V_G(14.4\text{ V}) - V_{\text{th}}(4.4\text{ V}) = 10$ V for the STD sample and fluorine-implanted spacer sample, respectively.

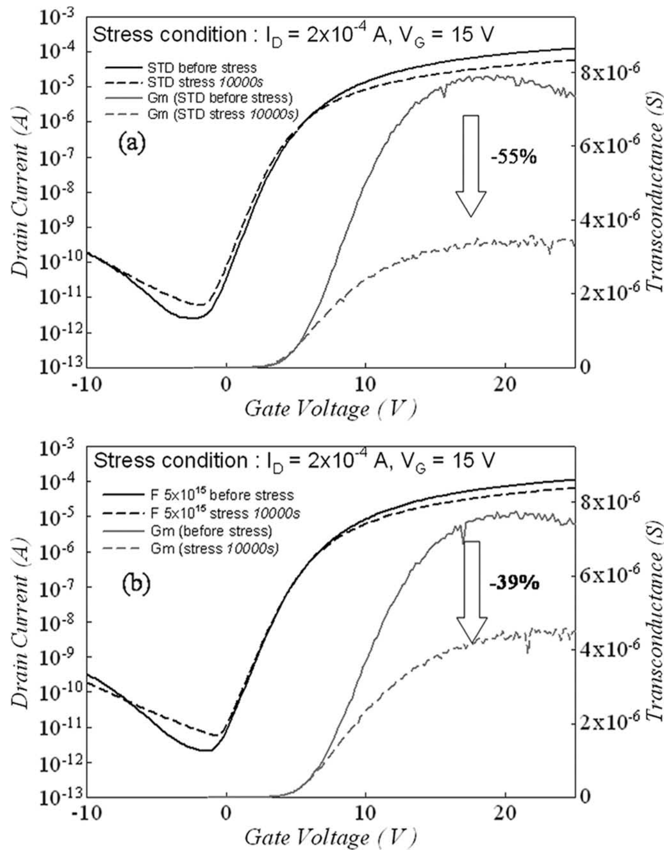


Fig. 4. Comparison of the I_D–V_G characteristics of the TFTs at $V_D = 5$ V under hot carrier stress (10 000 s) with (a) standard device and (b) fluorine-ion-implanted spacers.

The electrical reliabilities of TFTs with STD and fluorine-ion-implanted oxide spacers are shown in Figs. 3 and 4, respectively. The dc stress condition was set at $V_G = 15$ V and $I_D = 2 \times 10^{-4}$ ($V_D > 30$ V), and the stress time was 10 000 s. This stress condition is hot carrier operation in order to study the passivation effect of the Si–F bonds at the interface and bulk of conduction channel edge near the drain. Fig. 3(a) exhibits the V_D–I_D curve of STD TFTs, and it is found that a serious current crowding effect is obtained after stress (10 000 s), compared with the no-stress sample. However, I_D will be larger than the no-stress state if V_D exceeds 6 V. These results could be considered in that the hot carrier induced the defect generation at the channel edge and the N^- regime, leading to the degradation of electrical characteristics, and the excess $I_D(V_D > 6\text{ V})$ was affected by the depletion region, depending on V_D due to the thermionic field emission effect of depletion and floating-body effect; the floating-body effect gives rise to the kink regime in saturation. This mechanism can be attributed to holes generated by impact ionization near the drain [9], [10].

Hence, the TFTs with fluorine-ion-implanted oxide spacers can remarkably eliminate the hot carrier-induced degradation at the drain edge, as shown in Fig. 3(b), especially for the current crowding effect. Here, we considered that the fluorine-implanted spacer sample with stronger Si–F bonds existing in the grain boundary should resist the impact of hot carries during the stress. To further analyze the electrical properties of I_D–V_G curves for STD (at $V_D = 5$ V), it can be found that the transconductance (Gm) and subthreshold swing (S.S.) are strikingly degraded by hot carrier stress after 10 000 s and that the loss ratio of Gm is about 55%, as shown in Fig. 4(a). However, from Fig. 4(b), the TFTs with fluorine-ion-implanted oxide spacers can substantially restrain the aforementioned degradation because of the passivated effects of stronger Si–F bonds. Therefore, the TFTs with fluorine-ion-implanted oxide spacers can effectively reduce the hot carrier stress in our research.

IV. Conclusion

A poly-Si TFT with fluorine-ion-implanted oxide spacers was successfully demonstrated to passivate defects in this work. The dose and distribution of fluorine atoms could precisely be controlled in the spacers by using the ion implantation. The experimental results had shown that the proposed poly-Si TFT had superior electrical characteristics under hot carrier operation due to the fluorine-passivated defects between the conduction channel and the drain.

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