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Measuring the relative performance for leading fabless firms by using data envelopment analysis

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Abstract IC Design (fabless) is critical for the global semi-conductor industry. The total revenue of all global fabless firms in 2003 was about US$20 billion, with the top 30 firms earning accounting for 96% of the market share. To examine the leaders in the field, this research analyzes the relative performances of those top 30 fabless firms. Fabless firms are often evaluated based on subjective judgments, and an overall scheme to measure the performance involving objective, multi-input and multi-output criteria is yet to be established. There is also a need for identifying and determining suggestions of how specific firms could improve their performance. Data Envelopment Analysis (DEA) method has been employed in this paper to satisfy the above needs. Using the input and output data of 2003, this study used the DEA method to build a model to evaluate the performance of those global top 30 fabless firms. The current research used four efficiency models: CCR, A&P, BCC, and Cross-Efficiency. To offer a comparison of efficiencies and associated discussions, an analysis of the Scale-Return is provided. Finally, the performance of various fabless firms in 2003 is analyzed. According to the CCR and A&P models, the results showed that the top ten Decision Management Units (DMUs) achieved better operation performance among the 30 leading global fabless firms.

Keywords Performance · IC design (fabless) · Data envelopment analysis (DEA)

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Introduction

The total output value of global fabless firms was about US$20 billion in 2003. Of this figure, the top 30 firms had a market share of US$19.2 billion, or 96% of all sales (Semiconductor Yearbook of 2003). The electronic component market will continue to boom in the future since the components for cell-phones, CDs, CMOS, LCD Displays, DRAM, digital cameras, DDS and a host of other products will continue to increase in demand. These new products show that a new phase of the consumer electronics era is coming and that the new battlefield of top global enterprises will be full of challenges. Not only IT but also fabless firms, both of which are the upstream portion of the semiconductor industry, can expect to harvest such growth opportunities from this exciting trend.

There are several key elements explaining why the major players can hope to continuously lead in the fabless field. First, they still prevail with technological innovation and superior patent protection. Second, they build solid supply chains and high entry barriers to keep out competition. Third, they provide total solutions for customers; they provide excellent technical specifications, have flexible marketing as well as pricing strategies, and maintain stable chip OEM partner relationships. In other words, even though there are many factors contributing to success, excellent management performance is always the main key for outstanding fabless firms. Fabless firms, however, struggle with managing extreme boom and bust cycles. Whenever the company finds the right direction for business and has favorable R&D, then the business becomes more prosperous. These factors, working together, can make the company's products and achievements greater and greater. On the other hand, once the company's operation goes poorly and achievement is bad, a negative cycle is set off. The firm's competitiveness is downgraded in the market and investment begins to dry up. The company will have a harder time struggling with the dilemma of losing manpower and wealth (Semiconductor Yearbook of 2003). Such are the characteristics in today's fabless industry.

In the coming years, the global fabless industry will be the scene of frequent integration and the fabless, which has a single and competitive product line, will be the main target for big factories. The top 30 global fabless firms are mainly in the USA and Taiwan (Chang and Tsai 2002; Hung and Yang 2003). It is crucial for every company to find an objective effective evaluation standard based on scientific principles. To date, an overall scheme for measuring the performance of fabless firms involving multi-input and multi-output criteria has not been established (Shuai et al. 2004). There also lacks suggestions of how specific firms could improve their performance. Remarkably, this study found that the DEA method meets the above needs. This research employs the DEA method to evaluate the relative performance of the top 30 fabless firms, using input and output data of 2003 (Semiconductor Yearbook of 2003).

The DEA relies extensively on both efficiency analysis and operation performance. Chen et al. (2003) discussed the multiplier bounds in DEA. Kleine (2004) mentioned a general model framework of DEA. Lewis and Sexton (2004) used DEA to analyze efficiency of organizations with complex internal structure. Liu et al. (2003a,b), used DEA to assess the efficiency of Taiwan's colleges. Opricovic and Tzeng (2003) compared DEA and MCDM method. Tzeng et al. (2001) used DEA to evaluate the production efficiency for Taipei city bus company. Yu et al. (2004) analyzed fuzzy multiple MOPA to DEA with imprecise data. The DEA is a unified macro-index that deals with many different inputs and outputs at the same time without the prior knowledge of the function of inputs and outputs by using the Non-Parametric Approach (Charnes et al. 1985; Chen and Iqbal Ali 2002). DEA can avoid errors caused by the assumption of productive function in the unclear relationships among input and output. It is not necessary to have the same measurement unit; this flexibility makes it easier to deal with the data (Farrell 1957; Charnes et al. 1978; Semiconductor Yearbook of 2003; Andersen and Petersen 1993; Doyle 1992). Therefore, this research adopted DEA as the analysis tool and it includes CCR, A&P, BBC, and Cross-Efficiency.

The goal of this research is to use the DEA to analyze the top 30 global fabless achievements from the relative operation performance. On the basis of the 2003 data, the index regarding input includes Capital stock, Net Working Capital, and Long-Term Investments. In terms of output, Revenue and Earnings before Taxes (EBT) are included. The authors have tried to solve the problems by using the DEA model in this research and have presented the objective results that they hope will help fabless firms conduct better internal evaluations.

In sect. "The current status of the global fabless industry" of the text, authors introduce the present status of the global fabless industry. Section "Research methods" contains the description of DEA and other evaluation methods for the operation performance. Section "An illustrative example" includes analysis and discussion. Section "Conclusions and recommendations", the conclusion, includes recommendations for fabless firms to incorporate these findings and help them reach their strategic goals. The limitations of this research are also discussed.

The current status of the global fabless industry

From the revenue of the top 30 fabless corporations, it is easy to notice that there are some key players dominating the whole market. As mentioned above, in 2003, 96% of the global fabless revenue was generated by just 30 firms, primarily in the US, Taiwan, and Canada. Obviously, the fabless industry is not only becoming more concentrated daily, but the competition is getting more intensive. The list of the top 30 global fabless firms is shown in Table 1. The product positioning of various fable firms is discussed next.

Product positioning of the top 30 fabless firms

Qualcomm occupied 95% of the CDMA chipsets of the 3G wireless communication networks. ATI and NVIDIA occupied 90% of the drawing processors. Xilinx and Altera occupied 80–90% of the logic editor components. MediaTek occupied 50% of the single chips of VCD and DVD players. ATI and NVIDIA have made enormous profits over the past three years by successfully riding the trend of applied multimedia drawers. MediaTek, Sunplus, Ali, ESS, Zoran, and Cirrus Logic have fought fiercely in the storage chip market. In spite of their already-strong names in the fabless industry, they have placed great resources into the DVD±RW, DVD-Recorder, MPEG-4 and other new chip product lines. Sunplus has been very successful with its DSC control chips. Novatek has carved its own place in the Display Driver IC field thanks to its increasing supply of TFT LCD panels and low price. Also, the flash storage chip is one of the necessary devices for cell-phones, so SanDisk and SST have also entered into the relevant field of flash IC manufacturing. From the above description, one can easily determine the major contours of the global fabless industry as shown in Table 2.

Brief summary

The global fabless industry will probably undergo much integration in the coming years. Fabless firms with proven success will become the main targets for the big factories to take over. Take the leading WLAN chip manufacturer, Intersil,

Table 1 The top 30 fabless firms' rank/distribution/revenue (unit: US$ million)

Rank	Fabless firm	Distribution	2003 revenue	2002 revenue	Growth rate (%)
1	Qualcomm	US	2,466	1,942	27.0
2	Nvidia	US	1,823	1,766	3.2
3	Broadcom	US	1,611	1,090	47.8
4	ATI	Canada	1,511	525	187.8
5	Xilinx	US	1,300	1,125	15.6
6	MediaTek	Taiwan	1,116	865	29.0
7	SanDisk	US	1,080	485	122.7
8	Altera	US	827	712	16.2
9	Marvell	US	820	480	70.8
10	Conexant	US	633	621	1.9
11	VIA	Taiwan	598	736	−18.9
12	Qlogic	US	516	415	24.3
13	Adaptec	US	437	411	6.5
14	Globespan Virata	US	379	231	64.1
15	Aeroflex	US	341	203	68.3
16	Sunplus	Taiwan	325	253	28.5
17	Silicon Lab.	Taiwan	325	182	78.7
18	Novatek	Taiwan	320	196	63.0
19	SST	US	295	275	7.4
20	Realtek	Taiwan	272	269	1.3
21	MegaChips	Japan	271	345	−21.3
22	ICS	US	257	228	12.6
23	PMC-Sierra	Canada	249	218	14.4
24	OVTI	US	249	82	203.5
25	Zoran	US	217	149	45.2
26	Genesis Micro.	Canada	213	196	9.1
27	Cirruss Logic	US	198	293	−32.3
28	ESS	US	195	273	−28.6
29	Semtech	US	192	205	−6.4
30	Ali	Taiwan	191	178	7.1

Source: IC insights, 2003/12

Table 2 The product positioning of the top 30 global fabless firms

Product	Company
Communication ICs	Qualcomm, Broadcom, Marvell, Conexant, Q-Logic, Silicon Lab, Realtek, PMC-Sierra, ICS, SMSC, Zarlink, DSP Group
FPGA	Xilinx, Altera, Lattice
Graphic ICs	Nvidia, ATI
Multi-media ICs	MediaTek, Sunplus, ESS, Zoran, Cirrus Logic, Realtek
Flash	SanDisk, SST
LCD ICs	Novatek, Genesis microchip, Zoran
PC chipsets	VIA, Ali
Ower management	Semtech

Source: Topology research, 2004/03

for example, even though Intersil's market share was more than 50%, it was first bought out by Globalspan Virata, and then Globalspan Virata was purchased by Conexant in late 2003. Such chain-reaction mergers will probably be increasingly common in the near future. There are now at least 40 companies in the world that are working on the development of WLAN chips, but indications show that there will be only seven firms remaining after takeovers and mergers in two years: Intel, Broadcom, Marvell, TI, and three other already big names.

Looking forward, the main factor of success for fabless firms is their quality of operation performance. Under current consumer trends, big firms will combine with small companies that have their own niche, thus achieving the twin goals of system integration and meeting market demand. Major fabless work can be done at the chip factory to take advantage of the big firms' experiences and to develop the manufacturing, but the small companies cannot join this development. In addition, IC products will gradually head for unification, where scale and integration will become the main flashpoints of competition in the field. Finally, the whole semiconductor industry will probably be centralized to IDM and the large-scale fabless firms. Therefore, operation performance will determine the development and survival of small firms in the future.

Research methods

This section discusses this study's methods of research and development and point out the differences between six traditional research methods. The authors also introduce the investigative elements and the applied methods in this study.

Brown et al. (1998) pointed out that the key to effective evaluation is taking the R&D unit as one part of the entire organization and then emphasizing the inputs, processes, outputs, and benefits. Poh et al. (2001) addressed six research methods: the Scoring Method, Analytic Hierarchy Process (AHP), Comparative Method, Cost-Benefit Analysis, Economic Analysis, and Decision Tree Analysis. There are many ways to evaluate the problems of operation performance (Cavalluzzo and Ittner 2004; Folan and Browne 2005; Hoque 2004; Ittner et al. 2003; Schmitz and Platts 2004). It is necessary to use the multiple indices because a single index has its blind spots; for example, the financial approach cannot solve the input and output aspects. The DEA, in contrast, takes multiple criteria, multiple indexes, and the idea of relative importance as its core principle. DEA can overcome the traditional evaluation shortcomings by using weights, normalization, and comparison (Liu et al. 2004; Ohta and Yamaguchi 1995; Zimmermann 1978; Charnes et al. 1985). Therefore, this research used the DEA method, a multi-input and multi-output approach. DEA is one kind of cost-benefit analysis that is used for evaluating the operation performance of the top 30 global fabless firms. There are five main merits associated with DEA. First is to take the business cost-benefit ratio method and use the DEA to identify the operation performance of every company. Second, scholars have improved the DEA. There are four kinds of evaluation models commonly used, and DEA makes it convenient to identify the operation performance and the comparative analysis of every company. Third, from the analysis of internal and external periodical databases, the DEA is not only suitable for evaluating the achievement of nonprofit organizations but also for commercial enterprises. Fourth, fabless revenue in the semiconductor industry plays a crucial role, so fabless firms have an enormous influence on the global economy. Thus, there is an enormous need to find an evaluation model for the top 30 fabless firms so one can discover firms' competitive advantages and thereby further develop the semiconductor industry. Fifth, analysis of the input and output data of the top 30 firms are based on fabless annual reports as found in the ITRI (Industrial Technology Research Institute) 2003 Semiconductor Yearbook and Dataquest. The following section is mainly about the characteristics of the DEA, basic assumptions, and the application of different models.

Method of DEA

The DEA used in this research is a kind of mathematics programming model. It first applies the observed information into the model and then finds a DEA efficient frontier to calculate relative efficient values of each DMU among its group. Farrell (1957) first addressed the concept of the Deterministic Non-Parametric Frontier. The determinacy means that the engineering level of all DMUs is the same and faces the common production frontier. The non-parametric frontier is a pattern of non-preset production function; the multi-input efficiency evaluation established the foundation of DEA theory Farrell (1957). This pattern has some basic assumptions. First, the production frontier is formed by the most efficient DMU, and the ineffective DMUs are below the frontier. Second, Fixed Scale Returns are assumed. Third, the production frontier protrudes to the origin, so the slope of every dot is smaller than or equal to zero.

In DEA theory, when the combination of input and output of a certain DMU has fallen at the border of DEA, authors assume it is an efficient DMU. On the contrary, if the DMU has fallen out of the border, then this DMU is relatively inefficient. Many scholars have proposed and proven the analysis of the DEA model (Farrell 1957; Charnes et al. 1978; Semiconductor Yearbook of 2003). Basically, DEA is a non-parametric analytical method with the following main characteristics. First, this approach is one estimating non-parametric maximum production. It is not necessary to set the relationship between previous inputs and outputs in the target function and therefore avoid the risk of wrong function assumptions. Second, the DEA model can calculate the relative efficiency values of the specific individual and the relative group. Third, the DEA model sets up a comprehensive index by mathematical programming. It can measure the relative efficiency among the different inputs and outputs. The DEA model can solve the problem of the different units of measurement caused by the evaluation of multiple inputs and outputs. Fourth, DEA is more objective and fair than the general questionnaires and the decisions of policymakers (such as in AHP). And fifth, DEA method can provide efficiency scores for multi-inputs and multi-outputs in one single step. This is similar to the relative analysis method with single input and single output.

The CCR model of DEA

The CCR model used in this research, a tool for measuring an organization's efficiency, was created by Charnes et al. (1978). It supposes there are s kinds of output items, and n pieces of DMU using m kinds of input items; the k piece of DMU's efficiency value can then be calculated by using Fractional Linear Programming (Charnes and Cooper 1984).

A sample equation of CCR DEA linear programming formulation is as follows:

$$\text{Max } Z_k = \sum_{j=}^{s} u_j Y_{jk}$$

Subject to:

$$\sum_{j=1}^{s} u_j . Y_{jk} - \sum_{i=}^{m} v_i . X_{ik} \leq 0, \quad k = 1, \ldots, n,$$

$$\sum_{i=}^{m} v_i X_{ik} = 1,$$

$$u_j \geq \varepsilon > 0, \quad r = 1, \ldots, s,$$

$$v_i \geq \varepsilon > 0, \quad i = 1, \ldots, m,$$

$$\mathrm{u_j} = t \cdot U_j;$$

$$v_i = t \cdot V_i;$$

$$t^{-1} = \sum V_i \cdot X_{ik}$$

BCC model of DEA

Banker et al. (1984) addressed the BCC model, the input and output cost-benefit analysis. According to the BCC definition, the Scale Efficiency (SE) is the quantity of input under the fixed output standard, while the ratio of the quantity of input is under the best production scale. The Technical Efficiency (TE) is the quantity of input under the fixed output standard and the ratio of the quantity of input under the fixed output standard. The assumption of the CCR model is that the Scale Returns are fixed to estimate the whole efficiency. If an inefficient situation occurs, it might be partly influenced by the scale factor but not by the inefficient technique. Thus, Banker et al. revised the CCR model to create the BCC model and examined the Technical Efficiency under dynamic scale condition.

A&P model of DEA

While working on the efficiency analysis, it may happen that the DMU efficiency value is 1 by the calculation of CCR. That is a lone outlier without sufficient discriminating power. For the efficient DMU, Andersen and Petersen (1993) proposed an advanced model which would not influence the inefficient DMU, but the efficiency value of efficient DMU will be greater than 1 after recalculation. One can then rank the efficient DMUs in order. The way to calculate efficiency is to eliminate the efficient DMUs from the reference set of the CCR model, remove the B dot that originally lies on the frontier line by using the A&P model, and finally the production frontier turns into $\overline{AB'C}$, so the efficiency of dot B will be greater than 1 (Table 3).

Cross-efficiency model of DEA

Doyle and Green (1994) explained the concept of Cross-Efficiency. Compared to self-appraisal, it is a kind of peer-appraisal model. In the CCR model, if the efficient DMU from self-appraisal has few references, it shows the high possibility of departing from groups and the Cross-Efficiency value will thus have a greater decrease in peer-appraisal. In the Cross-Efficiency matrix table, the Cross-Efficiency value (e_k) of the k piece of DMU is the average of DMU$_k$'s efficiency by using the virtual multiple calculation of the other DMU.

Analyses and discussion of various DEA models

This research adopts the CCR, BCC, A&P, and Cross-Efficiency models of DEA to evaluate the operation performance of the top 30 global fabless firms with the same input and output values. The authors have simply used the different theoretical foundations and different relative efficiency standards to evaluate the companies and provide suggestions for improving their operation performance (Table 4).

Scholars have improved the original CCR model so that the Cross-Efficiency model is now more objective. The authors took the result of the CCR and BBC models for the analysis while evaluating the scale efficiency values even though four models of DEA are calculated. As for the performance evaluation of the top 30 fabless firms, authors used the Cross-Efficiency model for analysis and comparison.

An illustrative example

This section is based on the characteristics, restrictions, procedures, measurements and models of DEA in sect. "Research methods". The first step of the DEA model is to establish the index for analysis. In this context as shown in sect. "The current status of the global fabless industry",

Table 3 The cross-efficiency matrix table

DMU of peer-appraisal/DMU	1	2	...	n
1	$\boldsymbol{E}_{11}$	E_{12}		E_{1n}
2	E_{21}	$\boldsymbol{E}_{22}$		E_{2n}
⋮				
n	E_{n1}	E_{n2}		$\boldsymbol{E}_{nn}$
The cross-efficiency value of peer-appraisal	$\boldsymbol{E}_1$	$\boldsymbol{e}_2$	...	$\boldsymbol{e}_n$

Source: Doyle and Green (1994)

Table 4 The comparison sheet of various DEA methods

Event/DEA model	CCR model	BBC model	A&P model	Cross-efficiency model
Time	1978	1984	1993	1994
Relative efficiency standard	Specific DMU	Specific DMU	Adjacent DMU	Peer DMU
Weigh measurement	Single favorable	Single favorable	Average of two	Average of peer
Relative efficiency character	Subjective	Subjective	Subjective	Objective
Method type	Original type	Improving type	Improving type	Improving type

Source: Xu, Ji Sheng, etc., 2002, using the data envelopment analysis to evaluate the research performance of ITRI
Remark: CCR model (total efficiency value) and BBC model (technological efficiency value) can achieve the scale efficiency value

authors collected data on the revenue, ranking, location, and product positioning of global top 30 fabless firms. It is very important to know what field of improvements that fabless firms should concentrate on. Spotting these trends will influence the future competitiveness of the fabless industry.

Firstly, authors chose the top 30 fabless firms from “2003 IC Insights” statistics as DMU. Secondly, referring to the relevant documents, “2003 ITRI Semiconductor Yearbook” and each company’s annual report, authors found proper input and output items as parameters and conducted relationship analysis. Thirdly, authors selected appropriate DEA models and adopted four models for analyzing and comparing the real examples. Fourthly, authors compared the efficiency analysis between CCR and BCC models. The primary inefficient sources of DMU came from a lack of Pure Technological Efficiency (BCC efficiency) or Scale Efficiency, and recommendations for improvement have been made. Finally, authors included the rewards scale analysis to discuss the Scale Efficiencies of the top 30 fabless firms.

Selection of DMU

Golany and Roll (1989) thought that DMU must be homogeneous, which means the evaluating targets need to have the similar operation characteristics. These are outlined as follows:

The same internal essence: All of the evaluated firms are IC designs, and then transfer the products to the packaging factory for packaging and testing the products. Since the problems facing each company are similar, maximizing the operation value is their common goal.

The same external environment: Even though the semiconductor companies are distributed across the world, their industrial environments are roughly the same. The operation inputs and output items of every company are the same, for instance: the biggest expenses are the costs of R&D and the fixed assets such as equipment, etc.

According to the aforesaid section, the DMU of this research, the name of the companies, the world distribution, the profits, and the growth rates are stated as Tables 1 and 2. As shown in our results, the companies are listed in descending order according to revenue: Qualcomm, Nvidia, Broadcom, ATI, Xilinx, MediaTek, SanDisk, Altera, Marvell, Conexant, VIA, Qlogic, Adaptec, Globespan Virata, Aeroflex, Sunplus, Silicon Lab. Novatek, SST, Realtek, MegaChips, ICS, PMC-Sierra, OmniVision, Zoran, Genesis Micro, Cirruss Logic, ESS, Semtech, and Ali.

Selection of input and output items

When using DEA to actually weigh criteria by priority, one cannot consider too many input and output items. Otherwise the efficiency value of every DMU will be 1 because of the idea based on Pareto Optimality criterion, and this goes against the original idea of weight efficiency (Lee and Li 1993). It is thus necessary to merge similar items or adopt factor analysis. As for the restriction of precise item quantity, authors considered the geometry room dimension of DEA is counted with a sum of input and output of DMU. When the input and output both increase, the number of DMUs must be increased correspondingly, and then one can use the envelopment line principle to search for the most efficient DMUs. Authors referred to the Rule of Thumb for the item selection that the DMU should be at least twice the sum of input and output Banker et al. (1984).

The selected input and output items from 30 companies are:

- Input items: From Table 1, there were eight input items: R&D Expenses, Fixed Assets, Intangible Assets, Capital Stock, Cash, Net Working Capital, Long-Term Investments, and Debt Ratios.
- Output items: From Table 1, there were seven output items: Revenue, Earnings before Taxes (EBT), Net Income after Taxes, Earning per Share (EPS), Return on Common Equity (ROE), Return on Assets (ROA), and Turnover Ratios.

Financial experts’ selection process for inputs and outputs

The 15 aforesaid inputs and outputs were subjected to another advanced selection process to see if they fit with the following principles. (1) data origins are credible; (2) it can be controlled; (3) it conforms to the current period relationships of input and output; (4) they have the same evaluation basis;

(5) they have the definite relationship with the operation performance.

As a basis of annual reports and public financial information, this research collected fifteen preliminary data (Appendix Table A.1) to evaluate the index via the five selecting principles. The data was then ranked in order and summed up five inputs and five outputs as shown in Appendix Table A.2.

Correlation analysis and the double regression of input and output

The authors examined the input and output relationships by the Pearson correlation coefficient. The analysis results and variables are shown in Appendix Table A.3. One must then observe whether the relationships conform to isotonicity or not. In other words, if the input quantity is increased, then the output quantity cannot be reduced. The item must be rejected if there is a negative correlation. The input and output data of this research are all Ratio Scales, so one can adopt the Pearson Production-Moment Correlation for examination.

From Appendix Table A.3, one can find the correlation coefficients of items. The following ones are apparent and positive: Capital Stock, Net Working Capital, and Long-Term Investments among inputs; Revenue and Earnings before Taxes (EBT) among outputs. These four above-mentioned values all meet the requirements of isotonicity and significance. The input and output material comes from the companies' annual reports, experts' appraisals, and correlation analysis. Therefore, authors adopted their inputs (Capital Stock, Net Working Capital, and Long-Term Investments) and two outputs (Revenue and Earnings before Taxes) as the indices of evaluation as shown in Table 5.

Election and application of DEA model

After inspecting the isotonicity of the selecting inputs and outputs, authors chose the CCR, A&P, BCC, and Cross-Efficiency models of DEA for the efficiency value. Authors also examined the Integrated Technical Efficiency, Pure Technological Efficiency, and Scale Efficiency of each DMU using BCC and CCR models. Since the calculating course is miscellaneous, one may utilize different PC software to calculate the efficiency value with LINGO, the coefficient correlation

Table 5 Global top 30 fabless inputs-outputs data sheet in 2003 (Thousand US$)

Fabless/Item	Input			Output	
	Capital stock	Net working capital	Long-term investments	Revenue	EBT
Qualcomm	789,586	2,624,559	1,120,927	2,466,331	1,285,147
Nvidia	153,513	328,979	190,029	1,822,945	86,673
Broadcom	292,009	444,931	41,097	1,610,095	(934,738)
ATI	237,227	92,600	711,100	1,510,992	(280,200)
Xilinx	337,069	458,805	1,091,697	1,299,900	350,544
MediaTek	192,856	673,456	347,266	1,115,931	500,669
SanDisk	144,781	812,977	185,062	1,079,801	241,881
Altera	381,387	111,771	14,451	827,207	212,501
Marvell	127,456	287,499	0	819,762	63,352
Conexant	303,488	133,734	119,230	633,100	23,433
VIA	379,295	175,804	368,543	597,664	(50,016)
Qlogic	103,473	206,342	0	516,200	215,601
Adaptec	106,772	170,487	6,346	437,200	(189,160)
Globespan	268,586	133,734	119,230	379,100	23,433
Aeroflex	60,193	161,556	0	341,028	12,883
Sunplus	192,856	116,249	127,658	325,349	60,817
Silicon	48,850	81,138	0	325,305	66,196
Novatek	102,535	80,454	18,933	319,706	64,414
SST	94,723	175,866	83,046	295,041	(38,751)
Realtek	197,597	170,718	117,630	272,005	84,613
MegaChips	246,610	115,178	1,248	271,297	2,795
ICS	67,898	163,687	32,000	256,900	71,541
PMC-Sierra	173,568	198,327	52,905	249,483	(15,843)
OVTI	22,678	254,761	7,110	249,400	89,008
Zoran	33,231	67,954	0	216,528	(66,615)
Genesis	31,248	48,670	0	213,400	(5,268)
Cirruss	83,445	143,199	6,996	198,200	39,444
ESS	39,517	79,313	9,076	195,273	40,894
Semtech	73,013	124,048	86,119	192,079	42,718
Ali	51,594	(21,439)	41,730	191,082	152

with SPSS, and use EXCEL to find the fuzzy DEA model and the fuzzy multi-programming calculation.

CCR, A&P, and cross-efficiency value analysis

In the CCR model, if the value equals 1, this means the result is relatively efficient; in contrast, values smaller than 1 are relatively inefficient. The A&P model eliminates the efficient DMU itself from the reference set of CCR model to make the efficiency values equal to 1 become greater than 1, in order to further differentiate among the efficient DMUs. Both A&P and CCR models are self-appraisal. The reason they have high efficiency is because they offer higher virtual multiple value in accordance with the favorable inputs and outputs, so the evaluations are rather subjective. On the other hand, Cross-Efficiency is a peer-appraisal method. In sum, each model has its own function and influence on the analysis and explanation. The Cross-Efficiency model has been proved by this research and is comparatively objective.

Assisting the efficiency value of analysis by reference set frequencies: In order to enhance the discriminating power of the CCR model, and to avoid non-discrimination situation, λ_j derived from duel model is often used for assistance. When λ_j is > 0, all the related DMU_j will be the reference set for the assessing units. Thus the higher number of times a DMU efficiency appears in the reference set of other DMU, the higher is its robustness of efficiency. If a DMU efficiency has not shown up in the reference set of other DMU, it will be an outlier (Andersen and Petersen (1993)).

The results of this research are reported in Table 6. The CCR and A&P models using the 2003 data are both the results of self-appraisal. The better DMU among the top 30 fabless firms are Nvidia, Broadcom, ATI, Altera, Marvell, Qlogic, Silicon, OVTI, Genesis, and Ali. The poorer ones with efficiency values below 0.6 are Mega Chips, Conexant, ICS, SST, Xilinx, Cirruss, VIA, Globespan, Sunplus, Qualcomm, and Realtek. The more often the DMU appears in reference lists, the more robust that DMU's efficiency is. The number of times each company was listed is thus: Genesis (8), Ali (8), Nvidia (7), ATI (7), Altera (7), OVTI (6), and Silicon (5).

The comparison of ordinal scale efficiency: From the averages of different efficiencies in Table 6, the A&P and the Cross-Efficiency models scored highest while the CCR model

Table 6 CCR efficiency, A&P efficiency, and cross-efficiency

Number	DMU	CCR efficiency	Reference set	Cross-reference times	A&P efficiency	Cross-efficiency
1	Qualcomm	0.3026	1, 2, 4, 7, 24	0	0.3026	3.4954
2	Nvidia	1	2	7	1.8221	2.3285
3	Broadcom	1	3	1	1.0372	1.7767
4	ATI	1	4	7	1.1742	1.8704
5	Xilinx	0.4305	5	3	0.4305	1.8338
6	MediaTek	0.6456	2, 4, 6, 7, 24	0	0.6456	1.6768
7	SanDisk	0.6678	7	2	0.6678	1.5567
8	Altera	1	8	7	2.0289	1.2688
9	Marvell	1	9	1	1.5881	1.2143
10	Conexant	0.5838	2, 4, 8, 10, 30	0	0.5838	0.9960
11	VIA	0.3505	2, 4, 8, 11, 30	0	0.3505	0.9341
12	Qlogic	1	12	0	1.1501	0.8869
13	Adaptec	0.6989	3, 8, 9, 13, 17	0	0.6989	0.6987
14	Globespan	0.3404	2,8,14,17,30	0	0.3404	0.7157
15	Aeroflex	0.9225	15	0	0.9225	0.6586
16	Sunplus	0.3231	2, 8, 16, 17, 30	0	0.3231	0.6680
17	Silicon	1	17	5	1.1043	0.6472
18	Novatek	0.7202	8, 17, 18, 26, 30	1	0.7202	0.6518
19	SST	0.4362	4, 19, 24, 26	0	0.4362	0.6036
20	Realtek	0.2780	2, 4, 18, 20, 26, 30	0	0.2780	0.6259
21	MegaChips	0.5916	21	1	0.5916	0.5716
22	ICS	0.5498	4, 5, 22, 24, 26	0	0.5498	0.6046
23	PMC-Sierra	0.2656	8, 17, 23, 26, 30	0	0.2656	0.5605
24	OVTI	1	24	6	1.5652	0.5490
25	Zoran	0.9607	25	0	0.9607	0.4934
26	Genesis	1	26	8	1.3605	0.4845
27	Cirruss	0.4172	21, 26, 27, 30	0	0.4172	0.4943
28	ESS	0.8761	5, 24, 26, 28	0	0.8761	0.4577
29	Semtech	0.6567	5, 24, 26, 29	0	0.6567	0.4882
30	Ali	1	30	8	1.0701	0.4753

scored the lowest. Regarding the discriminating power, the efficiency value of 10 DMUs were 1 by the CCR model, so the efficiency value is unable to differentiate which one is better; some other reference sets are needed. However, the discrimination of the other two efficiency evaluations was better than that of the CCR model. Among them, A&P was the extension of the CCR model, so it had better discrimination. Table 7 lists all DMU ranks under each model and the relevant analysis for discussing the efficiency influence of the three models. The data after ranking is an ordinal scale type, so it is suitable to use the Spearman Rank-Order Correlation so that its coefficient correlation can show the consistent degree between four ranking groups.

There is high degree of correlation between rating by CCR efficiency and by A&P efficiency, since A&P model is an extension of the CCR model. For DMUs with an efficiency score less than 1, their ratings are the same either by CCR efficiency or A&P efficiency. Cross efficiency is a peer-evaluation type, their efficiency scores were obtained through subjective assessing and there was a high degree of correlation related to the efficiency score rating among DMUs by this model. The correlation coefficient can be as high as 0.959. If one considers three models together, the lowest correlation coefficient is 0.023, which implies that all kinds of models have positive correlation. Consequently, those DMUs that perform well will have higher ranking regardless of the models used.

Comparing the efficiency of the CCR and BCC models

If one subdivides the Integrated Efficiency (CCR efficiency), one can find that inefficiency comes from a lack of Pure Technological Efficiency (BCC efficiency) or Scale Efficiency. It means that the Integrated Technological Efficiency is the product of Pure Technological Efficiency and Scale Efficiency, representing the whole R&D efficiency of the top 30 fabless firms. Pure Technological Efficiency means the efficient application of inputs from every firm in the current year, so that it can reach the goal of minimum input

Table 7 DMU ranking based on efficiency scores by different models

DMU	Reference times of CCR efficiency	A&P efficiency	Cross-efficiency
Qualcomm	28	28	1
Nvidia	3	2	2
Broadcom	8	9	5
ATI	3	7	3
Xilinx	23	23	4
MediaTek	18	19	6
SanDisk	16	16	7
Altera	3	1	8
Marvell	8	3	9
Conexant	20	20	10
VIA	25	25	11
Qlogic	10	5	12
Adaptec	15	15	14
Globespan	26	26	13
Aeroflex	12	12	16
Sunplus	27	27	15
Silicon	7	8	17
Novatek	14	14	20
SST	22	22	18
Realtek	29	29	21
MegaChips	19	17	19
ICS	21	21	22
PMC-Sierra	30	30	23
OVTI	6	4	25
Zoran	11	11	26
Genesis	1	6	24
Cirruss	24	24	30
ESS	13	13	27
Semtech	17	18	28
Ali	1	10	29
Correlation coefficient (based on CCR efficiency & referenced times)	1	0.959	0.023
Correlation coefficient (based on A&P efficiency)	0.959	1	0.095
Correlation coefficient (based on cross-efficiency)	0.023	0.095	1

and maximum output. Its value shows the applied efficiency of input, and the Scale Efficiency represents the appropriate proportion of input and output of every firm in every year to reach maximum productivity. Greater values indicate more suitable scales and hence greater productivity.

Table 8 shows that inefficiency comes totally from a lack of Pure Technological Efficiency. For instance, Realtek, PMC-Sierra, Qualcomm, Sunplus, Globespan, VIA, SST, Cirruss, ICS, Conexant, MediaTek, and Novatek 13 are thirteen companies with an inefficient application of inputs. Authors found the scale inefficient companies were Xilinx, MegaChips, Semtech, SanDisk, Adaptec, Cirruss, ESS, Aeroflex, SST, Zoran, VIA, Conexant, PMC-Sierra, and Globespan 14. In addition, six unfortunate companies lacked both the Pure Technological Efficiency and Scale Efficiency: Cirruss, SST, VIA, Conexant, PMC-Sierra, and Globespan. The reason behind their lack of Integrated Technological Efficiency came more from the degree in which they lacked Pure Technological Efficiency than from their scale inefficiency. This inclination showed that the low technology inefficiency did not affect production scale. However, there were five companies—Xilinx, MegaChips, Semtech, SanDisk, and Adaptec—that had more serious problems of scale inefficiency. In scale inefficiency, Scale Returns of these five firms might increase or decrease progressively. The suggested improvements are listed in the following analysis.

Scale return analysis

Calculation of DMU efficiency scores by CCR model is based on the assumption of fixed scale return. In this situation, the DMU inefficiency operation might come from a different Scale Return. When the Scale Efficiency value is equal to 1, it is a Fixed Scale Return. However, when it is not 1, the Scale Return increases or decreases accordingly. The larger the deviation, the greater is the increase or decrease in scale return. As was explained in the second paragraph of Sect. "Research methods", authors found all DMUs

Table 8 CCR efficiency, BCC efficiency and scale return of each fabless

DMU/Efficiency	CCR model	BCC model	Scale model
Qualcomm	0.3026	0.3026	1
Nvidia	1	1	1
Broadcom	1	1	1
ATI	1	1	1
Xilinx	0.4305	1	0.4305
MediaTek	0.6456	0.6456	1
SanDisk	0.6678	1	0.6678
Altera	1	1	1
Marvell	1	1	1
Conexant	0.5838	0.6035	0.9674
VIA	0.3505	0.3648	0.9608
Qlogic	1	1	1
Adaptec	0.6989	1	0.6989
Globespan	0.3404	0.3415	0.9968
Aeroflex	0.9225	1	0.9225
Sunplus	0.3231	0.3231	1
Silicon	1	1	1
Novatek	0.7202	0.7202	1
SST	0.4362	0.4554	0.9578
Realtek	0.2780	0.2780	1
MegaChips	0.5916	1	0.5916
ICS	0.5498	0.5498	1
PMC-Sierra	0.2656	0.2696	0.9852
OVTI	1	1	1
Zoran	0.9607	1	0.9607
Genesis	1	1	1
Cirruss	0.4172	0.5113	0.8160
ESS	0.8761	1	0.8761
Semtech	0.6567	1	0.6567
Ali	1	1	1

Reference: The discrimination of scale returns: In the above Table, when $p<0$, the scale returns decrease progressively; when $p=0$, the scale returns are fixed; when $p>0$, the scale returns increase progressively (p value is the c value of BBC) had only two kinds of Scale Returns - fixed and progressively increasing – instead of progressively increasing only. Among these 30 firms, the ones with progressively increasing included Globespan, PMC-Sierra, VIA, Conexant, SST, Zoran, Ali, Semtech, Adaptec and Genesis. For DMU with sharp increase in Scale Return, the output increase rate is greater than the input increase rate, so as to expand Capital stock, Net Working Capital, and Long-Term Investments Table 9.

Discussion

The 2003 performance of the top 30 fabless firms used the ratio of input and output to find the relative efficiency of each company. The selection of the input and output values in this research was evaluated by experts' discussions and the two-stage coefficient correlation of input and output data that fit in with the DEA analysis. The evaluation of operation performance was divided into three stages: the evaluation of operation, the evaluation of outputs, and the evaluation of benefits. This research relies on the reference set and the four improvement types of DEA evaluations for differentiating the operation performance of the 30 fabless firms in 2003 (Tables 4 and 5) and probes into and compares the four DEA methods at the same time.

After analyzing and comparing the results, this research can give us the result of the competitive orientation and relative operation performance; moreover, it provides fabless industry the reference and basis for the development of specific policies. The performance evaluation of a fabless should not use a single financial input and output index. Using a single output weight value, or making comparisons with just a few companies, would result in inaccuracy. Therefore, our approach can obtain the weight of each standard objectively by using the DEA model of multi-input and multi-output in this research while at the same time find the objective analysis and orientation to evaluate the operation performance of global fabless firms. The author's hope that, on the strength of these results and the relevant business efficiency, this information could provide decision-makers with the references needed to improve their operation efficiency and wise allocation of resources.

Table 9 Scale return assessment

DMU/Efficiency	CCR	Scale efficiency	P	Scale return
Qualcomm	0.3026	1	0	Fixed
Nvidia	1	1	0	Fixed
Broadcom	1	1	0	Fixed
ATI	1	1	0	Fixed
Xilinx	0.4305	0.4305	0	Fixed
MediaTek	0.6456	1	0	Fixed
SanDisk	0.6678	0.6678	0	Fixed
Altera	1	1	0	Fixed
Marvell	1	1	0	Fixed
Conexant	0.5838	0.9674	0.3739	Increase
VIA	0.3505	0.9608	0.2267	Increase
Qlogic	1	1	0	Fixed
Adaptec	0.6989	0.6989	5.1775	Increase
Globespan	0.3404	0.9968	0.1204	Increase
Aeroflex	0.9225	0.9225	0	Fixed
Sunplus	0.3231	1	0	Fixed
Silicon	1	1	0	Fixed
Novatek	0.7202	1	0	Fixed
SST	0.4362	0.9578	0.6479	Increase
Realtek	0.2780	1	0	Fixed
MegaChips	0.5916	0.5916	0	Fixed
ICS	0.5498	1	0	Fixed
PMC-Sierra	0.2656	0.9852	0.1398	Increase
OVTI	1	1	0	Fixed
Zoran	0.9607	0.9607	1.1807	Increase
Genesis	1	1	5.3252	Increase
Cirruss	0.4172	0.8160	0	Fixed
ESS	0.8761	0.8761	0	Fixed
Semtech	0.6567	0.6567	5.1336	Increase
Ali	1	1	3.8388	Increase

Remark: Scale return discrimination: $p < 0$ shows a decrease in scale return; $p = 0$ shows a fixed scale return; $p > 0$ shows an increase in scale return

Conclusions and recommendations

Fabless firms play an important role in the global semiconductor industry, an industry that has been booming over the past 20 years. Authors used the DEA to evaluate the operation performances of the top 30 fabless firms and also used the DEA efficiency value to evaluate cost effectiveness. This model can not only compare and assess efficiency, but it also offers relevant resource allocation and improves management. DEA is different from the traditional financial achievements or the single comparison index. In rest of this section the authors conclude based on an objective comparison of the top 30 fabless firms and follow that with suggestions and recommendations to improve the performances by reviewing inputs and outputs.

Conclusions

Results of various efficiency rank analyses: The DMU rank coefficient correlation of the A&P and CCR models was 0.959. The DMU rank of the A&P and Cross-Efficiency model was 0.095. The DMU coefficient correlation rank of the Cross-Efficiency model was 0.023. From the lowest value 0.023 of the Spearman rank coefficient correlation of the three models, the rank results of A&P and CCR showed the positive correlation. Regarding discrimination, the CCR model must have the reference times while A&P found the solution just once to obtain the same discrimination ability that the CCR model had.

Results of operation performance evaluations: Both the A&P and CCR models are the results of self-appraisal. The better DMUs among the top 30 fabless firms were Nvidia, Broadcom, ATI, Altera, Marvell, Qlogic, Silicon, OVTI, Genesis, and Ali. The weaker firms with efficiency values smaller than 0.6 were Mega Chips, Conexant, ICS, SST, Xilinx, Cirruss, VIA, Globespan, Sunplus, Qualcomm, and Realtek. The more often a company appears as a reference, the more robust the DMU efficiency gets. The rankings of the reference times were Genesis (8), Ali (8), Nvidia (7), ATI (7), Altera (7), OVTI (6), and Silicon (5).

The Cross-Efficiency model was the result of peer-appraisal. The better DMUs among the top 30 fabless firms were these nine: Qualcomm, Nvidia, ATI, Xilinx, Broadcom, MediaTek, SanDisk, Altera, and Marvell. The worst DMUs (with efficiency values lower than 0.6) were MegaChips, the PMC-Sierra, OVTI, Cirruss Logic, Zoran, Semtech, Genesis Micro, and Ali.

Inefficiency source: From the results of CCR and BCC analysis, one could learn that the inefficiency came totally from a lack of Pure Technological Efficiency. Realtek, PMC-Sierra, Qualcomm, Sunplus, Globespan, VIA, SST, Cirruss, ICS, Conexant, MediaTek, and Novatek are 13 companies with an inefficient application of inputs. The 14 scale inefficient companies were Xilinx, MegaChips, Semtech, SanDisk, Adaptec, Cirruss, ESS, Aeroflex, SST, Zoran, VIA, Conexant, PMC-Sierra, and Globespan. In addition, authors found six companies, Cirruss, SST, VIA, Conexant, PMC-Sierra, and Globespan, in the case that lacked both Pure Technological Efficiency and Scale Efficiency, The reason behind their lacking of Integrated Technological Efficiency came more from their lacking of Pure Technological Efficiency than from their scale inefficiency; this implied that low technology inefficiency would not affect production scale. However, there were five companies—Xilinx, MegaChips, Semtech, SanDisk, and Adaptec—that had more serious problems with scale inefficiency. In the scale inefficiency, their scale returns might increase or decrease progressively.

Analysis of the Scale Returns: From the Scale Returns of the top 30 fabless firms in 2003, authors found that all DMU fall into two types: fixed or progressively increasing. This was surprising because authors expected only one type: progressively increasing. Among the firms studied, the companies that increased progressively were Globespan, PMC-Sierra, VIA, Conexant, SST, Zoran, Ali, Semtech, Adaptec, and Genesis. Since the increasing rate of output was greater than input, these firms should expand their Capital Stock, Net Working Capital, and Long-Term Investment expenditures.

Recommendations

From the relevant documents and interviews with business leaders, authors know that every manager pays much attention to evaluating operation performance, both internally and externally. On the basis of every company's orientation and mission, the evaluation also involves the progressive efficiency and deferred performance. Thus, it is hard to set up an effective integrated evaluation model and select a suitable index and fair weight of evaluation. Authors have tried to solve the above-mentioned problems by using the DEA model in this research and have presented objective results that authors hope will help fabless firms conduct better internal evaluations.

In order to promote the operation performance of 20 firms with Fixed Scale Returns, it is necessary to strengthen the efficient application of the input Capital Stock, Net Working Capital, and Long-Term Investments to expand the Revenue and Earnings before Taxes of every company.

Authors found 13 companies with inefficient technology that should strengthen their technical management and development. Especially regarding input resource application, they should finish the collection and the establishment of input and output data for every company as quickly as possible. This would help those companies carry out further research and evaluation and more accurately adjust their resource applications and distributions.

Appendix

Table A.1 Preliminary selection of input/output items

Assessing items/Criteria	Data source and reliability	Controllable	Same period of time	Assessing criteria	Performance correlation
R&D expense	○	○	Δ	○	○
Fixed assets	○	○	Δ	○	○
Intangible assets	Δ	Δ	Δ	Δ	○
Capital stock	○	○	Δ	○	○
Cash	○	○	Δ	○	○
Net working capital	○	○	Δ	○	○
Long term investments	○	○	Δ	○	○
Debt ratio	○	Δ	Δ	Δ	Δ
Revenue	○	○	Δ	○	○
Earnings before taxes (EBT)	○	○	Δ	○	○
Net income before preferred dividends	○	Δ	Δ	○	○
Earning per share	○	○	Δ	○	○
Return on common equity(ROE)	○	○	Δ	○	○
Return on assets(ROA)	○	○	Δ	○	○
Turnover ratio	○	○	Δ	○	○

Remark: ○ = 100% matched, Δ = average, X = non-matching those listed above are matched items

Table A.2 2003 global inputs–outputs data sheet (5×5) Unit: US$ Thousand

Fabless /items	Input					Output				
	R&D expense	Fixed assets	Capital stock	Net working capital	Long-term investments	Revenue	EBT	EPS	ROE (%)	Turnover ratio (%)
Qualcomm	523,267	622,265	789,586	2,624,559	1,120,927	2,466,331	1,285,147	1.05	10.48	27.96
Nvidia	269,972	190,029	153,513	328,979	190,029	1,822,945	86,673	0.59	7.08	130.27
Broadcom	434,018	142,113	292,009	444,931	41,097	1,610,095	(934,738)	(3.29)	−64.43	79.80
ATI	248,800	711,100	237,227	92,600	711,100	1,510,992	(280,200)	0.15	−180.08	80.16
Xilinx	247,609	335,114	337,069	458,805	1,091,697	1,299,900	350,544	0.37	12.20	44.25
MediaTek	119,697	31,775	192,856	673,456	347,266	1,115,931	500,669	0.79	46.06	90.66
SanDisk	84,200	59,470	144,781	812,977	185,062	1,079,801	241,881	1.17	11.25	53.36
Altera	178,543	160,924	381,387	111,771	14,451	827,207	212,501	0.41	14.07	55.61
Marvell	213,740	149,705	127,456	287,499	0	819,762	63,352	0.09	2.08	33.66
Conexant	159,354	36,310	303,488	133,734	119,230	633,100	23,433	0.09	−422.94	67.95
VIA	72,856	57,986	379,295	175,804	368,543	597,664	(50,016)	(0.04)	55.18	68.34
Qlogic	87,755	67,224	103,473	206,342	0	516,200	215,601	1.11	15.41	55.59
Adaptec	123,022	58,435	106,772	170,487	6,346	437,200	(189,160)	(0.14)	−30.42	41.59
Globespan	159,354	36,310	268,586	133,734	119,230	379,100	23,433	0.09	−422.94	40.69
Aeroflex	31,102	69,080	60,193	161,556	0	341,028	12,883	0.14	2.47	103.15
Sunplus	45,928	41,883	192,856	116,249	127,658	325,349	60,817	0.79	14.71	66.76
Silicon	48,296	30,712	48,850	81,138	0	325,305	66,196	0.86	15.57	165.07
Novatek	17,952	18,130	102,535	80,454	18,933	319,706	64,414	0.19	39.10	122.63
SST	43,144	11,325	94,723	175,866	83,046	295,041	(38,751)	0.06	−19.66	74.44
Realtek	42,984	40,594	197,597	170,718	117,630	272,005	84,613	0.13	16.23	1.33
MegaChips	10,275	7,203	246,610	115,178	1,248	271,297	2,795	0.07	1.24	163.08
ICS	35,006	15,749	67,898	163,687	32,000	256,900	71,541	0.87	22.55	81.52
PMC-Sierra	119,473	20,750	173,568	198,327	52,905	249,483	(15,843)	(0.05)	−3.53	45.12
OVTI	15,500	20,622	22,678	254,761	7,110	249,400	89,008	0.68	19.58	72.12
Zoran	40,402	20,029	33,231	67,954	0	216,528	(66,615)	(2.05)	−12.72	35.04
Genesis	30,983	17,257	31,248	48,670	0	213,400	(5,268)	(0.47)	−1.09	51.96
Cirruss	76,168	22,663	83,445	143,199	6,996	198,200	39,444	(2.39)	21.72	62.99
ESS	33,184	24,629	39,517	79,313	9,076	195,273	40,894	0.64	11.14	55.38
Semtech	30,371	49,579	73,013	124,048	86,119	192,079	42,718	0.47	8.55	47.02
Ali	41,512	42,125	51,594	(21,439)	41,730	191,082	152	0.001	17.00	115.43

Table A.3 Correlation between input/output items using Pearson correlation coefficients

Output/CC/Input	R&D expense	Fixed assets	Capital stock	Net working capital	Long-term investments
Revenue	0.907	0.783	0.711	0.731	0.722
EBT	0.183	0.305	0.579	0.709	0.535
EPS	−0.166	0.116	0.095	0.210	0.227
ROE	−0.208	−0.110	−0.189	0.108	−0.032
ROA	−0.206	−0.147	−0.230	−0.239	−0.215

Table A.4 Glossary

Fabless:	IC design company
DEA:	Data envelopment analysis
CCR:	DEA model created by Charnes, Cooper and Rhodes
A&P:	DEA model proposed by Andersen and Petersen
BCC:	DEA model addressed by Banker, Charnes and Cooper
DMUs:	Decision management units
OEM:	Original equipment manufacturer
MCDM:	Multi-criteria decision making
MOPA:	Multi-object programming approach
SE:	Scale efficiency
TE:	Technical efficiency
CDMA:	Code division multiple access
FPGA:	Field-programmable gate array
WLAN:	Wireless local area network
IDM:	Integrated device manufacturer
CMOS:	Complementary metal-oxide-semiconductor
LCD:	Liquid crystal display
DRAM:	Dynamic random access memory
DDS:	Digital data storage
EBT:	Revenue and earnings before taxes
DSC:	Digital still camera

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