HIGH-SPEED DIVIDE-BY-4/5 PRESCALERS WITH MERGED AND GATES USING GaInP/GaAs HBT AND SiGe HBT TECHNOLOGIES

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ABSTRACT: *This paper demonstrates the divide-by-4/5 prescalers with merged AND gates in 2-μm GaInP/GaAs heterojunction bipolar transistor (HBT) and 0.35-μm SiGe HBT technologies. By biasing the HBT near the peak transit-time frequency (f_T), the maximum operating frequency of a D-type flip-flop can be promoted. At the supply voltage of 5 V, the GaInP/GaAs prescaler operates from 30 MHz to 5.2 GHz, and the SiGe prescaler has the higher-speed performance of 1–8 GHz at the cost of power consumption.* © 2008 Wiley Periodicals, Inc. Microwave Opt Technol Lett 50: 1498–1500, 2008; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.23407

Key words: *heterojunction bipolar transistor (HBT); GaInP/GaAs; SiGe; dual-modulus; divide-by-4/5; prescaler; emitter-couple logic (ECL)*

1. INTRODUCTION

Recently, the personal wireless communication system is growing rapidly. The faster and accurate frequency synthesizer or phase-locked loops (PLL) system are required at the transceiver for more efficient usage of finite channels. A prescaler plays an important role because it dominates the maximum operating frequency and power consumption of the frequency synthesizer and PLL system.

In the integer-N synthesizer, the reference frequency, f_{REF}, determines the channel space. For high-resolution requirement, the reference frequency must be reduced at the cost of the bandwidth. To overcome this trade-off problem, fractional-N structure is proposed, which f_{REF} higher than channel space can increase the loop-bandwidth without the degradation of the resolution. This kind of synthesizer generally uses the dual-modulus prescaler with the programmable divide-by-N/N + 1 to achieve the fractional-N function, such as divide-by-2/3 or divide-by-4/5 prescaler.

For the multichannel application, a synchronous divide-by-4/5 prescaler combined with several asynchronous divide-by-2 prescalers and a digital-control circuit generates different divide ratios, as shown in Figure 1. Because the input port directly receives the high-speed clock (CLK) signal, the current-mode logic [1] is suitable to the divide-by-4/5 prescaler. As to the asynchronous dividers, true single-phase-clock prescalers [2, 3] are adopted, which usually operate at lower frequencies because of the charge rearrangement, circuit delay, and the requirement of large voltage swing. As mentioned earlier, the divde-by-4/5 prescaler [4] is originally composed of three D-type flip-flops (D-FFs) and two separated NAND gates. More gate-delay slows down the maximum operating frequency. Therefore, a D-FF with a merged AND gate is widely utilized in the dual modulus prescalers. According to the previous literatures, the merged-gate divide-by-4/5 prescalers are already demonstrated in the silicon [5, 6] and GaAs FET [7] processes.

In this paper, the divde-by-4/5 prescaler is first demonstrated in 2-μm GaInP/GaAs heterojunction bipolar transistor (HBT) technology successfully. The GaInP/GaAs HBT technology with the peak unit-gain frequency (f_T) of 30–40 GHz has several advantages, such as the low base resistance, the suppressed 1/f noise, the accurate thin film resistors, and the semi-insulating GaAs substrate. For instance, the accurate resistor allows designers to correctly estimate the required voltage swing for specified signal-to-noise ratio, and to easily bias required current density. Another is implemented in 0.35-μm SiGe HBT technology. Because of graded bandgap in the SiGe base layer, the increasing quasielectric field reduces the transit-time across the base layer. Therefore, the SiGe HBT with enhanced cutoff frequency becomes suitable for the higher frequency applications and for the integration with the digital CMOS process. The design issues are discussed in the next section. Finally, Section 3 describes the fabrication and performance.

2. CIRCUIT DESIGN

In the conventional divide-by-4/5 prescalers, a D-type latch composed of the differential pair and the cross-coupled regenerative pair is an essential subcircuit. The multilevel (series-gated) structure can sense different inputs simultaneously. Figure 2 shows the static D-FF structures without and with merged AND gate, which are bilevel and trilevel structures, respectively. Compared with the conventional divide-by-4/5 topology, the AND gate merged into the D-FF reduces the propagation delay and DC power dissipation because of omitting the current sources required for the additional NAND gates. However, the trilevel structure could compress the headroom of each device, especially the transistor, X_1, X_3, and X_{7-8}. Smaller headroom makes device easily enter the saturation region when a large internal swing appears. Compared with SiGe process, GaAs HBT has a higher base-collector turn-on voltage, so as to alleviate this problem.

The current of the emitter-couple logic (ECL) pair can be fully commutated by only several times of the thermal voltage; thus, the D-type latch using HBT has the properties of high speed and low input sensitivity. The switching speed of an ECL can be prompted by increasing the current density, but HBT must be avoided entering the high-level current density region. Because Kirk effect substantially induces the diffusion capacitance of devices, an increase of RC time-constant in the D-latch results in the decrease of f_T. The speed of the clock pair is higher than that of the differential and regenerative pairs, so the current density of clock pair is chosen to operate near the peak of unit-gain frequency (f_T) under the specified output swing. Moreover, the optimization of the device size is important as the current biasing [8]. After optimization, the sizes of the read and latch pairs would be better chosen as the half of the clock pairs. Except for reducing the parasitic

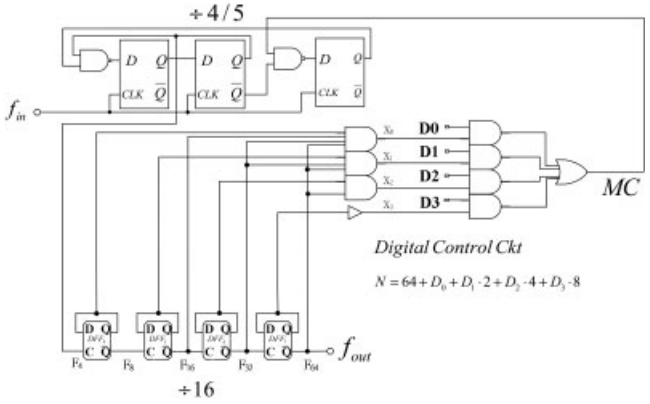

Figure 1 The schematic of the divide-by-64–79 prescaler

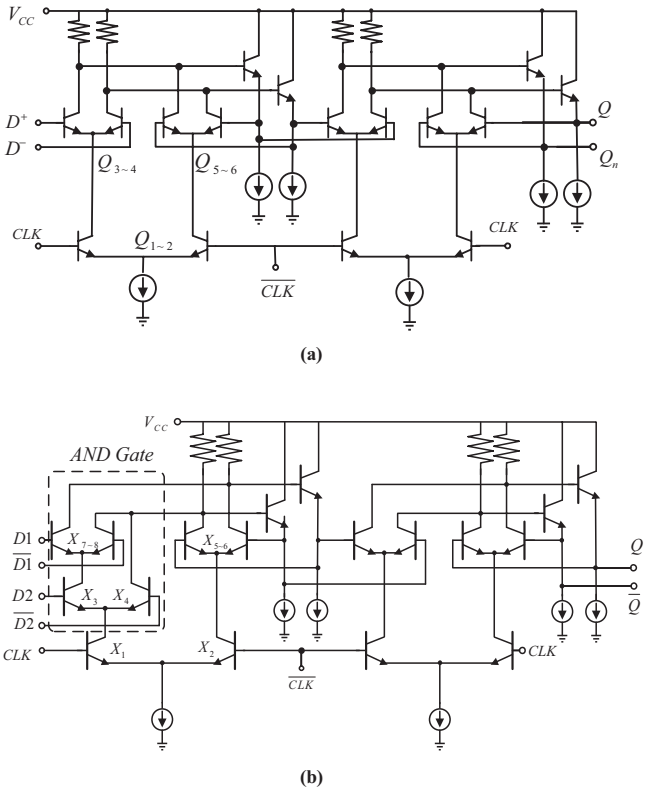

Figure 2 The circuit diagrams of static D-FFs (a) without and (b) with a merged AND gate

capacitances of the loading, they still operate at the high current density as well as the clock pairs.

Figure 3 shows the block diagram of divide-by-4/5 prescaler, including a static D-FF shown in Figure 2(a) and two merged AND-gate D-FF shown in Figure 2(b). When operating at the divide-by-5 mode (MC = 1), the periods of the high (D = 1) and low (D = 0) voltage level are separately three and two CLK cycle. As to the divide-by-4 mode (MC = 0), the DFF_1 is disabled and the delay of the high voltage level is reduced by one CLK cycle.

2.1. GaInP/GaAs HBT Divide-by-4/5 Prescaler

In the static D-FF, the emitter sizes of clock (Q_1–Q_2), read (Q_3–Q_4), and latch (Q_5–Q_6) transistors are 2.0 × 4.0 μm^2, 2.0 × 2.0 μm^2, and 2.0 × 2.0 μm^2, respectively. The emitter sizes of the clock (X_1–X_2), latch (X_5–X_6), and D_1-read (X_7–X_8) in Figure 2(b) are chosen as same as that of the static D-FF except D_2-read pair (X_3–X_4) is sized to 2.0 × 4.0 μm^2. The GaInP/GaAs HBT devices used in the prescaler has the peak f_T of 35 GHz and BV_{CEO} of 13 V. The thin film resistors and MIM Si_3N_4 capacitors are 50 Ω/sq and 0.36 fF/μm^2, respectively.

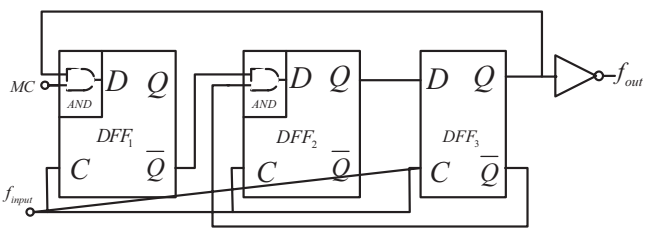

Figure 3 The block diagram of the divide-by-4/5 prescaler with merged AND gates

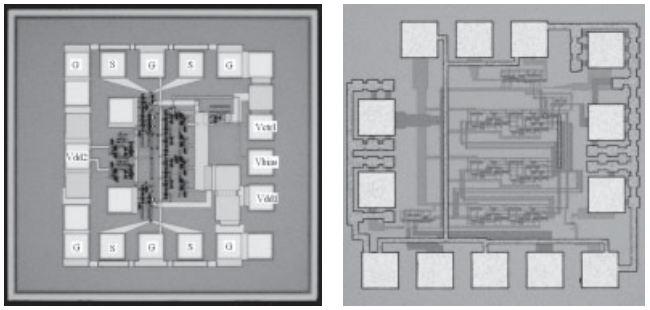

Figure 4 Die photographs of the divide-by-4/5 prescalers using (a) 2-μm GaInP/GaAs HBT and (b) 0.35-μm SiGe HBT technology

2.2. SiGe HBT Divide-by-4/5 Prescaler

All transistors in the SiGe HBT prescaler are the emitter area of 0.3 × 9.9 μm^2, BV_{CEO} of 2.5 V, and the peak f_T of 67 GHz at the current density of 1.343 mA/μm^2 and V_{CE} = 1 V. This device configuration has two base and a single collector contacts. The load resistors and bypass capacitors are 100 Ω/sq N+ poly without silicide and 1 fF/μm^2 MIM, respectively.

3. EXPERIMENTAL RESULTS

The chip photographs of the divide-by-4/5 dividers using 2-μm GaInP/GaAs HBT and 0.35-μm SiGe HBT technology are shown in Figure 4. The former size is 1.0 × 1.0 mm^2 and the later size is 0.85 × 0.80 mm^2. All chips were on-wafer measured by using 50-Ω GSG RF probes, GSGSG RF probes, and DC probes. Then, the single-ended input is fed with the sinusoidal signal by Agilent E8254A Signal Generator and the outputs are measured by Agilent E4407B Spectrum Analyzer.

3.1. GaInP/GaAs HBT Divide-by-4/5 Prescaler

As shown in Figure 5, the operating frequency range of the dual modulus prescalers is from 30 MHz to 5.2 GHz at the CLK current density of 0.192 mA/μm^2. It operates under a core current of 24.9 mA and a supply voltage of 5 V. At low operating frequency, a higher input power is required to increase the slew rate of the sinusoidal signal, and then the period of a nearby differential signal cross-point is shortened. If this period within a small CLK differ-

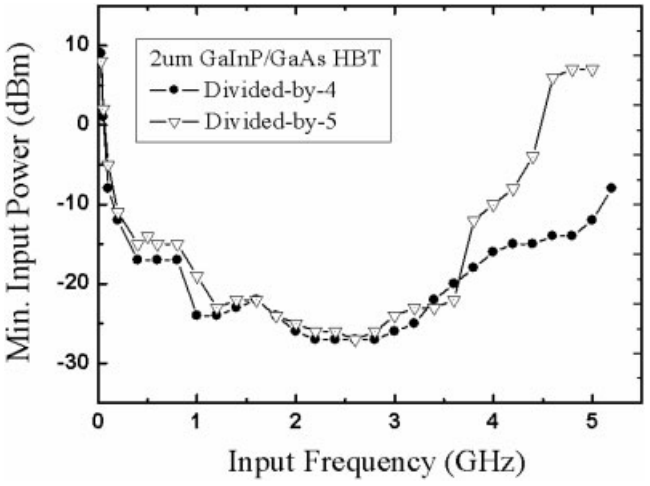

Figure 5 The measured minimum input sensitivity of the 2-μm GaInP/GaAs HBT divide-by-4/5 prescaler

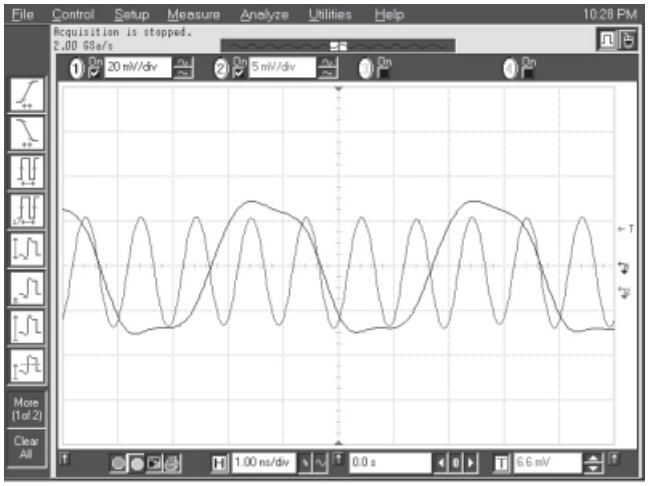

Figure 6 The input and output waveforms of the divide-by-4 mode at the input frequency of 1 GHz

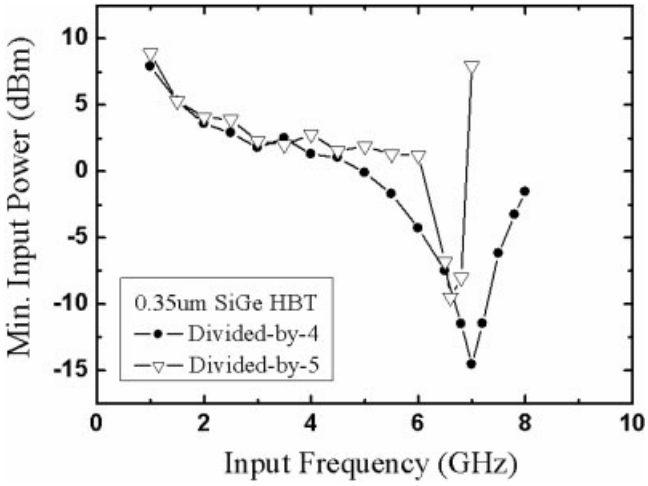

Figure 8 The measured minimum input sensitivity of the 0.35-μm SiGe HBT divide-by-4/5 prescaler

ent voltage is extended because of a slow slew-rate, the self-oscillation will take place and it disturbs the original divide-by-4/5 waveform. Figures 6 and 7 show the input and output waveforms of the different divide modulus at the input frequency of 1 GHz.

3.2. SiGe HBT Divide-by-4/5 Prescaler

Figure 8 represents the input sensitivity as a function of the operating frequency. When the current density of clock transistors is about 1.30 mA/μm^2, the operating frequency range is from 1.0 to 8.0 GHz. The current consumption of the core circuit is 76.5 mA under 5 V supply voltage. The lowest sensitivity points of the divide-by-4/5 occur at 6.7 and 7.0 GHz, respectively.

4. DISCUSSIONS AND CONCLUSIONS

This paper describes the design issues of the divide-by-4/5 prescaler with merged AND gates fabricated in 2-μm GaInP/GaAs HBT and 0.35-μm SiGe HBT technologies. Because the CLK transistors in the D-FF usually operate at higher frequency, how to choose the CLK transistor size and the bias current properly plays an important role. With 5 V supply voltage, the GaInP/GaAs HBT divide-by-4/5 prescaler can operate from 30 MHz to 5.2 GHz. The average sensitivity level is below -10 dBm and the lowest sensitivity is -29 dBm at 2.71 GHz. Meanwhile, a 0.35-μm SiGe divide-by-4/5 HBT prescaler is also designed in the same topology. Based on the compared results, the latter using higher-f_T, SiGe HBT has faster performance of 1–8 GHz at the cost of power consumption.

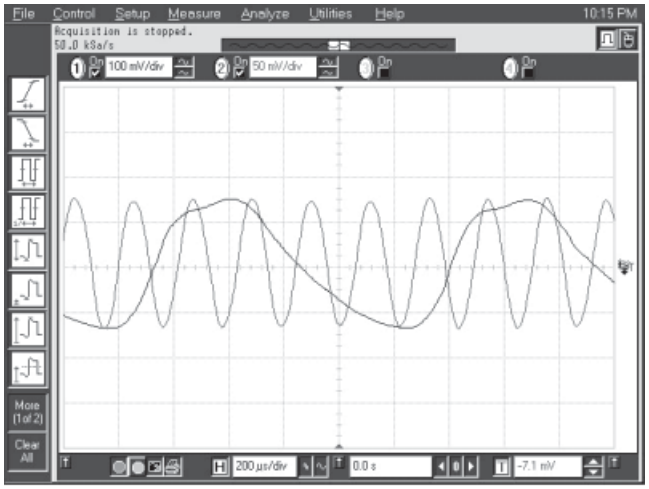

Figure 7 The input and output waveforms of the divide-by-5 mode at the input frequency of 1 GHz

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REFERENCES

1. H.D. Wohlmuth and D. Kehrer, A 15 GHz 256/257 dual-modulus prescaler in 120 nm CMOS, In: Proceedings of the European Solid-State Circuits Conference, 2003, pp. 77–80.
2. C.-Y. Yang, G.-K. Dehng, J.-M. Hsu, and S.-I. Liu, New dynamic flip-flops for high-speed dual-modulus prescaler, IEEE J Solid-State Circuits 33 (1998), 1568–1571.
3. J. Navarro and W. Van Noije, A 1.6-GHz dual modulus prescaler using the extended true-single-phase-clock CMOS circuit technique (E-TSPC), IEEE J Solid-State Circuits 34 (1999), 97–102.
4. K. Herbert, F.M. Thomas, W. Martin, A. Klaus, B. Sabine, and T. Ludwig, A low power 20 GHz SiGe dual-modulus prescaler, In: Proceedings of the IEEE MTT-S International Microwave Symposium Digest 2000, pp. 731–734.
5. K. Herbert, W. Martin, B. Josef, F.M. Thomas, R. Gunter, and A. Klaus, 36 GHz Dual-Modulus Prescaler in SiGe Bipolar Technology, In: Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium Digest 2002, pp. 239–242.
6. W. Hans-Dieter, K. Daniel, T. Ronald, and S. Werner, A 17 GHz Dual-Modulus Prescaler in 120 nm CMOS, In: Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium Digest 2003, pp. 479–482.
7. S. Shoichi, K. Yukio, T. Nobuyuki, K. Katsue, M. Masao, T. Toshituki, and H. Akimichi, A 1 GHz 50mW GaAs Dual Modulus Divider IC, IEEE J Solid-State Circuits 19 (1984), 710–715.
8. S. Shoichi, K. Yukio, T. Nobuyuki, K. Katsue, M. Masao, T. Toshituki, and H. Akimichi, Accurate analytical delay expressions for ECL and CML circuits and their applications to optimizing high-speed bipolar circuits, IEEE J Solid-State Circuits 25 (1990), 572–583.