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Improved Electrical Performance and Reliability of Poly-Si TFTs Fabricated by Drive-In Nickel-Induced Crystallization with Chemical Oxide Layer

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Ni-metal-induced crystallization (MIC) of amorphous Si (α-Si) has been employed to fabricate low-temperature polycrystalline silicon thin-film transistors (TFTs). However, the Ni residues degrade the device performance. In this study, a new method for manufacturing MIC–TFTs using drive-in Ni-induced crystallization with a chemical oxide layer (DICC) is proposed. Compared with that of MIC–TFTs, the on/off current ratio (I_{on}/I_{off}) of DICC–TFTs was increased by a factor of 9.7 from 9.21×10^4 to 8.94×10^5. The leakage current (I_{off}) of DICC–TFTs was 4.06 pA/μm, which was much lower than that of the MIC–TFTs (19.20 pA/μm). DICC–TFTs also possess high immunity against hot-carrier stress and thereby exhibit good reliability.

Key words: Drive-in nickel-induced crystallization, chemical oxide, fluorine ion implantation, metal-induced crystallization, thin-film transistors (TFTs)

INTRODUCTION

Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have attracted considerable interest for their use in active-matrix liquid-crystal displays because they exhibit good electrical properties and can be integrated in peripheral circuits on inexpensive glass substrates.[1] Intensive studies have been carried out to reduce the crystallization temperature and time of amorphous silicon (α-Si) films. Metal-induced crystallization (MIC) is one of these efforts. The advantages of MIC include low cost, good uniformity, low crystallization temperature (~500°C), and short crystallization time (0.5 h to 5 h). The Ni-MIC process produces crystallized α-Si thin films of the best quality, because $NiSi_2$ has the lowest lattice mismatch (0.4%) with Si.[2,3] Unfortunately, Ni and $NiSi_2$ residues in the poly-Si film increase the leakage current and shift the threshold voltage.[4,5] Therefore, Ni concentration in MIC poly-Si should be reduced to enhance device performance. The atomic layer deposition system and gettering method have been employed to reduce the amount of undesired metal impurity. However, both methods are complex and incur high cost.[6–8] Several recent studies have demonstrated that the introduction of fluorine (F) atoms can improve the performance and reliability of poly-Si TFTs, especially under electrical stress. Unfortunately, the minimum off-currents were almost unchanged,[9–11] probably because the Ni concentration was constant.

This study proposes two processes for improving the performance of MIC–TFTs. First, Ni atoms were collided into the α-Si film by fluorine ion implantation. Second, a chemical oxide layer was introduced between the Ni and α-Si layer. With these two processes, the electrical performance and reliability of TFTs were both improved. They showed a 4.73-fold decrease in minimum leakage current and a 9.70-fold increase in on/off current ratio compared with MIC–TFTs.

EXPERIMENTAL PROCEDURES

Three kinds of poly-Si TFTs were investigated in this study: MIC–TFT, fabricated by the traditional

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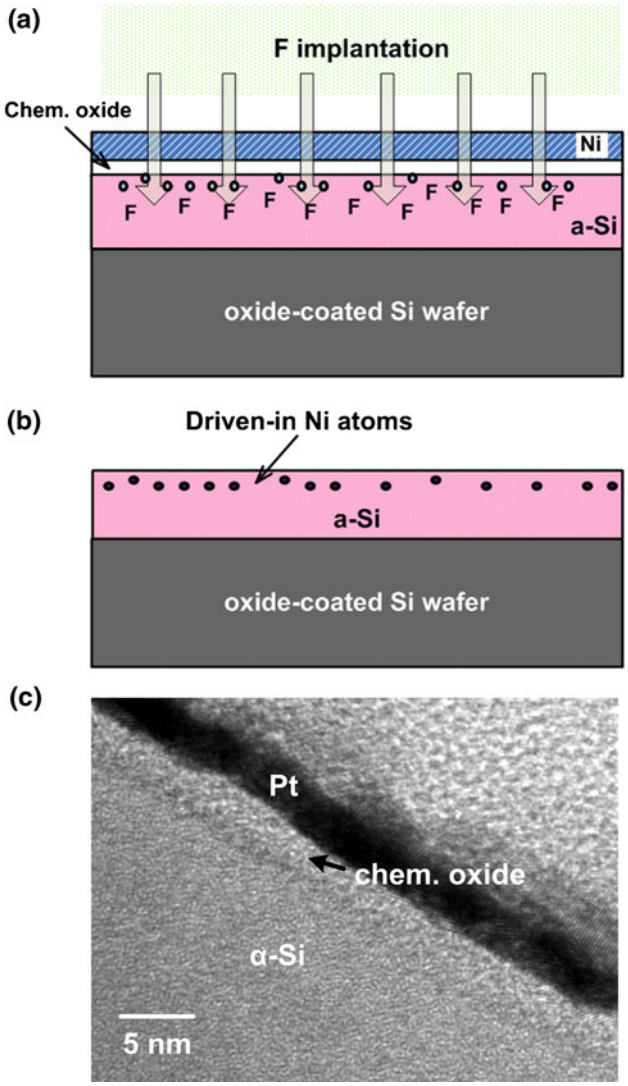

Fig. 1. Schematic illustration of the DICC–TFTs process: (a) F^+ implantation process to drive Ni into the α-Si layer, (b) removal of remaining Ni film and chemical oxide, and (c) TEM image of chemical oxide layer.

Ni-MIC method; DIC–TFT, in which F^+ ions were implanted to drive Ni into the α-Si layer; and DICC–TFT, in which a chemical oxide layer was introduced into DIC–TFT before the F^+ implantation. *n*-Type self-alignment poly-Si TFTs were investigated in this study. A 100-nm-thick undoped α-Si layer was deposited onto a 500-nm-thick oxide-coated Si wafer by using a low-pressure chemical vapor deposition (LPCVD) system.

To fabricate DICC–TFTs, samples were dipped into a mixed solution of H_2SO_4 and H_2O_2 for 20 min to form a chemical oxide (chem-SiO_2) layer on top of the α-Si layer, as shown in Fig. 1c. A 5-nm-thick Ni film was then deposited. Samples were subjected to F^+ implantation to drive Ni into the α-Si layer, as shown in Fig. 1a.

The working and dose ranges of our ion implantation system (E220HP) are from 10 keV to 200 keV and 1×10^{12} cm^{-2} to 5×10^{15} cm^{-2}, respectively. In this study, the ion accelerating energy was set to 10 keV. Simulation software (SRIM) was employed to adjust the projection range. Figure 2 shows the simulation data for the DIC–TFTs and DICC–TFTs. The projection range was set at a depth of 15 nm, near the surface of the α-Si layer. The fluorine ion dose was 2×10^{15} cm^{-2}. To reduce Ni contamination, the remaining Ni film and chemical oxide layer were then removed by wet etching (Fig. 1b). The α-Si was subsequently annealed at 500°C for 1 h in N_2 to achieve crystallization.

DIC–TFTs and MIC–TFTs were prepared for the purpose of comparison. The basic fabrication processes for both TFTs were almost the same as those for DICC–TFTs. In the DIC–TFTs, no chemical oxide layer was introduced. As for MIC–TFTs, the major difference was that the surfaces of the MIC poly-Si did not undergo any F^+ implantation. A 5-nm-thick Ni film was deposited on the α-Si. After annealing at 500°C, the remaining Ni was removed. The deduced crystallization process parameters of all poly-Si films are summarized in Table I. It is

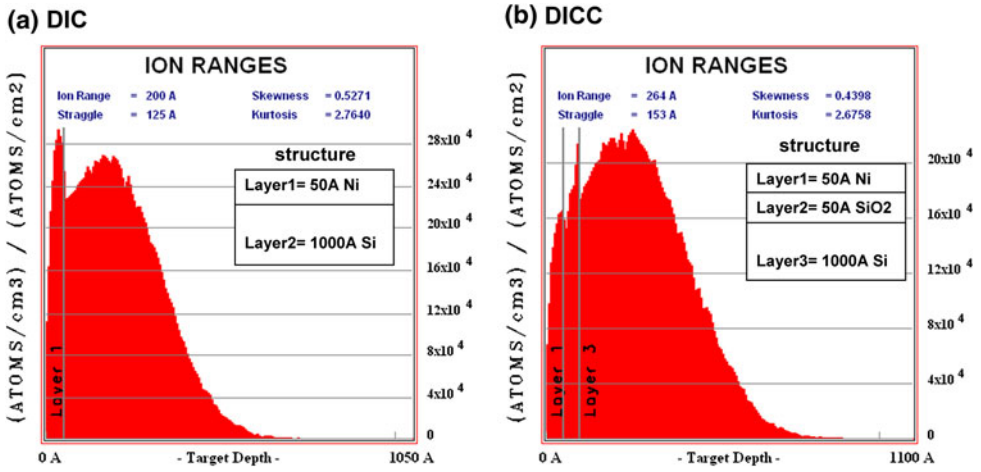

Fig. 2. Simulation data for DIC–TFTs and DICC–TFTs at 10 keV.

Table I. Deduced crystallization process parameters of all poly-Si films

	Chemical Oxide	Implant Energy	Implant Dose
MIC	N/A	N/A	N/A
DIC	N/A	10 keV	5×10^{15}
DICC	5 nm	13 keV	5×10^{15}

worth noting that this DIC process does not need any additional annealing steps and is compatible with MIC processes.

TFT devices were fabricated by standard IC processes. The islands of poly-Si regions on the wafers were defined by reactive-ion etching. Next, a 100-nm-thick tetraethylorthosilicate/O_2 oxide layer was deposited as the gate insulator by plasma-enhanced chemical vapor deposition (PECVD). Then, a 100-nm-thick poly-Si film was deposited as the gate electrode by LPCVD. After defining the gate, self-aligned 35-keV phosphorous ions were implanted at a dose of 5×10^{15} cm^{-2} to form the source/drain and gate. After dopant activation, a 500-nm-thick SiO_2 layer was deposited by PECVD as the passivation layer. Contact holes were formed, and a 500-nm-thick Al layer was then deposited by thermal evaporation and patterned as the electrode. Finally, a sintering process was performed at 400°C for 30 min in N_2 ambient.

RESULTS AND DISCUSSION

Figure 3 exhibits the I_D–V_G transfer characteristics of TFTs at a drain bias of 5 V for W/L = 10 μm/10 μm devices. The measured and extracted key device parameters are summarized in Table II. Ten TFTs were measured in each case to investigate device-to-device variation; average values with standard deviations in parentheses are shown in Table II. As can be seen, the minimum leakage current of DIC–TFTs was much lower than that of conventional MIC–TFTs. In poly-Si film, Ni residues serve as deep-level traps, which promote thermionic emission-dominated leakage current because the Ni concentration in DIC–TFTs was reduced.[12–14] Secondary-ion mass spectroscopy (SIMS) was employed to verify both Ni and F concentrations in TFTs. As shown in Fig. 4a, the DIC process did reduce the Ni content in MIC poly-Si. As a result, the minimum leakage current of DIC–TFTs was much lower than that of conventional MIC–TFTs. Unfortunately, the on-current of DIC–TFTs was lower than that of MIC–TFTs. This degradation might be due to channel damage caused by ion implantation.[15]

To improve this on-current degradation, the DICC process (chemical oxide layer) was applied to the fabrication of DIC–TFTs. As shown in Fig. 3, the on-currents of TFTs were much improved by this

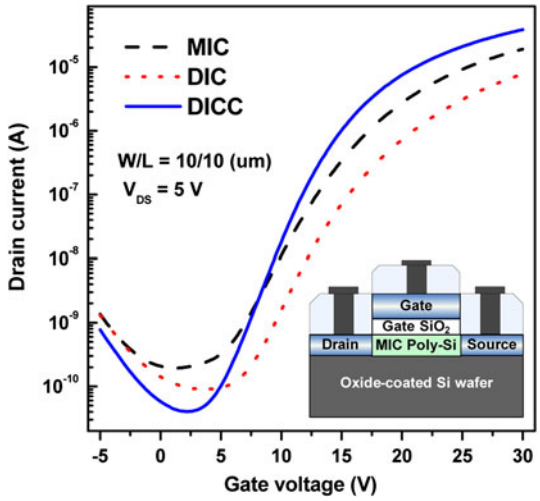

Fig. 3. Typical $I_{DS}-V_{GS}$ transfer characteristics of DIC–TFTs, DICC–TFTs, and MIC–TFTs (W/L = 10 μm/10 μm).

Table II. Average device characteristics of DIC–TFTs, DICC–TFTs, and MIC–TFTs with standard deviations in parentheses

W/L = 10 μm/10 μm	MIC	DIC	DICC
M_{FE} (cm^2/V s)	15.60 (1.13)	10.85 (1.86)	26.70 (1.31)
V_{TH} (V)	12.85 (0.71)	14.99 (1.03)	11.99 (0.18)
S.S. (V/dec)	2.77 (0.12)	2.52 (0.14)	2.06 (0.03)
I_{min} (pA/μm)	19.20 (1.02)	9.08 (3.79)	4.06 (0.22)
Max. on/off ratio ($\times 10^5$)	0.92 (0.07)	1.25 (0.71)	8.94 (0.76)

DICC process. Compared with that of MIC–TFTs, the on/off current ratio (I_{on}/I_{off}) of DIC–TFTs was increased by a factor of 9.7 from 9.21×10^4 to 8.94×10^5. The leakage current (I_{off}) of DICC–TFTs was 4.06 pA/μm, which was much less than that of DIC–TFTs (9.08 pA/μm) and MIC–TFTs (19.20 pA/μm). This improvement is attributed to the reduction of Ni concentration,[12–14] which was verified by SIMS measurement. As shown in Fig. 4a, the Ni content in DICC was lower than that in DIC and MIC. Obviously, the Ni concentration in the channel layer was reduced by the introduction of the chemical oxide layer.

In addition, the improvement of the on-current of DICC–TFTs implies that the chemical oxide layer has ameliorated the channel damage caused by ion implantation. Moreover, as shown in Fig. 4b, high F content is present at the poly-Si/oxide interface, meaning that F atoms have diffused to the interface to terminate Ni-related defects.[10] The on-current of DICC–TFTs was expected to be higher than that of MIC–TFTs, since F atoms can passivate dangling and strain bonds (trap states).[9–11]

To verify the interaction between implant damage and passivation of F^+ implantation on the channel

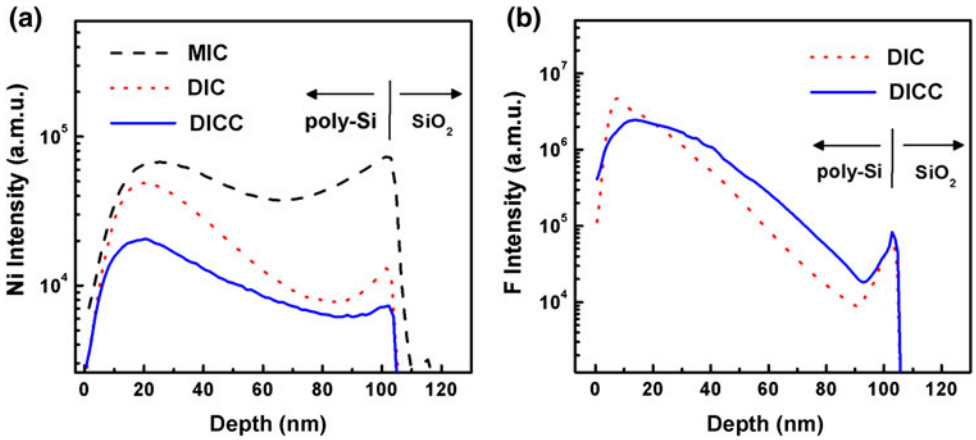

Fig. 4. SIMS depth profiles of (a) nickel and (b) fluorine in the structure of poly-Si films.

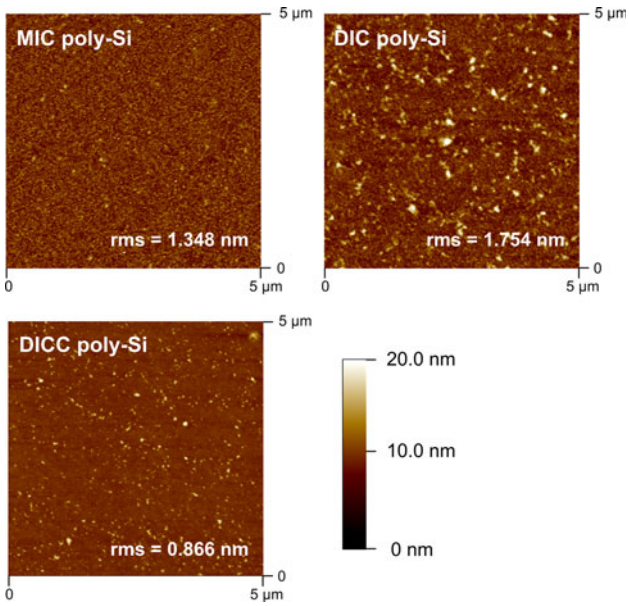

Fig. 5. AFM images and rms roughnesses of poly-Si after remaining Ni and chemical oxide were removed.

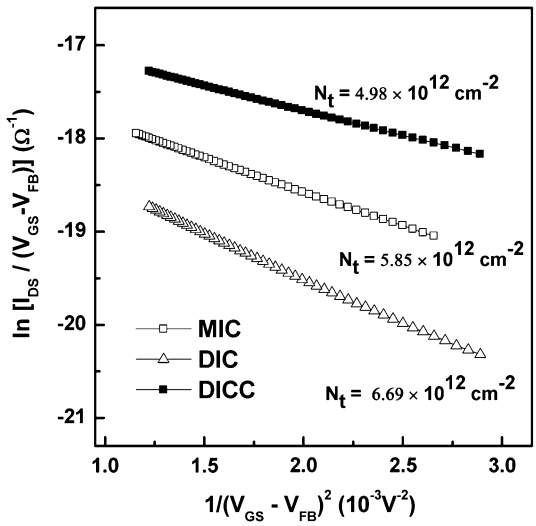

Fig. 6. $\ln[I_{DS}/(V_{GS} - V_{FB})]$ versus $1/(V_{GS} - V_{FB})^2$ at low V_{DS} and high V_{GS} of TFTs.

layer, the surface roughness and effective trap state density (N_t) were measured. The damage of poly-Si surfaces (after the residual Ni and chemical oxide layer were removed) was assessed using atomic force microscopy (AFM). As shown in Fig. 5, the root-mean-square (rms) roughness of MIC, DIC, and DICC films were 1.348 nm, 1.754 nm, and 0.866 nm, respectively. DIC poly-Si has the roughest surface due to ion bombardment.[15] On the other hand, DICC poly-Si has the smoothest surface. The chemical oxide layer did improve surface roughness (reduced implantation damage).

The effective trap state density (N_t) was measured using Levinson and Proano's method, where N_t is estimated from the slope of the linear segment of $\ln[I_{DS}/(V_{GS} - V_{FB})]$ versus $1/(V_{GS} - V_{FB})^2$ at low V_{DS} and high V_{GS}, where V_{FB} is defined as the gate voltage that yields the minimum drain current at $V_{DS} = 0.1$ V.[16,17] As shown in Fig. 6, the N_t of DICC–TFTs was 4.98×10^{12} cm^{-2}, which was much less than that of MIC–TFTs (5.85×10^{12} cm^{-2}) and DIC–TFTs (6.69×10^{12} cm^{-2}).

In other words, there were three major defects related to the performance of MIC–TFTs: (1) Ni concentration (Ni-related defects), (2) grain boundaries, and (3) channel damage. In DIC and DICC, F^+ implantation was employed to drive Ni into the α-Si layer. Compared with MIC, DIC and DICC can reduce the Ni concentration, thus overcoming the Ni-related defects. Moreover, F atoms can passivate dangling bonds and strain bonds, thus improving the negative effects of grain boundaries. However, the on-current of DIC–TFTs was lower than that of MIC–TFTs due to channel damage caused by ion implantation. In DICC, a chemical oxide layer was introduced between the Ni and α-Si layer to reduce

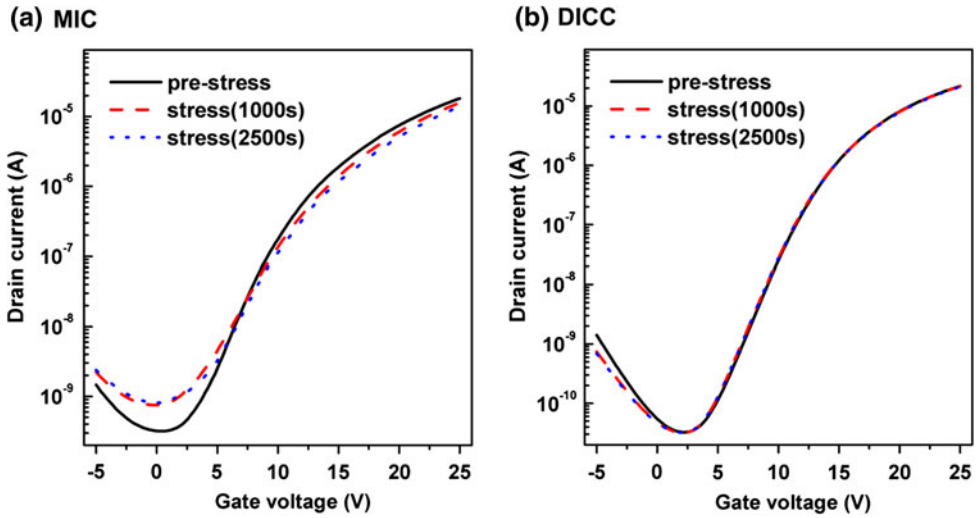

Fig. 7. *I–V* curves of DICC–TFTs and MIC–TFTs after stress.

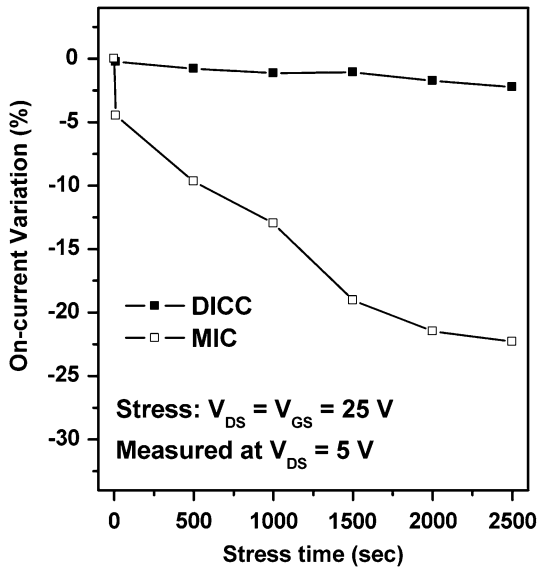

Fig. 8. Variation of on-current versus hot-carrier stress time for the DICC–TFTs and MIC–TFTs.

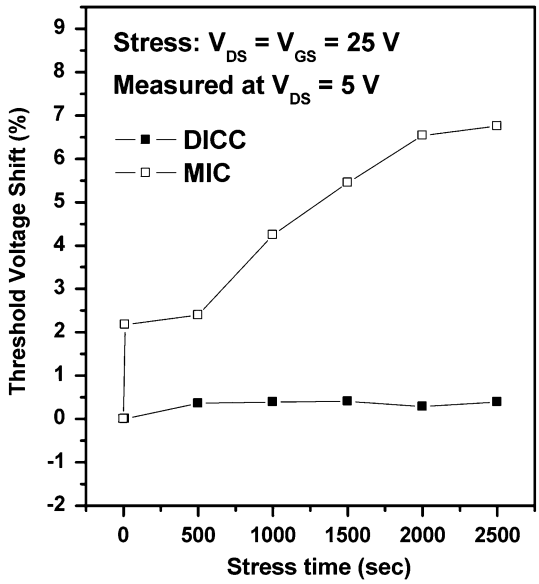

Fig. 9. Variation of threshold voltage versus hot-carrier stress time for the DICC–TFTs and MIC–TFTs.

channel damage. As a result, DICC–TFTs has the highest on-current.

The other important issue of poly-Si TFTs is their reliability, which was examined under hot-carrier stress. In general, the stress voltage was set at the on-state saturation region. Early studies have demonstrated that device degradation increased with stress voltage from 20 V to 30 V. In this case, the stress voltage was set at 25 V ($V_{DS} = V_{GS} = 25$ V for 2500 s).[9,15,18] Figure 7 presents the *I–V* curves of the TFTs. As shown in Figs. 8 and 9, the on-current and the threshold voltage of TFTs were both degraded because dangling bonds were created due to the trapping of electrons at weak Si–Si and Si–H bonds.[19,20] Compared with that of conventional MIC–TFTs, the on-current degradation of DICC–TFTs is greatly improved by F^+ implantation. DICC–TFTs also possess high immunity against the hot-carrier stress and thereby exhibit lower ΔV_{th} and $\Delta I_{on}/I_{on}$, compared with conventional MIC–TFTs. This is because weaker Si–H and Si–Si bonds were replaced by stronger Si–F bonds,[21] which could not be broken under hot-carrier stress, thus leading to improved electrical reliability.

CONCLUSIONS

In this study, an investigation of poly-Si TFTs using the DICC process led to the development of a simple process for manufacturing LTPS TFTs. In

DICC, F^+ implantation was employed to drive Ni into the α-Si layer. This implantation could reduce Ni concentration, and passivate dangling bonds and strained bonds by F atoms. As a result, DICC–TFTs had the lowest leakage current (4.06 pA/μm), which was much lower than that of MIC–TFTs (19.20 pA/μm). In addition, a chemical oxide layer was introduced between the Ni and α-Si layer to reduce channel damage/defects caused by ion implantation. As a result, the on/off current ratio of DICC–TFTs was increased by a factor of 9.7 from 9.21×10^5 to 8.94×10^5 compared with that of MIC–TFTs. It was also found that DICC can greatly alleviate the threshold voltage and on-current degradation under hot-carrier stress. DICC–TFTs possess high immunity against the hot-carrier stress and thereby exhibited lower ΔV_{th} and $\Delta I_{on}/I_{on}$ compared with conventional MIC–TFTs. This is because weaker Si–H and Si–Si bonds were replaced by stronger Si–F bonds, which could not be broken under hot-carrier stress, thus leading to improved electrical reliability.

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